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► To cite this version:

Kremena Makasheva, Christina Villeneuve-Faure, Caroline Bonafos, Christian Laurent, Alessandro Pugliara, et al.. Dielectric engineering of nanostructured layers preventing electrostatic charging in thin dielectrics. Nanotechnology Materials and Devices Conference (NMDC), 2015 IEEE, Sep 2015, Anchorage, United States. 10.1109/NMDC.2015.7439236 . hal-01763535

HAL Id: hal-01763535

<https://hal.science/hal-01763535>

Submitted on 11 Dec 2020

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Dielectric engineering of nanostructured layers preventing electrostatic charging in thin dielectrics

Kremena Makasheva, *Member, IEEE*, Christina Villeneuve-Faure, Caroline Bonafos, Christian Laurent, *Fellow, IEEE*, Alessandro Pugliara, Bernard Despax, Laurent Boudou and Gilbert Teyssedre, *Member, IEEE*

¹**Abstract**—New dielectric-engineering concept is developed intending a net improvement of the performance of dielectric layers under electrical stress. Instead of synthesis of new dielectric materials a new class of dielectric layers that gain their performance from design rather than from composition is established. Two kinds of nanostructured dielectric layers are presented here: (i) silicon oxynitride layers ($\text{SiO}_x\text{N}_y\text{:H}$) with gradual variation of their properties (discrete or continuous), and (ii) SiO_2 layers with tailored interfaces; a single layer of silver nanoparticles (AgNPs) is embedded in the vicinity of the dielectric free surface. Modulation of the conductive properties of the nanostructured layers over 7 orders of magnitude is achieved. The nanostructured layers exhibit much shorter charge retention times and appear promising candidates for general applications where surface charging of dielectrics must be avoided, in particular for implementation in RF MEMS capacitive switches with electrostatic actuation.

Topic — MEMS/NEMS

Index Terms/Keywords — silver nanoparticles, silicon nanoparticles, nanostructured dielectric layers, plasma processes

I. INTRODUCTION

THE electrostatic charging of thin dielectric layers represents an intensive field of scientific research, yet requiring a comprehensive study. The charge injection in dielectrics is at the origin of space charge formation [1, 2] leading in some cases to unexpected behaviour of the dielectric layers under electrical stress. Although the electrostatic charging of thin dielectric layers lays down the principle of operation of various technological devices, like non-volatile memories [3, 4], it is considered as the main cause of electrostatic sticking in MicroElectroMechanical Systems (MEMS) [5-7]. Indeed, the dielectric charging in RF MEMS switches is at the origin of failure and low reliability of capacitive switches with electrostatic actuation. Charge trapping on the surface and in the volume of the dielectric layer leads to a significant increase of the surface potential and to a modification of the values of applied voltage for switch actuation in a way that

after certain number of events the switch is out of control.

This work presents an experimental study on the synthesis, structural and electrical characterization of nanostructured layers preventing the electrostatic charging in thin dielectrics. Instead of synthesis of new materials, a new class of dielectric layers that gain their performance from design rather than from composition is established. Two kinds of nanostructured layers are presented: (i) silicon oxynitride layers ($\text{SiO}_x\text{N}_y\text{:H}$) with gradual variation of their properties (discrete or continuous), and (ii) silica layers (SiO_2) with tailored interfaces; a single layer of silver nanoparticles (AgNPs) is embedded at the vicinity of the dielectric free surface.

II. EXPERIMENTAL PART

The nanostructured dielectric layers were deposited in a Plasma Enhanced Chemical Vapor Deposition (PECVD) process, fully compatible with microelectronic technology. Capacitively coupled radio-frequency (RF) discharges operating at 13.56 MHz and low gas pressure (tens of Pa) were used for deposition [8, 9]. The nanostructured layers with gradual properties (discrete or continuous) are composed of levels of amorphous silicon oxynitride layers ($\text{a-SiO}_x\text{N}_y\text{:H}$, $x < 2$, $y < 1$) with different Si concentration. The plasma precursor ratio $\gamma = [\text{N}_2\text{O}]/[\text{SiH}_4]$ allows adjusting the Si-content in the film. The dielectric layer with $\gamma = 100$ exhibits properties close to a thermal SiO_2 layer. The lower the γ -value, the richer in Si the dielectric layer is. To realize the nanostructured dielectric layer with tailored interfaces a single layer of AgNPs is deposited on thermally grown SiO_2 layer and covered by dielectric layers with different thicknesses of either plasma organosilicon deposits ($\text{SiO}_x\text{C}_y\text{:H}$) or plasma silica (SiO_2) layers.

The nanocomposite layers were structurally characterized by Transmission Electron Microscopy (TEM) in cross-sectional (XS-TEM) and plan view (PV-TEM). The observations were performed using a field emission TEM, FEI TecnaiTM F20 microscope operating at 200 kV, equipped with a spherical aberration corrector and the Gatan Imaging Filter (GIF) TRIDIEM. The Fourier Transform Infrared (FTIR) spectra were acquired with a Bruker Vertex 70 spectrometer in the range $400 - 4000 \text{ cm}^{-1}$. Thicknesses of the nanostructures were determined by spectroscopic ellipsometry using a SOPRA GES-5 ellipsometer. The nanostructured layers were electrically tested under electrical stress and environmental conditions typical for RF MEMS switches. Charge injection and decay dynamics were probed by Kelvin Force Microscopy (KFM) with Multimode 8 Bruker apparatus according to the experimental protocol described in [10].

¹ This work was financially supported by the Agence Nationale de la Recherche in France, project ANR-InTail under contract ANR-AA-PBLI-II-2011. The authors acknowledge financial support from the French CNRS and CEA METSA network for the TEM observations, project METSA 11B14.

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III. RESULTS AND DISCUSSION

A. Silicon oxynitride layers with gradual properties

Dielectric engineering, as performed in this work, allows exploring a large band of operating conditions of the nanostructured layers. To prevent electrostatic charging effects the nanostructures are engineered with a high resistivity layer ($\gamma = 100$ or 25) on bottom to assure good isolation. In the following levels the conductivity is increased by increasing the Si-content ($\gamma = 10$) to finish with a top level having further increased conductivity ($\gamma = 5$ or 2). A nanostructure ($\gamma = 25 \rightarrow 10 \rightarrow 5 \rightarrow 2$) with continuous variation of the properties is shown in Fig. 1.

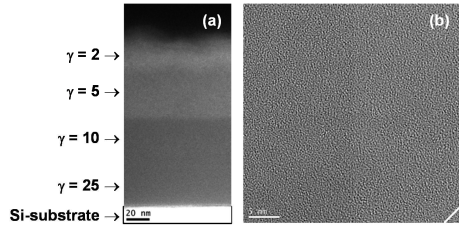


Fig. 1. TEM images of $\text{SiO}_x\text{N}_y\text{:H}$ nanostructured layer with continuous variation of its properties ($\gamma = 25 \rightarrow 10 \rightarrow 5 \rightarrow 2$): (a) Energy Filtered TEM image in XS-view, and (b) High Resolution TEM image in XS-view.

The evolution with charging time of the integrated intensity of potential profiles for bias voltage of 25 V as performed in the KFM study is shown in Fig. 2a for mono-layers with different γ -values and for two nanostructured layers with continuous levels $\gamma = 100 \rightarrow 25 \rightarrow 10 \rightarrow 5$ and $\gamma = 100, 25 \rightarrow 10 \rightarrow 5 \rightarrow 2$, called grad5 and grad2. The small integrated intensity (I_s) for the highly insulating layers ($\gamma = 100$ and 25) is related to low density of injected charges. The Si-rich layers ($\gamma = 5$ and 2) also exhibit small integrated intensity with saturation effect due to increased charge transport in depth of the layer, as well as transversally (the FWHM is doubled). The intermediate layer ($\gamma = 10$) presents very strong increase of the integrated intensity and fast surface charge diffusion. The two nanostructured layers combine the properties of the constituent layers and behave like insulating layers in terms of charge saturation effect, and like Si-rich layers in terms of charge transport in the volume, however governed by the properties of the intermediate layers with strong surface diffusion.

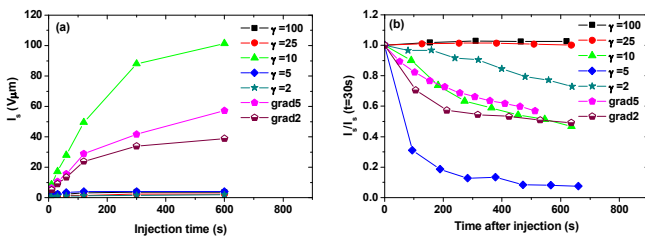


Fig. 2. Evolution of (a) the integrated intensity, I_s for 25 V bias on the AFM tip, and (b) the I_s normalized to its value at 30 s after injection (technological time to start measurements). Charge injection for 5 min at 25 V.

The charge decay mechanisms are also classified according to the layer composition (Fig. 2b). The nanostructured layers follow the decay of intermediate layer revealing simultaneous

action of surface and volume charge transport, however modulated by the presence of other levels in the nanostructure.

Combined effect of increased dielectric constant, by increasing the Si-content in the layer, with fast charge decay in the nanostructured layers qualifies them as appropriate for application in capacitive RF MEMS switches.

B. Silica layers with tailored interfaces

Tailoring the properties of a SiO_2 layer is achieved by embedding a single layer of AgNPs (below the percolation threshold) at the vicinity of the dielectric free surface (Fig. 3). The AgNPs are thought to play the role of deep trapping centers thereby stabilizing the charge injection due to the field reduction at the electrode when the AgNPs are charged.

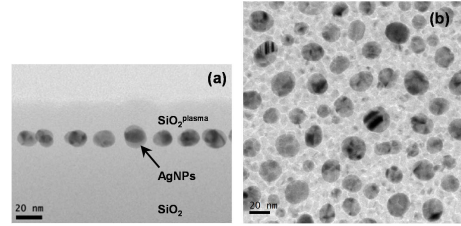


Fig. 3. Bright field TEM images of SiO_2 layers with tailored interfaces: (a) XS-TEM image and (b) PV-TEM image.

Two types of plasma deposits are tested as cover layers: silica (SiO_2) and organosilicon ($\text{SiO}_x\text{C}_y\text{:H}$). KFM measurements of the potential profile induced by charge injection reveal strong lateral charge spreading for the nanostructure with AgNPs covered by $\text{SiO}_x\text{C}_y\text{:H}$ layer.

IV. CONCLUSION

Dielectric engineering of thin dielectric layers is applied to establish a new class of nanostructures preventing electrostatic charging. The obtained results show that strong gradual variation of the conductive properties across the nanostructured dielectrics provides efficient charge transport in depth of the structure and reduces the electric field at the surface, decreasing in that way the density of injected charges. The presented nanostructured layers appear quite promising for application in RF MEMS capacitive switches.

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