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Impact of the gate and insulator geometrical model on the static performance and variability of ultra-scaled silicon nanowire FETs

Demetrio Logoteta, Nicolas Cavassilas, Alessandro Cresti, Marco G. Pala, *Member IEEE*, Marc Bescond

***Abstract*—We investigate the effect of the geometrical model adopted for the gate electrode and for the insulator envelopping the access regions on the full-quantum simulation of ultra-scaled nanowire field-effect transistors (NW-FETs). We compare the results obtained in the 'minimal' geometry commonly used in simulations with those obtained in a more realistic one, able to fully account for the gate fringing effects. We evaluate the impact of the model geometry on the static performance of NW-FETs, and discuss the interplay with the surface roughness and the random distribution of dopants. We find that the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio evaluated in the minimal geometry can be remarkably underestimated in short devices, notably in the case of small length-to-width ratio. The roughness-induced current degradation and the sensitivity to the surface roughness variability can also suffer from non-negligible underestimations when evaluated in this geometry. Finally, we point out that an inaccurate description of the device electrostatics is expected to result in an overestimation of the sensitivity to the doping-induced variability.**

***Index Terms*—nanowires, fringe field, non-equilibrium Green's function, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio, surface roughness, doping induced variability.**

I. Introduction

INTEGRATED electronic devices and prototypes in experimental setups are commonly deeply buried into insulating layers and contacted by means of gate electrodes several tens of nanometers thick. Notwithstanding, the geometries routinely considered for the numerical quantum simulation of nanoelectronic devices assume for the insulator enrobbing the device access regions a quite small thickness with respect to the decay length of the electric field (usually the same thickness as the gate oxide) and model the gate with thickless stripes. This prevents any account for the outer fringe field originating from the gate sidewalls [1]. More realistic geometries are systematically considered only in the framework of simpler transport models, in order to provide semianalytical descriptions of parasitics [1], [2], [3] or perform extensive explorations of the design parameter space [4], [5], [6], [7]. Here, we propose a full-quantum simulation study focusing on the static characteristics of gate-all-around ultra-scaled silicon NW-FETs, aimed to investigate the impact of extending the simulation domain so as to include a larger part of the gate electrode and of the insulator enveloping the source and drain extensions. Throughout the paper, we assess this impact in connection with some of the main tasks the numerical simulation of electronic devices is supposed to accomplish: the prediction of the upper performance bounds of devices, the estimation of their change in the presence of non-idealities, and the evaluation of their sensitivity to the sources of variability. We proceed by carrying out a systematic comparison of the results obtained for NW-FETs of different width and/or gate length within two different model geometries, which feature a different thickness of the gate and the insulator enrobbing the device. The deviations are quantified in terms of the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio, which we assume as a representative figure of merit. Besides considering perfect devices, we also discuss the modifications of the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio in the presence of surface roughness and its sensitivity to the disorder induced by surface roughness or random distribution of dopants. These latter are expected to be the dominant sources of variability for NW-FETs and have a stronger impact in ultra-scaled devices because of the weaker self-averaging effects.

The paper is organized as follows. Section II illustrates the physical models and the simulation techniques; Section III presents the main results: subsection III-A focuses on the evaluation of I_{ON} in perfect NW-FETs; subsection III-B treats the current degradation induced by the surface roughness; in subsection III-C, we discuss the device sensitivity to the variability induced by surface roughness and doping. Finally, in Section IV we draw our concluding remarks.

II. Model

We consider square gate-all-around unstrained silicon NW-FETs along the [100] orientation. The dielectric constant of the gate insulator is set to 3.9 (SiO_2) and its thickness to $t_{\mathrm{ox}} = 1$ nm. This choice is aimed at simplifying as much as possible the device structure and make the interpretation of the simulation results easier. Replacing the SiO_2 layer with a more realistic, equivalent high-k stack is expected to negligibly change the device electrostatic, particularly the gate fringe field. However, a single SiO_2 layer of the considered thickness could entail a significant gate leakage current. This current could mask some of the effects emerging in the subthreshold regime of the devices and make difficult the extension of the resulting physical picture to NW-FETs with more opaque gate

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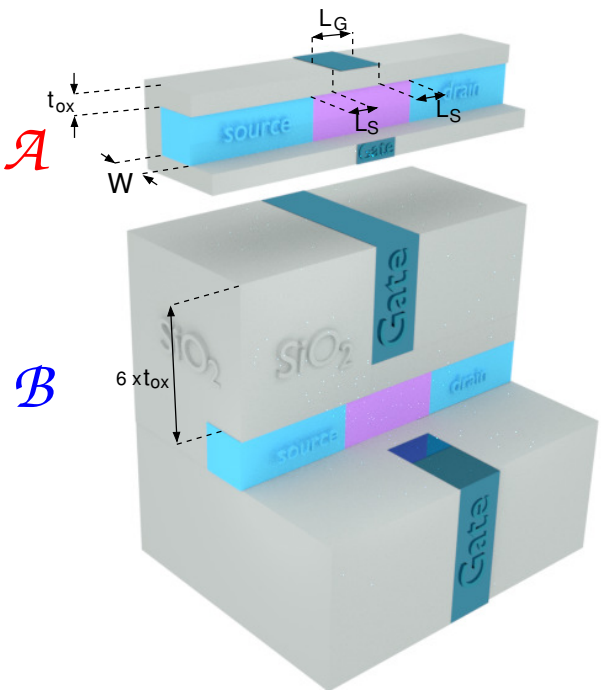

Fig. 1. Sketch of the simulated NW-FETs, modeled according to the minimal geometry $\mathcal{A}$ and the more realistic geometry $\mathcal{B}$.

insulators. In light of this, the leakage current is not taken into account in our simulations.

The geometries compared in this study are sketched in Fig. 1. The minimal geometry $\mathcal{A}$ is the simplest and most commonly used one. The gate corresponds in it to a wrapping surface belonging to the boundary of the simulation domain. For a given size of the nanowire and gate oxide thickness, it is the rectangular parallelepiped geometry enclosing the minimum volume. On the other hand, the geometry $\mathcal{B}$ models the gate as a three-dimensional shell. The value of 5 nm set for its thickness has been verified to guarantee a reasonable stabilization of the results against any further increase. In both the $\mathcal{A}$ and $\mathcal{B}$ geometries, the spacer insulator is SiO_2. This choice has been recently suggested as a better option to limit the increase of the switching delay as the gate length is scaled down to 10 nm [8]. In order to further simplify the device structure, SiO_2 was also set as the insulator enveloping the access regions of the devices, since the value of its dielectric constant is not far from the one of the commonly employed interlayer dielectrics.

In order to investigate the interplay with different degrees of quantum confinement and short channel effects, we considered devices with two different transversal cross-sections W^2 (2×2 and 5×5 nm^2), gate lengths L_G (5 and 10 nm) and gate underlaps L_S (0 and 3 nm). The source and drain extensions are assumed 12 nm long and continously n-doped with concentration $N_D = 10^{20}$ cm^{-3}, unless otherwise stated. Following the projections of the International Technology Roadmap for Semiconductors 2015 for low power devices at the 2021/2024 technological nodes [9], throughout the paper we assume a source-drain bias of $V_{DS} = 0.6$ V and we set the nominal OFF current to $I_{OFF} = 10^{-4}$ μA/μm, unless

TABLE I
PERCENTAGE INCREASE OF THE I_{ON}/I_{OFF} RATIO IN THE $\mathcal{B}$ GEOMETRY WITH RESPECT TO THE $\mathcal{A}$ ONE IN THE BALLISTIC (BAL) AND DISSIPATIVE (PHON) REGIME. I_{OFF} IS SET TO 10^{-4} μA/μm.

	$L_S = 3$ nm				$L_S = 0$ nm	
	$L_G = 5$ nm		$L_G = 10$ nm		$L_G = 5$ nm	$L_G = 10$ nm
	BAL	PHON	BAL	PHON	PHON	PHON
$W = 2$ nm	53%	28%	26%	10%	26%	6%
$W = 5$ nm	122%	117%	21%	20%	516%	13%

otherwise stated. The current in the ON state is computed as $I_{ON} = I_{DS}(V_{GS}^{(off)} + V_{DS})$, where $V_{GS}^{(off)}$ denotes the gate voltage V_{GS} in the OFF state. All the values of current provided in the paper are normalized to the width of the nanowires.

Our simulation methodology is based on the self-consistent solution through a fixed point iteration algorithm of the transport equations within the non-equilibrium Green's function formalism and of the Poisson equation. A comprehensive illustration of this approach can be found in Ref. [10]. To describe the system, we assumed an effective mass Hamiltonian, calibrated on tight-binding band structure computations [11]. This approximation is able to provide an accurate description of transport in silicon nanowires with the considered crystallographic orientation [12]. The nanowires with a 2×2 nm^2 transversal cross-section have been simulated in the real-space basis corresponding to a seven-point stencil central finite difference discretization. For the nanowires with $W = 5$ nm a coupled mode-space approach has been resorted, in order to limit the otherwise unmanageable computational burden. Electron-phonon scattering was included within the self-consistent Born approximation. Acoustic and optical phonons were modeled in the elastic and dispersionless approximation, respectively, by assuming the self-energy expressions and the deformation potentials in Ref. [13].

The surface roughness at the interface between silicon and SiO_2 was included nonperturbatively by introducing random fluctuations in the oxide thickness, according to the metodology detailed in Ref. [14]. The surface fluctuations $\Delta(\boldsymbol{r})$ have been generated by assuming an exponential autocorrelation function $\langle \Delta(\boldsymbol{r})\Delta(\boldsymbol{r'} - \boldsymbol{r})\rangle = \Delta_m^2 e^{-\sqrt{2}r/L_m}$, where Δ_m is the root mean square (rms) value of the fluctuations and L_m their correlation length.

Ionized discrete donors have been modeled as positive elementary point charges. Central cell corrections, depending on the particular chemical species considered and expected to be small for shallow dopants [15], have been neglected. In order to take into account the substitutional position of dopants, a hard sphere model has been resorted, where individual dopants have been considered at the center of non-overlapping spheres with radius 1 nm. The screening by the mobile charge is automatically taken into account within the Hartree approximation through the self-consistent coupling with the Poisson equation.

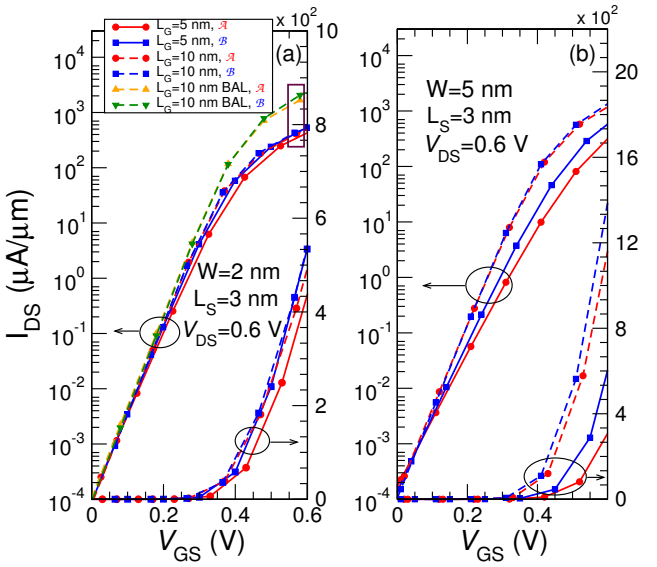

Fig. 2. Transfer characteristics of the NW-FETs with $L_{\rm S} = 3$ nm, simulated with the $\mathcal{A}$ and the $\mathcal{B}$ geometry. (a) $W = 2$ nm; (b) $W = 5$ nm. All the curves have been shifted in order to set $I_{\rm DS} = I_{\rm OFF}$ at $V_{\rm GS} = 0$ V. The abbreviation 'BAL' in the legends indicates that the corresponding curves refer to the ballistic regime.

III. Results and Discussion

A. ON current in perfect NW-FETs

Fig. 2 and Fig. 3 show the transfer characteristics for the NW-FETs with $L_S = 3$ nm and $L_S = 0$, respectively, in the $\mathcal{A}$ and $\mathcal{B}$ geometry. All the curves are shifted in order to set $I_{\rm DS} = I_{\rm OFF}$ at $V_{GS} = 0$ V. Table I summarizes the percentage increase of the $I_{\rm ON}/I_{\rm OFF}$ ratio in $\mathcal{B}$ with respect to $\mathcal{A}$. It turns out that the $I_{\rm ON}$ is always higher in $\mathcal{B}$, by an amount depending on the particular configuration considered. The largest variations are obtained for the devices with $W = 5$ nm and $L_G = 5$ nm, for which the ON current can

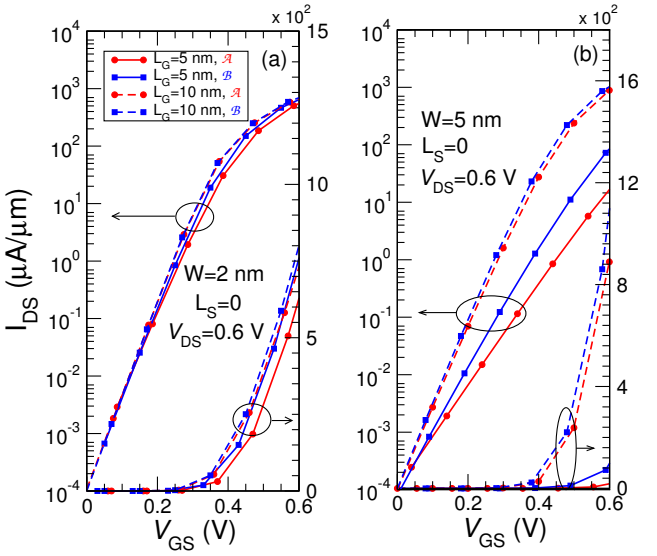

Fig. 3. Transfer characteristics of the NW-FETs with $L_{\rm S} = 0$ nm, simulated with the $\mathcal{A}$ and the $\mathcal{B}$ geometry. (a) $W = 2$ nm; (b) $W = 5$ nm. All the curves have been shifted in order to set $I_{\rm DS} = I_{\rm OFF}$ at $V_{\rm GS} = 0$ V.

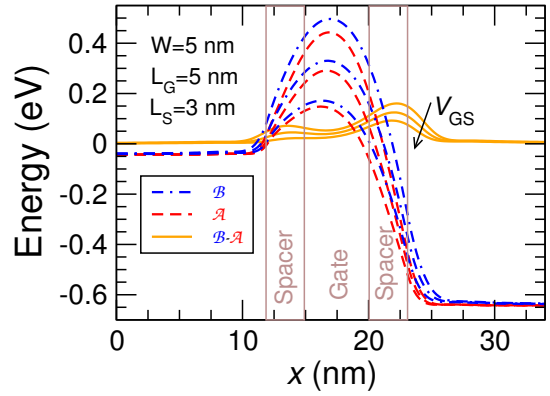

Fig. 4. Lowest subbands of the NW-FET with $W = 5$ nm, $L_{\rm G} = 10$ nm and $L_{\rm S} = 3$ nm for three different gate voltages, simulated by using the $\mathcal{A}$ and the $\mathcal{B}$ geometry (dashed and dot-dashed lines, respectively). The continous lines represent the difference between two subbands in the $\mathcal{A}$ and the $\mathcal{B}$ geometry corresponding to the same $V_{\rm GS}$ value.

double ($L_S = 3$ nm) or even increase several times ($L_S = 0$). According to Fig. 2 and Fig. 3, this behavior is due to the significant subthreshold swing degradation in $\mathcal{A}$ with respect to $\mathcal{B}$. More insight can be gained from Fig. 4, showing the lowest conduction subband in the NW-FET with W =5 nm, $L_{\rm G} = 5$ nm and $L_{\rm S} = 3$ nm. The plot highlights that for a given $V_{\rm GS}$ the source-to-drain barrier is wider and higher in $\mathcal{B}$, which can be interpreted as due to an increase of the effective gate length with respect to $\mathcal{A}$. This behavior can be traced back to the different extent by which the geometries account for the gate fringe field. Geometry $\mathcal{B}$ is able to fully account for it (inner fringe and outer fringe from the gate sidewalls [1]), while geometry $\mathcal{A}$ can only take into account the inner fringe. This is further illustrated in Fig. 4 by the plot of the difference between the subbands obtained in $\mathcal{A}$ and $\mathcal{B}$ corresponding to the same $V_{\rm GS}$: the difference peaks in the source and drain spacers, where the fringe field is more intense, and decreases as $V_{\rm GS}$ increases, due to the enhancement of the gate screening with the increment of the mobile charge. Analogously to the case in which the effective gate length is intentionally increased through the inclusion of gate underlaps [16], this effect entails an increase of the control over the height of the barrier and a suppression of the tunneling current in the subthreshold region, thus resulting in an improved subthreshold swing in the $\mathcal{B}$ geometry. The relative improvement is higher for the devices with larger W, shorter gate length and no spacers, since they exhibit a poorer electrostatic integrity and the relative impact of an increase of the effective gate length is stronger.

We point out that the discrepancies between the value of the $I_{\rm ON}/I_{\rm OFF}$ ratio evaluated in the $\mathcal{A}$ and $\mathcal{B}$ geometry can strongly depend on the electron-phonon coupling strength. The percentage increase of the $I_{\rm ON}/I_{\rm OFF}$ ratio in the ballistic regime is reported in Table I for the NW-FETs with $L_S = 3$ nm. The comparison with the values obtained in the presence of electron-phonon scattering indicates that the deviations between $\mathcal{A}$ and $\mathcal{B}$ are always larger in the ballistic regime, in particular for the narrower NW-FETs. As can be checked in Table I by comparing the cases $L_{\rm G} = 5$ nm and

10 nm, the magnitude of the effect is weakly dependent on the gate length, which suggests that it can be traced back to a different modulation of the potential at large gate overdrives. In order to gain more insights, the lowest conduction subbands on the source side corresponding to the transfer characteristic data points enclosed by a rectangle in Fig. 2, are compared in Fig. 5. In both the ballistic and dissipative case, switching from $\mathcal{A}$ to $\mathcal{B}$ geometry entails a decrease of the potential barrier in the source spacer, which is directly modulated by the fringe field. On the other hand, while in the ballistic case electrons are mainly injected from the source contact at the base of the barrier, in the presence of phonons electrons are injected over its top, due to the linear bending of the subband (see maps in Fig. 5). Only a fraction of them hit the barrier due to the incomplete energy relaxation in the source. As a results, the modification of the barrier in $\mathcal{B}$ with respect to $\mathcal{A}$ at large gate overdrives affects more the ballistic current than its dissipative counterpart. A similar behavior is found for the NW-FETs with $W = 2$ nm and $L_{\rm S} = 0$ (not shown). In wider devices, the modulation of the barrier at large gate overdrives is less influenced by the gate fringe field, and similar percentage increases of the $I_{\rm ON}/I_{\rm OFF}$ ratio in $\mathcal{B}$ with respect to $\mathcal{A}$ are found in the ballistic regime and in the presence of electron-phonon scattering (cf. the values for $W = 5$ nm in Table I). This is a consequence of the lower resistance of the source extension, which results in a smaller bending of the subbands, and of the weaker effectiveness of the fringe field in modulating the potential over the whole transversal cross-section of the nanowire.

B. Surface roughness-induced current degradation

We limit our analysis to NW-FETs with $W = 5$ nm. In NW-FETs with $W = 2$ nm typical rms values for the surface roughness result in considerably larger subband fluctuations, entailing a stronger dependence of the transfer characteristics on the particular roughness realization. In these conditions a full statistical study is required in order to extract clear trends.

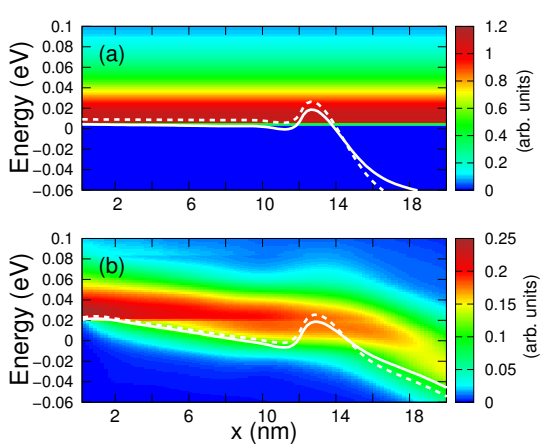

Fig. 5. Current spectrum on the source side for NW-FETs with $W = 2$ nm, $L_{\rm G} = 10$ nm and $L_{\rm S} = 3$ nm simulated with the $\mathcal{B}$ geometry in (a) the ballistic regime and (b) in the presence of electron-phonon scattering. The continuous curves represent the corresponding lowest subband, while the dashed ones refer to the lowest subband obtained in the $\mathcal{A}$ geometry. The maps and the curves refer to the points enclosed by a rectangle in Fig. 2

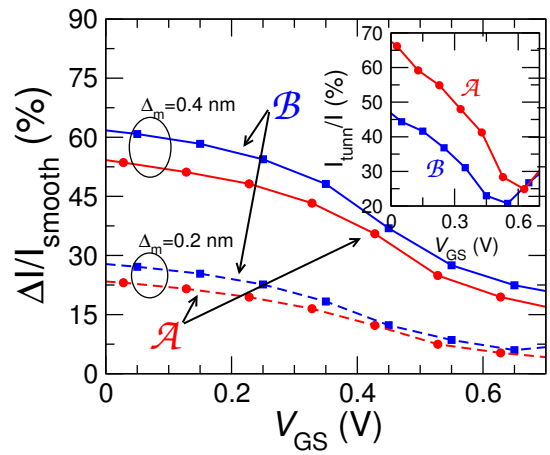

Fig. 6. Percentage decrease of the current as a function of $V_{\rm GS}$ in the presence of surface roughness with respect to the current in the smooth device. The NW-FET has $W = 5$ nm, $L_{\rm G} = 5$ nm and $L_{\rm S} = 3$ nm. Two different rms values of the oxide thickness fluctuations $\Delta_{\rm m}$ =0.2 and 0.4 nm are considered. The correlation length is $L_{\rm m} = 1$ nm. *Inset*: percentage of tunneling current as a function of $V_{\rm GS}$ in the rough NW-FET with $\Delta_{\rm m} = 0.4$ nm.

Fig. 6 illustrates the percentage degradation of the current as a function of $V_{\rm GS}$ for NW-FETs with $L_{\rm G} = 5$ nm and $L_{\rm S} = 3$ nm and for rms values of 0.2 and 0.4 nm. In order to make the comparison meaningful, the same realization of the surface roughness has been used for $\mathcal{A}$ and $\mathcal{B}$. The plots clearly show a larger current degradation in $\mathcal{B}$, which reduces as $V_{\rm GS}$ increases. We discuss first the low-$V_{\rm GS}$ behavior. At low gate voltages only few low-energy modes contribute to transport [17]. Due to the presence of a large potential barrier in the channel, in the source extension the transport *via* these modes takes place at higher energies with respect to the bottom of the corresponding subbands and is thus only weakly affected by the subband fluctuations induced by the surface roughness. The roughness influences the transport mainly in the channel region, by affecting the shape and the height of the barrier. On the other hand, as already mentioned in Sec. III-A and quantified in the inset of Fig. 6, the source-drain tunneling is overestimated in the $\mathcal{A}$ geometry. The tunnel component of the current at low enough energies is weakly sensitive to the details of the top of the barrier and thus, in the considered situation, to the fluctuations induced by the roughness. Therefore, the overestimation of tunneling finally results in an underestimation of the scattering and, as a consequence, of the current degradation in $\mathcal{A}$ with respect to $\mathcal{B}$. The weak sensitivity of the low-energy tunneling current to the potential fluctuations can be understood by referring to the Wentzel-Kramers-Brillouin (WKB) approximation for the transmission through a barrier defined by a potential $U(x) = U_0(x) + \delta U(x)$, where U_0 is the smooth potential and $\delta U(x)$ the potential fluctuations due to the roughness. The transmission T as a function of the energy E reads $T(E) \sim e^{-(2/\hbar)\int\sqrt{2m^*(E-U(x))}dx}$, where $\hbar$ is the reduced Plank constant, m^* is the effective mass in the transport direction and the integral is computed between the classical turning points. To the first order in the fluctuations $\delta U(x)$, the variation of the action integral is $\delta\int\sqrt{2m^*(U(x)-E)}dx \propto \int\frac{\delta U(x)}{\sqrt{(U_0(x)-E)}}dx$. This shows

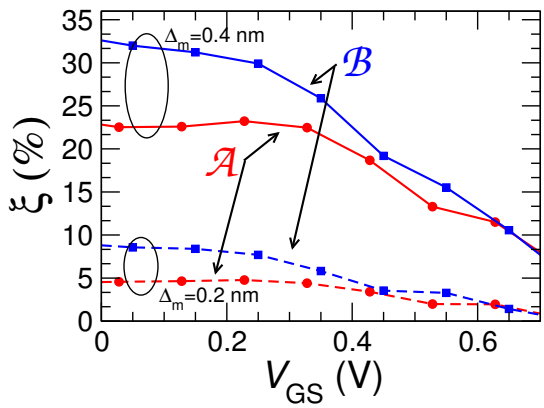

Fig. 7. Deviation of the current with respect to the average $\xi = |I_{\rm DS}^{(2)} - I_{\rm DS}^{(1)}|/\langle I_{\rm DS}\rangle$ for a set $\{1,2\}$ of two different realizations of the surface roughness. Two different rms values of the oxide thickness fluctuations $\Delta_{\rm m}$ =0.2 and 0.4 nm are considered. $L_{\rm m} = 1$ nm. $W = 5$ nm, $L_{\rm G} = 5$ nm and $L_{\rm S} = 3$ nm.

that the influence of a perturbation $\delta U(x)$ on the transmission tends to become negligible as E decreases with respect to the top of the barrier.

As $V_{\rm GS}$ increases, the discrepancies between the $\mathcal{A}$ and $\mathcal{B}$ case reduce. This originates from the concomintant decrease of the percentage of tunneling and of the difference of this percentage between $\mathcal{A}$ and $\mathcal{B}$ (see the inset of Fig. 6). Moreover, as the components of the current spectrum close to the bottom of the subbands increase due to the lowering of the barrier, also the surface roughness in the source and drain extension starts to contribute to the back scattering, thus reducing the relative importance of the fluctuations in the channel. The deviations in the current degradation entails the emergence of deviations in terms of the $I_{\rm ON}/I_{\rm OFF}$ ratio. Since, according to the previous discussion, $I_{\rm OFF}$ in rough devices is degraded more than $I_{\rm ON}$, it turns out that the $I_{\rm ON}/I_{\rm OFF}$ ratio is enhanced by the surface roughness (both in $\mathcal{A}$ and $\mathcal{B}$). For $\Delta_m = 0.4$ nm, we find for the relative variation of the $I_{\rm ON}/I_{\rm OFF}$ ratio with respect to the smooth case $|\Delta(I_{\rm ON}/I_{\rm OFF})|/(I_{\rm ON}/I_{\rm OFF})_{\rm smooth} = 72\%$ in $\mathcal{A}$, while it appreciably increases to 96% in $\mathcal{B}$.

For longer gates (not shown), the difference in the current degradation between $\mathcal{A}$ and $\mathcal{B}$ decreases due to the suppression of the tunneling.

C. Device sensitivity to the sources of variability

In this section we consider the modifications of the NW-FET transfer characteristics induced by a change of the surface roughness realization or of the dopant distribution. The purpose is not to assess the variability ranges, which would require a full statistical study, but only to qualitatively investigate how the sensitivity predicted for the devices changes when switching from the $\mathcal{A}$ to the $\mathcal{B}$ geometry.

1) Surface roughness-induced variability: In order to address the impact of the model geometry on the sensitivity to the surface roughness variability, an ensemble $\{1,2\}$ of two different realizations (the same for $\mathcal{A}$ and $\mathcal{B}$) has been considered. The relative deviation of the current $\xi = |I_{\rm DS}^{(2)} - I_{\rm DS}^{(1)}|/\langle I_{\rm DS}\rangle$ with respect to the average $\langle I_{\rm DS}\rangle = (I_{\rm DS}^{(2)} + I_{\rm DS}^{(1)})/2$ is taken as a measure of the sensitivity. ξ is plotted in Fig. 7 for NW-FETs with $W = 5$ nm, $L_{\rm G} = 5$ nm and $L_{\rm S} = 3$ nm. A $V_{\rm GS}$ dependence qualitatively similar to the one associated to the current degradation in Fig. 6 is found, with a clear enhancement of ξ in $\mathcal{B}$ with respect to $\mathcal{A}$. This translates to a different sensitivity of the OFF current and thus of the $I_{\rm ON}/I_{\rm OFF}$ ratio. By defining the relative deviation of the $I_{\rm ON}/I_{\rm OFF}$ ratio with respect to the average as

$$\xi_{I_{\rm ON}/I_{\rm OFF}} = \left| \left(\frac{I_{\rm ON}^{(2)}}{I_{\rm OFF}^{(2)}}\right) - \left(\frac{I_{\rm ON}^{(1)}}{I_{\rm OFF}^{(1)}}\right) \right| \Big/ \left\langle \frac{I_{\rm ON}}{I_{\rm OFF}} \right\rangle, \quad (1)$$

we find $\xi^{(\mathcal{A})}_{I_{\rm ON}/I_{\rm OFF}} = 2.6\%$ and $\xi^{(\mathcal{A})}_{I_{\rm ON}/I_{\rm OFF}} = 11\%$, for rms=0.2 nm and 0.4 nm, respectively. The corresponding values in $\mathcal{B}$, 6.4% and 20%, increase by almost a factor 2.

As for the current degradation in the previous subsection, the origin of the discrepancies in Fig. 7 can be traced back to the overestimation of the tunneling in the geometry $\mathcal{A}$. Indeed, in the previous subsection we have pointed out that the roughness has a weaker impact on the current in $\mathcal{A}$. This directly entails a smaller sensitivity of the current to the change of the roughness realization with respect to $\mathcal{B}$. On the other hand, by referring again to the WKB approximation for the tunneling transmission, we can write $T(E) \sim e^{-(2/\hbar)\int\sqrt{2m^*(U(x)-E)}dx} = e^{-(\sqrt{8m^*}/\hbar)\Delta x\left\langle\sqrt{(U(x)-E)}\right\rangle_x}$, where Δx is the width of the barrier at the energy E and $\langle f(x)\rangle_x$ denotes the average of $f(x)$ over Δx. The rearranged expression for T indicates that the tunneling current tends to experience the potential in an averaged way, or, in the examined situation, that the tunneling current can be approximately considered modulated by the potential averaged over the roughness fluctuations, instead than by the actual rough potential. This further contributes to decrease the current sensitivity to the roughness in $\mathcal{A}$ with respect to $\mathcal{B}$. The dependence of the sensitivity on V_{GS} in Fig. 7 is qualitatively similar to the one of the current degradation in Fig. 6, and the same considerations made in the previous subsection apply.

2) Doping-induced variability: We consider NW-FETs with $L_{\rm S} = 0$ and the structure sketched in Fig. 8, including on the source and drain side a 6 nm long region where the continous doping is replaced with a distribution of positive point charges modeling ionized dopants. The number of charges has been set equal to the average number of discrete dopants in the considered volume region according to the doping concentration $N_{\rm D}$. While this approach entails an unphysical interface between the continuously doped region and the one including discrete dopants, it guarantees that the (screened) Coulombic tails of the dopant potential extending toward the source and drain contacts are fully taken into account. An alternative approach to model disordered contacts can be found in Ref. [18]. We considered two representative arrangements of dopants, differing in the average distance of the dopants from the gated region. Since the dopants close to the channel are very effective in lowering and thinning the source-to-drain barrier, this distance is expected to be one of the dominant parameters determining the dispersion of the transfer characteristics [19]. The transverse y and z coordinate of each

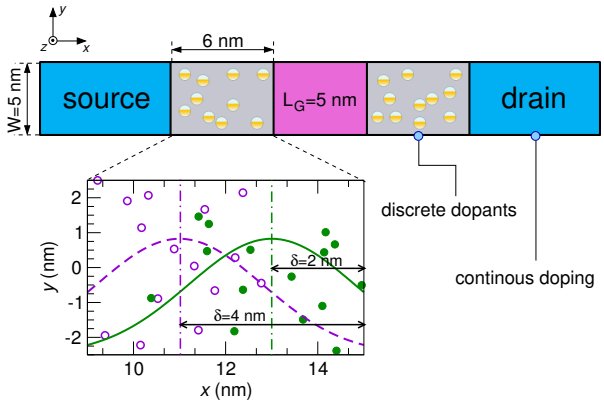

Fig. 8. Structure of the nanowires considered for the study of the doping variability. The empty and filled circles of the plot correspond to the projection on the $x-y$ plane of the two distributions of discrete dopants considered in the source extension of the NW-FET with $W = 5$ nm. Empty circles have a Gaussian probability density of their x coordinate (dashed curve, not normalized) centered at a distance $\delta = 4$ nm from the gated region; in the case of the filled circles the probability density (continue curve) is shifted of 2 nm in the direction of the gate. The y and z coordinates of the dopants are extracted for both distributions according to a uniform probability density.

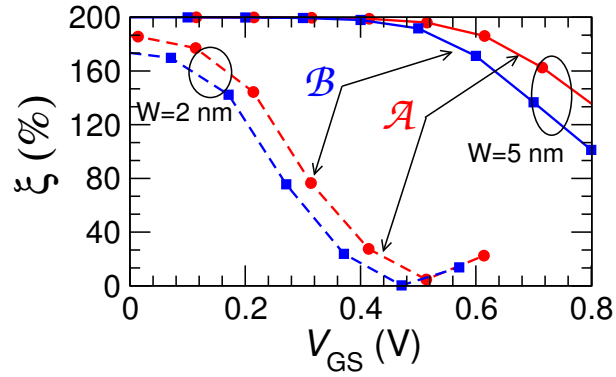

Fig. 9. Deviation of the current with respect to the average $\xi = |I_{\rm DS}^{\rm (C)} - I_{\rm DS}^{\rm (F)}|/\langle I_{\rm DS}\rangle$ for a set $\{\rm C, F\}$ of two different distributions of discrete dopants. $W = 2$ and 5 nm, $L_{\rm G} = 5$ nm.

point charge have been independently extracted assuming a uniform probability distribution over the silicon transversal cross-section. The x coordinate of the charges follows instead a Gaussian distribution. The two different arrangements of dopants correspond to different choices for the mean of the Gaussian probability density, namely for the x coordinate $x_{\rm bar}$ of the barycenter of the charge distribution. For one of the arrangement, which we will denote by 'F' (Far), $x_{\rm bar}$ is 4 nm far from the gated region, both on the source and the drain side, while it is 2 nm far for the other, which we will denote by 'C' (Close). Analogously to the case of rough devices in the previous subsection, we computed the transfer characteristics with the two dopant arrangements both in the $\mathcal{A}$ and the $\mathcal{B}$ geometry and we then extracted the relative deviation of the current with respect to the average $\xi = |I_{\rm DS}^{\rm (F)} - I_{\rm DS}^{\rm (C)}|/\langle I_{\rm DS}\rangle$ as a function of $V_{\rm GS}$. For transfer characteristics obtained in the same geometry a common reference is set by shifting them so that $(I_{\rm DS}^{(F)} + I_{\rm DS}^{(C)})/2 = I_{\rm OFF} = 10^{-1}$ μA/μm at $V_{\rm GS} = 0$. Note that here we set a larger value of $I_{\rm OFF}$ because for the considered dopant arrangements the deviations between $\mathcal{A}$ and $\mathcal{B}$ emerge, in terms of ξ, only at large enough gate overdrives. Indeed, in the devices with the dopant distributions closer to the gate, the subthreshold swing is strongly degraded and, in the subthreshold region, $I_{\rm DS}^{(F)} \gg I_{\rm DS}^{(C)}$ and thus $\xi^{(\mathcal{A})} \approx \xi^{(\mathcal{B})} \approx 200\%$.

Fig. 9 shows the plot of ξ in the geometry $\mathcal{A}$ and $\mathcal{B}$ for NW-FETs with $W = 5$ nm and $W = 2$ nm. The sensitivity appears always overestimated in $\mathcal{A}$. This discrepancy originates from the antagonistic effect of the gate fringe fields, partially counterbalancing the differences in the electrostatic potential due to the different distribution of the dopants. Indeed, while the positive dopants close to the gate tend to thin and lower the potential barrier, the gate fringe field tends to widen and lift it. This interplay finally results in a weaker sensitivity of the self-consistent potential in the channel to the distribution of dopants, translating to a smaller sensitivity of the transfer characteristics. Since the gate fringe field gradually decreases far from the gate just as the effect of a dopant on the barrier decreases as it is moved apart toward the source or drain contact, this behavior can be interpreted as a disorder regularization promoted by the fringe field and tending to level out the influence of the dopants at different positions. Finally, we report the deviations in terms of $\xi_{I_{\rm ON}/I_{\rm OFF}}$, for which a definition analog to Eq. 1 is assumed. Despite the differences in the current at large gate overdrives visible in Fig. 9, no sensible deviations are found for the wider NW-FETs because, since $I_{\rm OFF}^{\rm (F)} \ll I_{\rm OFF}^{\rm (C)}$, then $I_{\rm ON}^{\rm (F)}/I_{\rm OFF}^{\rm (F)} \gg I_{\rm ON}^{\rm (C)}/I_{\rm OFF}^{\rm (C)}$ and $\xi^{(\mathcal{A})}_{I_{\rm ON}/I_{\rm OFF}} \approx \xi^{(\mathcal{B})}_{I_{\rm ON}/I_{\rm OFF}} \approx 200\%$. For the narrower NW-FETs the degradation of the subthreshold swing in the 'C' case is weaker and we find $\xi^{(\mathcal{A})}_{I_{\rm ON}/I_{\rm OFF}} \approx 116\%$ and $\xi^{(\mathcal{B})}_{I_{\rm ON}/I_{\rm OFF}} \approx 126\%$.

IV. Conclusion

We compared the results of full-quantum simulations of ultra-scaled silicon NW-FETs obtained in a geometry fully accounting for the gate fringe field with the corresponding obtained in a commonly used minimal geometry only partially accounting for them. The comparison was carried out in terms of the prediction of the upper bounds of the device static performances, of their change in the presence of surface roughness, and of their sensitivity to the variability induced by surface roughness and random distribution of dopants. Our results indicate that large underestimations of the $I_{\rm ON}/I_{\rm OFF}$ ratio can arise in the minimal geometry, especially for devices with high $W/L_{\rm G}$. The poor electrostatic integrity of these devices enhances, indeed, the relative importance of the effective gate length increase promoted by the outer fringe field. In conditions of weaker electron-phonon scattering (lower temperature or materials exhibiting a weaker electron-phonon coupling), this underestimation is expected to increase for very narrow NW-FETs due to the stronger sensitivity to the modulation of the barrier exerted by the fringe field at large gate overdrives. The current degradation and the sensitivity to the variability induced by the surface roughness at the channel-oxide interface are predicted to be non-negligibly

underestimated in the minimal geometry. This effect has been traced back to the overestimation of the tunnel component of the current, less affected by the scattering from the fluctuations of the electrostatic potential. Finally, we highlighted a fringe field-driven regularization effect on the disorder induced by the random distribution of dopants, entailing an overestimation of the sensitivity to the doping-induced variability when the fringe field is not fully taken into account.

This study helps clarifying the physical mechanisms governing the interplay between the gate fringe fields and the electron transport, and provides a guide to estimate the degree of approximation associated to different choices of the simulated geometry.

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