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### ► To cite this version:

V. Della Marca, J. Amouroux, G. Molas, J. Postel-Pellerin, F. Lalande, et al.. How to improve the silicon nanocrystal memory cell performances for low power applications. 2012 International Semiconductor Conference (CAS 2012), Oct 2012, Sinaia, Romania. 10.1109/SMICND.2012.6400686 . hal-01760587

**HAL Id: hal-01760587**

**<https://hal.science/hal-01760587>**

Submitted on 29 Jul 2020

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# HOW TO IMPROVE THE SILICON NANOCRYSTAL MEMORY CELL PERFORMANCES FOR LOW POWER APPLICATIONS

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**Abstract** - In this paper we propose to optimize the 1T silicon nanocrystal (Si-nc) memory cell in order to reduce the energy consumption for low power applications. Optimized Channel Hot Electron Injection (a 4.5V programming window is reached consuming 1nJ) and Fowler-Nordheim programming are analyzed and compared. The tunnel oxide thickness, Si-ncs area coverage and SiN silicon nanocrystals capping layer are adjusted to optimize the data retention and endurance criteria. We present for the first time the endurance characteristics of a Si-nc cell up to  $10^6$  cycles with a final programming window of 4V.

**Keywords:** Silicon nanocrystal memories; energy consumption; tunnel oxide thickness.

## 1. INTRODUCTION

The market of nonvolatile Flash memories for portable systems requires more and more low energy and high reliability solutions. The silicon nanocrystal Flash memory cell appears as one promising candidate for embedded applications due to its good reliability (resistance to SILC, no tail-bits) and ease of integration [1, 2]. The impact of the technological features on the memory performances was studied in the literature [3]. In order to reduce the operating voltages, the integration of high-k materials in the gate stack was also proposed [4, 5]. Other architectures like split-gate memories [6, 7] allow reducing the energy consumption of the memory, but require the addition of a select transistor, controlling the programming current.

In this context, the impact of the technological parameters (tunnel oxide thickness, SiN trapping layer, nanocrystal features) was not studied in details to find a good trade-off in order to improve the global cell performances for low power and high reliability applications. In this paper we focused on the impact of the tunnel oxide thickness during Channel Hot Electron Injection (CHEI) on energy consumption. In

alternative we propose to use the Si-nc cell in full Fowler-Nordheim (FN) regime, where the coupling factor plays an important role. In this scenario we studied the impact of the nanocrystal size and of the SiN capping layer to optimize the data retention and the endurance. Finally, for the first time to our knowledge, a 1M cycles endurance is shown for a Si-nc memory cell.

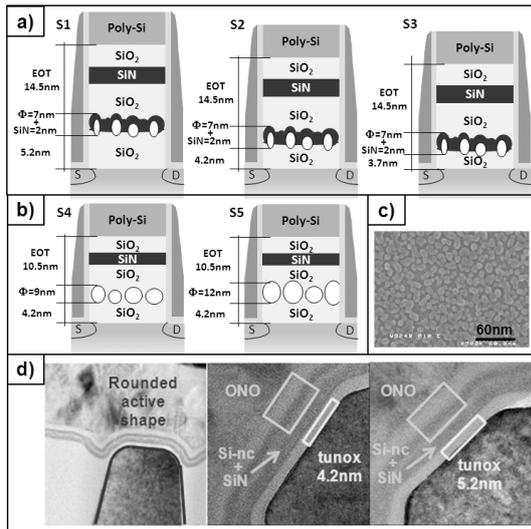
## 2. TECHNICAL DETAILS

The silicon nanocrystals are grown by Low Pressure Chemical Vapor Deposition (LPCVD) on the tunnel oxide top surface with a two-step process. During the first step, diffusion of silane ( $\text{SiH}_4$ ) on hydrophilic surface causes the germination phenomenon; while the second step is a selective growth with dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) diffusion [8]. Using this approach the density and diameter ( $\Phi$ ) of Si-nc can be independently controlled. The first increases with silane diffusion period and the second is controlled by the dichlorosilane diffusion period.

*Si-nc/SiN memories (samples S1 to S3)* - The Si-ncs ( $\Phi \sim 7\text{nm}$ , density =  $6 \cdot 10^{11}\text{cm}^{-2}$ ) were deposited on three tunnel oxide thicknesses (tunox): 3.7nm, 4.2nm and 5.2nm; and capped by a 2nm of SiN. Then, to complete the stack, the ONO (Oxide-Nitride-Oxide) Inter-Poly Dielectric (IPD) layer was deposited to reach 14.5nm of Equivalent Oxide Thickness (EOT) (Fig. 1a).

*Si-nc memories (sample S4 and S5)* - Si-ncs with two different diameters (S4:  $\Phi \sim 9\text{nm}$ , S5:  $\Phi \sim 12\text{nm}$ ; density =  $7.2 \cdot 10^{11}\text{cm}^{-2}$ ) were deposited on 4.2nm tunnel oxide. The EOT of the ONO IPD is 10.5nm thick in this case (Fig. 1b).

Fig. 1c-d presents Si-ncs Scanning Electron Microscopy (SEM) plan views and Transmission Electron Microscopy (TEM) cross section of memory cells.



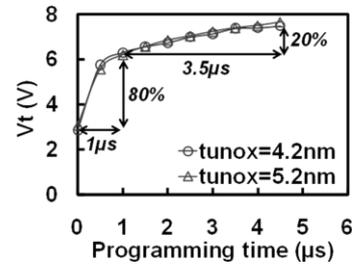
**Fig. 1.** a)-b) Schematics of memory devices studied in this work; c) SEM top view of silicon nanocrystal; d) TEM cross sections.

### 3. ELECTRICAL RESULTS

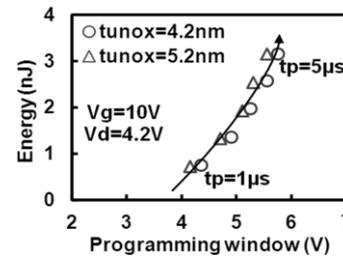
In the first part of this section we present some experimental results to explain the effect of tunnel oxide thickness ( $t_{\text{unox}}$ ) and programming time ( $t_p$ ) on cell performances during the CHEI programming. After this, in the second part, we propose the Si-nc cell optimization and demonstrate the importance of the coupling factor increasing [9] and the reliability issued induced by the SiN capping layer on the Si-ncs.

#### 3.1. Impact of tunnel oxide thickness

In Fig.2 we show the CHEI programming kinetics of Si-nc/SiN cell using two different tunnel oxide thicknesses (samples S1 and S2). The gate voltage ( $V_g$ ) is 9V while the drain voltage ( $V_d$ ) is 4.2V. The two samples have the same programming speed, which means that the hot carrier injection is independent on the tunnel oxide thickness. One can also notice that 80% of the charge is injected during the first programming microsecond, suitable for fast low power applications. To study the impact of tunnel oxide thickness on energy consumption the memory was programmed using box pulses of different durations (Fig. 3). The measurement setup and the computation method are presented in [10]. It appears that the tunnel oxide thickness has a limited influence on the energy and programming window. In particular to achieve a window of 4V,  $t_p=1\mu\text{s}$  is sufficient, consuming an energy lower than 1nJ.

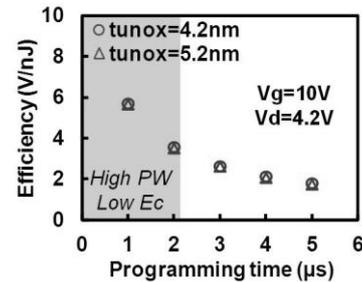


**Fig. 2.** The CHEI programming kinetics of Si-nc/SiN cell (S1 and S2), using two different tunnel oxide thicknesses.



**Fig. 3.** Consumed energy versus the programming window, for two tunnel oxide thicknesses (S1 and S2).

We defined the programming efficiency as the ratio between the programming window and the energy. Fig. 4 shows that the efficiency is higher using short pulses and is independent on the tunnel oxide thickness; what is consistent with the results presented above.



**Fig. 4** Efficiency versus the programming time for Si-nc/SiN cell.

In alternative to CHEI programming for low power application, FN can also be used, but the results of Fig. 5 show that long program/erase times are required to reach a sufficient programming window. To conclude this part, the impact of the tunnel oxide thickness on data retention at 150°C is reported in Fig. 6. The charge loss increases decreasing the tunnel oxide thickness. To achieve the specification of ten years retention, a thick (~5nm) tunnel oxide is necessary, what degrades the programming window in FN/FN mode. Fig. 7 shows the endurance plots of Si-nc/SiN cells for three tunnel oxide thicknesses. The cells are programmed by CHEI ( $V_g=9\text{V}$ ,  $V_d=4.2\text{V}$ ,  $t_p=1\mu\text{s}$ ) and erased by FN ( $V_g=-18\text{V}$   $t_e=10\text{ms}$ ).

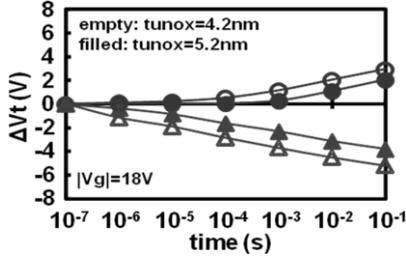


Fig. 5. Fowler-Nordheim program/erase characteristics of Si-nc/SiN cell (samples: S1 and S2).

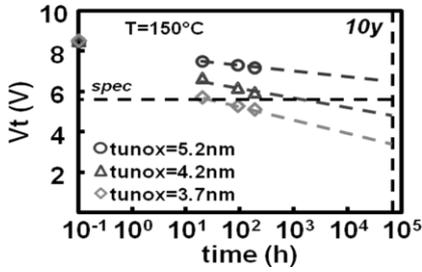


Fig. 6. Data retention at 150°C of Si-nc/SiN cell with different tunnel oxide thicknesses (samples: S1, S2 and S3).

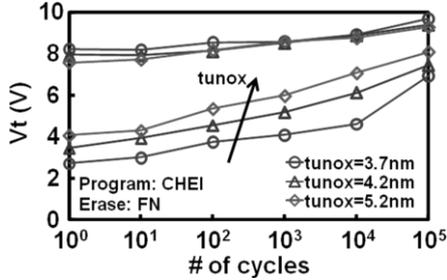


Fig. 7. Endurance characteristics of Si-nc/SiN cell, with different tunnel oxide thicknesses (samples: S1, S2 and S3).

It is important to notice that the level of programmed threshold voltage remains unchanged varying the  $t_{\text{unox}}$ , while the difference is significant on the erased state. Furthermore the charge trapping in the SiN layer reduces the cycling performances of the cell and a gradual window narrowing is measured.

### 3.2. Memory Cell Optimization

In order to improve the cell performances we decided to increase the coupling factor keeping constant the tunnel oxide thickness. We decreased the EOT of the ONO stack and increased the silicon nanocrystal size. Moreover we removed the SiN capping layer to avoid the erase saturation issue observed during cycling. We considered the capacitor model of floating gate device [11] for Si-nc cell [12] (Fig. 8).

The coupling factor of standard floating gate is calculated as follow:

$$\alpha_g = \frac{C_{\text{ONO}}}{C_{\text{ONO}} + C_{\text{tun}}} \quad (1)$$

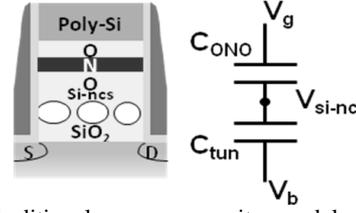


Fig. 8 Traditional memory capacitor model used for the floating-gate-like approach [12].

Where  $\alpha_g$  is the coupling factor,  $C_{\text{ONO}}$  is the IPD capacitance and  $C_{\text{tun}}$  the tunnel oxide capacitance. Decreasing the EOT of IPD stack layer the  $C_{\text{ONO}}$  is increased and the coupling factor increases. The programming window of the Si-nc cell also depends on the  $C_{\text{ONO}}$  [12]:

$$\Delta Vt = \frac{-Q_{\text{fg}}}{C_{\text{ONO}}} \Phi \quad (2)$$

Where  $\Delta Vt$  is the programming window,  $Q_{\text{fg}}$  the charge stored in the nanocrystals and  $\Phi$  is the Si-nc diameter. In this case to compensate the  $C_{\text{ONO}}$  increasing, we decided to increase the nanocrystals diameter, keeping electrical isolation in the charge trapping layer (Fig. 1c). Fig. 9 shows the corresponding FN program/erase characteristics (samples S4 and S5). One can notice that a 4V programming window can be obtained in a few microseconds, depending on the nc size. In particular the erase operation is improved increasing the diameter.

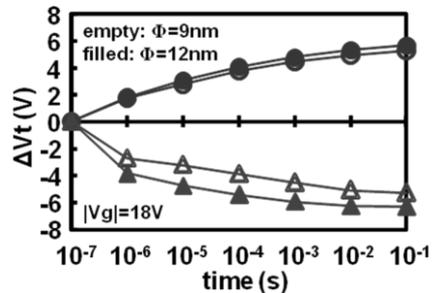


Fig. 8 Fowler-Nordheim program/erase characteristics of Si-nc optimized cells (samples S4 and S5).

Furthermore, without the SiN capping layer, the cell reliability is improved. We compared in Fig. 9 the results of data retention at 150°C obtained for the Si-nc/SiN and Si-nc cells, using the same tunnel oxide thickness (samples S2 and S5). In Fig. 10 we compared the cycling of Si-nc cells (Sample S5) using CHEI programming or full FN operations. In the first case, the programming conditions are:  $V_g=9V$ ,  $V_d=4.2V$ ,  $t_p=1\mu s$ , while the erase conditions are:  $V_g=-18V$ , 5V/ms ramp followed by 1ms plateau.

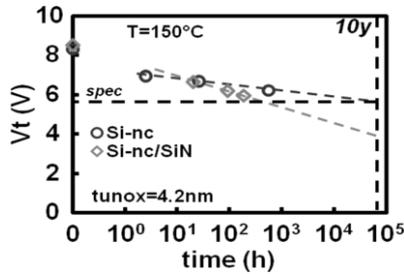


Fig. 9 Data retention comparison of Si-nc/SiN and Si-nc cells (samples S2 and S5) at 150°C.

In FN regime the absolute value of gate voltage is 20V, and the program/erase time is 3 $\mu$ s. We demonstrated that this optimized memory can be used for low power and fast applications using either NAND or NOR architectures. The impact of the covering ratio on the endurance is also investigated. Fig. 11 presents the results of 1Mcycles endurance for the Si-nc cell (samples S4 and S5). The cells are programmed by CHEI ( $V_g=9V$ ,  $V_d=4.2V$ ,  $t_p=1\mu s$ ) and erased by FN operation ( $V_g=-18V$ , 5V/ms ramp followed by 1ms plateau). Increasing the covered area the erase operation is improved. The sample, with the higher covering ratio, shows a programming window of 5.5V for the virgin state and of 4V after 1Mcycles. Moreover, without SiN capping layer, the parasitic charge trapping is avoided, and the erased  $V_t$  drift is strongly reduced.

#### 4. CONCLUSIONS

In this work, we studied the effect of tunnel oxide thickness on Si-nc/SiN cell consumption. This parameter has a limited impact on energy and programming efficiency during a channel hot electron injection. We propose to use this device with fast programming pulses for low power applications, optimizing the programming conditions, and adjusting the tunnel oxide thickness to find the good trade-off between endurance and data retention. Finally, we propose to optimize the technological features of the memory cell to improve programming window and reliability. To do this we increased the coupling factor with a thinner IPD stack ( $EOT=10.5nm$ ) and a higher covering ratio (+25%). The optimized cell is able to be programmed by CHEI or by FN ( $\Delta V_t=4V$ ) in a few microseconds. Furthermore the SiN layer capping the ncs was removed to avoid a parasitic charge trapping, reaching 10 years data retention and 1M cycles of endurance.

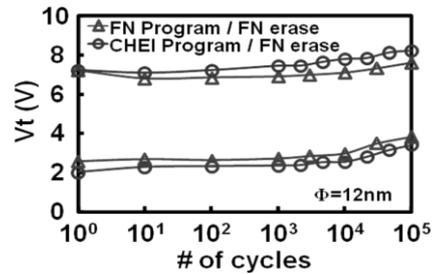


Fig. 10 Endurance characteristics of Si-nc cells (sample S5).

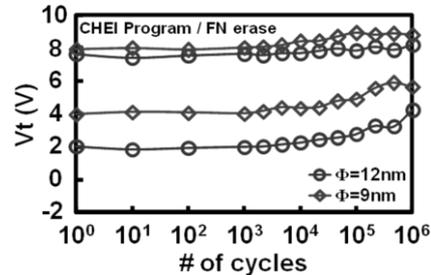


Fig. 11 Endurance characteristics with different covered areas (samples S4 and S5).

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