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Optimization of Programming Consumption of Silicon Nanocrystal Memories for Low Power Applications

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Abstract— **In this paper we propose the optimization of the programming operation scheme of Silicon nanocrystal (Si-nc) memories in order to reduce the energy consumption for low power applications. Using the program kinetic characteristics and a dynamic current measurement method, the programming window and the energy consumption during Channel Hot Electrons programming are deeply analyzed; evaluating ramp and box pulse with various gate and drain voltage biases. Finally the critical role of the tunnel oxide is evaluated to satisfy both retention and consumption requirements.**

Keywords- Silicon nanocrystal memories; energy consumption; tunnel oxide thickness.

I. INTRODUCTION

The market of nonvolatile Flash memories, for portable systems, requires more and more low energy and high reliability solutions. The silicon nanocristal Flash memory cell appears as one promising candidate for embedded applications due to its good reliability (resistance to SILC, no tail-bits) and ease of integration [1, 2]. The impact of the technological features on the memory performances was studied [3]. In order to reduce the operating voltages the integration of high-k materials in the gate stack was also proposed [4, 5]. Other architectures like split-gate memories [6, 7] allow reducing the energy consumption of the memory, but require the addition of a select transistor, controlling the programming current. In this context, the impact of the programming parameters in 1T structures during the CHE operation (signal shape, applied voltages, programming time) was not studied in details, and the optimization of the operating scheme to reduce the energy consumption is still lacking. In this paper, we focused on programming pulse shape, to evaluate the dynamic cell performances. Gate programming box and ramp pulses are used, for different bias voltages. We also propose a solution to improve the cell programming efficiency, optimizing the trade-off between the programming window (PW) and the energy consumption (Ec) of the Si-nc memory cell. Finally, the impact of the tunnel oxide thickness on the consumption and data retention is analyzed.

II. TECHNICAL DETAILS

A. *Nanocrystal fabrication process*

The first process step consisted in SiO_2 tunnel oxide growth on a P-type silicon substrate. The tunnel oxide presents either siloxane (Si-O-Si) or silanol (Si-O-H) groups on the active surface. A chemical preparation of this silicon oxide layer enables the surface hydroxylation. This cleaning increases the number of Silanol groups, which are used as nucleation sites [8].

The silicon nanocrystals are grown by Low Pressure Chemical Vapor Deposition (LPCVD) on the tunnel oxide top surface with a two-steps process. During the first step, diffusion of Silane (SiH_4) on hydrophilic surface causes the germination phenomenon; while the second step is a selective growth with Dichlorosilane (SiH_2Cl_2) diffusion [9]. Using this approach the density and size of Si-nc can be independently controlled. The first increases with Silane diffusion period and the second is controlled by the Dichlorosilane diffusion period.

B. *Sample description*

Silicon nanocrystal memories were integrated on 200mm wafers. Three different tunnel oxide thicknesses were compared: 3.7nm, 4.2nm and 5.2nm. The nanocrystals are capped by a 2nm SiN layer to avoid parasitic process oxidation. The cell stack is completed with an ONO layer with an equivalent oxide thickness (EOT) of 14nm. The cell is 80nm wide and 180nm long. In figure 1 we show TEM cross sections of the processed devices. It is worth noting the rounded active area that increases the programming efficiency due to an enhanced coupling factor [10, 11]

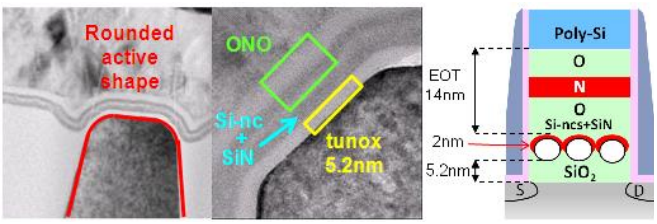

Figure 1. TEM pictures (left) and schematic (right) of silicon nanocrystal memory cell.

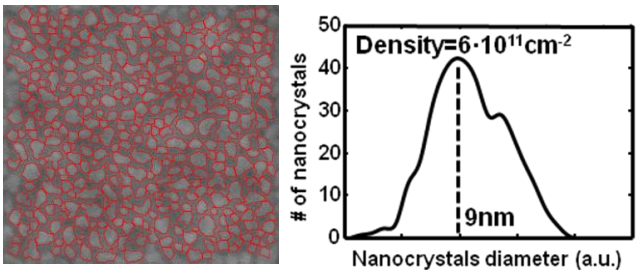

Figure 2. Silicon nanocrystal top view using Critical Dimension Scanning Electron Microscopy (CDSEM), and nanocrystal diameter extrapolated distribution.

The nanocrystals are observed in top view using an in-line Critical Dimension Scanning Electron Microscopy CDSEM; their average size and density are extracted with a technique of image processing (figure 2). The extracted average size of nanocrystals diameter is 9nm while the density is $6 \cdot 10^{11} cm^{-2}$.

III. Experimental Results

In this section we study the dependence between program pulse shape, biases, and the programming consumption of Si-nc memory cells. To this aim, the experimental setup described in [12] is used. The setup (figure 3) includes in particular an Agilent B1500 semiconductor device analyzer, equipped by two pulse generator modules WGFMU (Waveform Generator and Fast Measurement Unit). In this way, it is possible to measure the drain current during the programming operation for periods of several microseconds. Moreover a study on effect of tunnel oxide thickness is presented.

A. Inpact of programming scheme on energy consumption

To understand the dynamic evolution of the programming window and the energy consumption during the CHE operation, we performed programming kinetic experiments using box and ramp pulses. Each time, before the cell programming, a smart erase procedure was performed to reach the expected threshold voltage (Vt) value. In figure 4a-b are plotted the applied gate pulses during programming; while in figure 4c-d are shown the measured dynamic drain currents (Id). One should note that the drain current follows the gate voltage potential, indicating a transistor-like behavior [13]. The experiments were repeated for different gate and drain voltages (Vg and Vd), to evaluate the impact of the biasing conditions on the cell performances. Considering these results we calculated the consumed programming energy Ec during the CHE operation as follows:

$$Ec = \int_{t=0}^{t=tp} (Id \cdot Vd) dt. \qquad (1)$$

where Id is the drain current consumption, tp the programming time, and Vd the programming drain bias. In figure 5 the window and the energy are plotted keeping constant the programming time. It appears that the box pulse is more efficient in terms of programming window than the ramp, paying with higher energy consumption. Moreover increasing the drain voltage of 0.4V leads to the same gain in terms of memory window than increasing Vg of 1.2V.

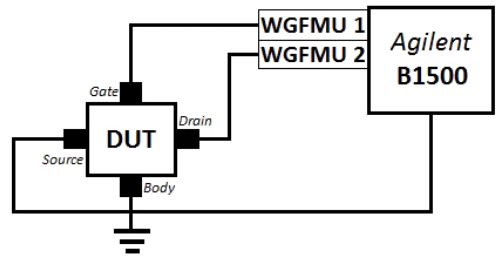

Figure 3. Experimental sutup used to measure the current consumption during the channel hot electron prigramming operation.

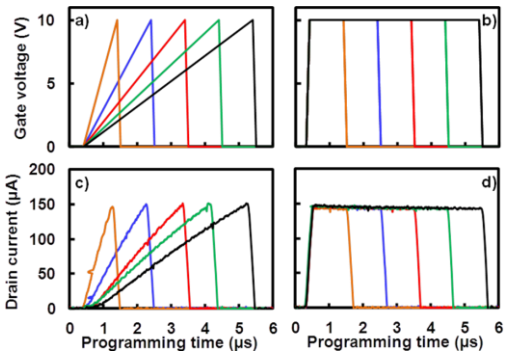

Figure 4. (a) Ramp and (b) box gate pulses used to program the cell by CHE; Vd=4.2V. Dynamic drain currents measured with (c) ramp and (d) box pulses.

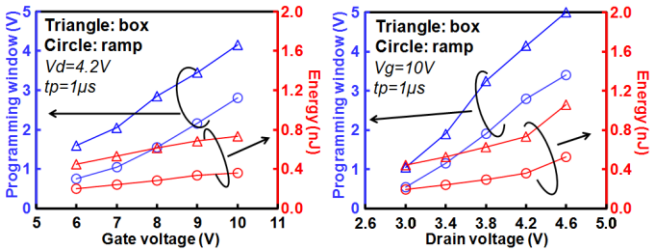

Figure 5. Programming window and energy consumption as a function of the gate (left) and drain (right) voltage. Ramp and box gate pulses are used.

To better understand the cell performances as a function of programming time, the programming energy is plotted as a function of the programming window (figure 6). The box pulse allows increasing the programming window keeping constant the energy consumption and the biasing conditions. The abrupt variation of Vg allows to start the hot carrier generation at the beginning of the programming time. Using a ramp the hot electron injection starts when Vg≈Vd [14, 15], in this way the programming efficiency is lower. The programming window tends to saturate, leading to higher required programming time. This is due to the quantity of injected charges that modify the vertical electric field during the programming operation. Considering these results we defined the programming efficiency as the ratio between the programming window and the energy consumption. In figure 7 we report this programming efficiency in case of box pulse for different biasing conditions. One can notice the linear dependence with the gate voltage (or vertical electric field). On the other hand an optimized efficiency is measured for Vd=4.2V.

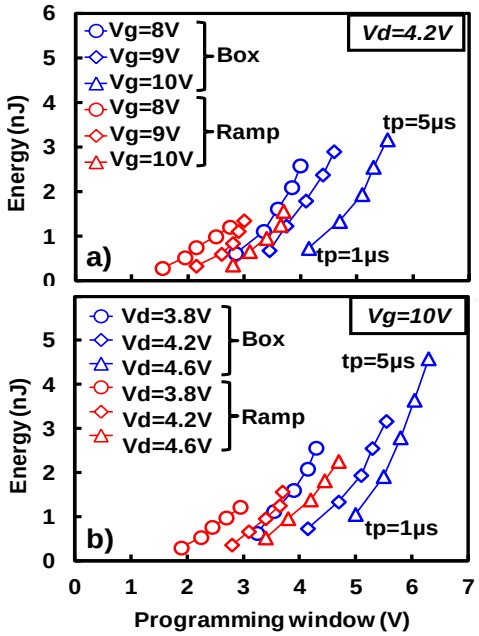

Figure 6. Energy consumption as a function of the programming window for different gate (a) and drain (b) voltages.

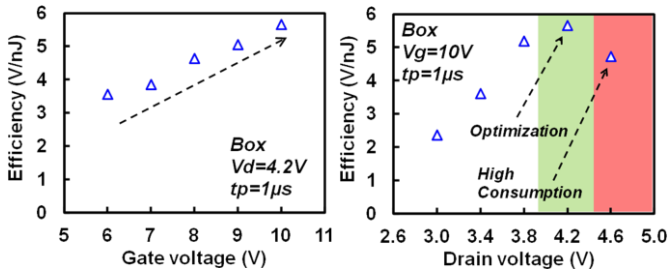

Figure 7. Efficiency (PW/Ec) vs gate (left) and drain (right) voltage, using tp=1µs.

When the drain voltage is higher than 4.2V, the programming injection tends to saturate while the drain current increases, increasing the consumption and reducing the programming efficiency.

Using the optimized programming scheme (Box pulse, Vg=10V and Vd=4.2V), we plotted the efficiency in figure 8 as a function of the programming time. The graph shows that silicon nanocrystal memories are suitable for fast programming operation, reaching the best trade-off between PW and Ec.

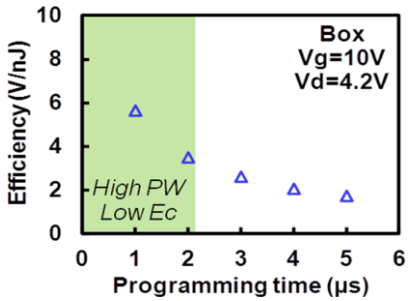

Figure 8. Efficiency in function of programming time for Si-nc cell, using box gate pulses (Vg=10V, Vd=4.2V).

B. Impact of Tunnel Oxide Thickness on cell performances

In this section we studied the impact of the tunnel oxide thickness (tunox) on the programming operation (memory window and programming consumption) and data retention. We performed first programming kinetic experiments using cumulative box pulses for two tunnel oxide thicknesses (figure 9). A very small impact of the tunnel oxide thickness on the threshold voltage shift is observed, in agreement with Hot Carrier Injection theory. We can also notice that most of the charge is injected during the first microsecond of programming. In figure 10 the energy consumption is plotted as a function of the programming window using the optimized programming conditions identified before (box pulse, Vg=10V and Vd=4.2V). Once again the tunnel oxide thickness has a limited influence on the consumed energy and the programming window during the CHE programming. In particular to achieve a 4V programming window, a programming pulse of 1µs is sufficient, for the two tunnel oxide thicknesses, with a consumption energy lower than 1nJ.

In conclusion we demonstrated that this technological parameter does not play an important role to reduce the programming efficiency (figure 11). In this way, the tunnel oxide thickness is adjusted depending on the retention requirements. In figure 12 we extrapolated the 10 years data retention at 150°C for different tunnel oxide thicknesses. In order to reach the charge loss specification for portable devices, a tunox of 5.2nm is the minimum required value. Because the parasitic charge trapping in SiN capping layer [16], further improvements can be obtained avoiding this step process.

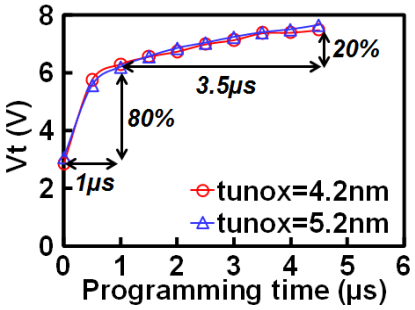

Figure 9. Channel Hot Electron threshold voltage (Vt) kinetic characteristics using the box pulses, for the tunnel oxide thicknesses of 4.2nm and 5.2nm.

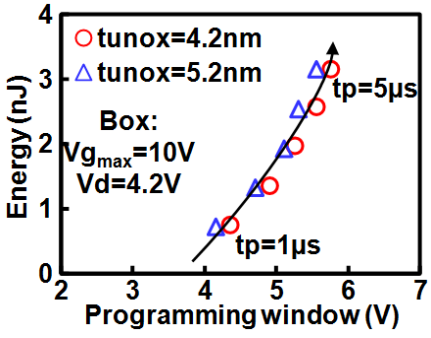

Figure 10. Energy consumption as a function of the programming window for cells with 4.2nm and 5.2nm tunnel oxide thicknesses using box pulses (Vg=10V, Vd=4.2V).

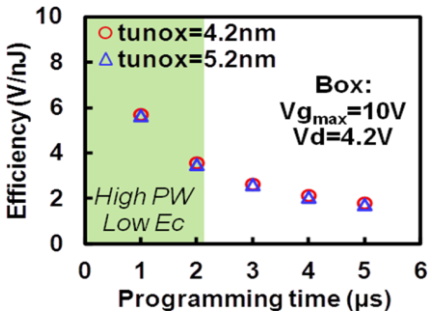

Figure 11. Efficiency in function of programming time for cells with 4.2nm and 5.2nm of tunnel oxide thickness (Vg$_{max}$=10V, Vd=4.2V).

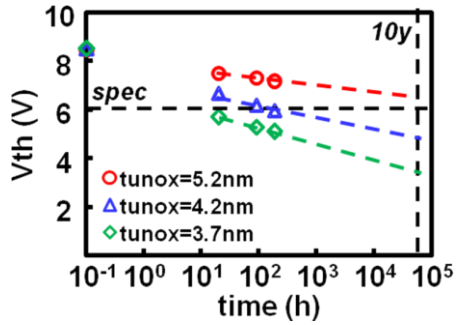

Figure 12. Data retention at 150°C for tunnel oxides of 5.2nm, 4.2nm, 3.7nm.

IV. Conclusion

In this work we studied the impact of programming scheme on energy consumption for silicon nanocrystals memory cell. We propose an optimization concerning the programming pulse shape demonstrating the best efficiency of box pulse versus the ramp. The linear dependence on gate voltage is shown, while an optimum point of work is found for a 4.2V drain voltage. The consumption has been reduced up to 1nJ reaching a programming window bigger than 4.5V. Moreover the best trade-off to improve the cell efficiency is obtained using very fast pulses that is a crucial point for portable applications. Finally we demonstrated that the programming efficiency does not depend on tunnel oxide thickness during a channel hot electron programming operation for silicon nanocrystal memories.

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