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Improved Performance of Silicon Nanocrystal Memories for Application Working Over a Wide Range of Temperature

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The microelectronic industry requires more and more low consumption and high reliability solutions. In this scenario the silicon nanocrystal memories (Si-nc) are one of the most mature technologies able to replace the Flash floating gate in NOR embedded applications. The main advantages of Si-nc memories are: the full compatibility with the CMOS process using a reduced number of masks (1) and the robustness against SILC (2). In this paper we present an experimental work on the optimized silicon nanocrystal cell industrially manufactured, where the reliability is improved (3). In particular the impact of silicon nanocrystals size and temperature on cell programming window is shown. Moreover we demonstrated for the first time at our knowledge that it is possible to achieve 1Mcycles endurance characteristic in the temperature range of [-40°C; 150°C], programming by channel hot electron (CHE) and erasing by Fowler-Nordheim (FN).

Technical Details

The Non-Volatile Memories (NVM) integrating silicon nanocrystals are considered as an emerging solution to extend Flash memories downscaling. In this paragraph we explain the Si-nc industrial nucleation and grown fabrication process by Low Pressure Chemical Vapor Deposition (LPCVD). In a context of technological industrialization, it is of primary importance to develop in-line metrology tools dedicated to Si-nc growth process control. Hence, silicon nanocrystals were observed in top view by using an in-line Critical Dimension Scanning Electron Microscopy (CDSEM), thus their average size and density were extracted from image processing (4).

Silicon nanocrystal fabrication process

Silicon nanocrystals were grown on top of a thin silicon oxide (SiO₂) by Low Pressure Chemical Vapor Deposition two steps recipe. The active tunnel oxide surface was chemically prepared to increase the number of silanol groups which are used as nucleation sites; this cleaning step impacts the final tunnel oxide thickness (5). SiO₂ top surface presents both siloxane (Figure 1a) and silanol (Figure 1b) units. The two steps process was used in either epitaxy tool or in industrial LPCVD furnace. The first step consists in nucleation with silane (SiH₄) diffusion on hydroxyl tunnel oxide surface (Figure 1c). The second step concerns a selective growth achieved by using

dichlorosilane (SiH_2Cl_2) diffusion (Figure 1d). Thanks to this two step process, the Si-nc size and density may be controlled independently. Nucleation step enables controlling the number of Si-nc on top surface of tunnel oxide while the size is monitored by the selective growth period (6).

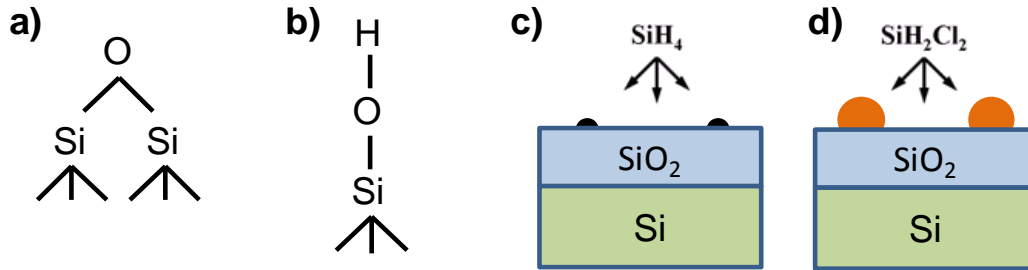


Figure 1. Schematics of: a) siloxane units, b) silanol units, c) Si-nc nucleation step by silane (SiH_4) and d) selective growth by using dichlorosilane (SiH_2Cl_2).

Process characterization

In this study, we present two optimized recipes with size and density variations to modulate the covering device area. Silicon nanocrystals size and density were observed with an industrial CDSEM tool which was generally used to control critical photolithography dimensions (Figure 2.a) (6).

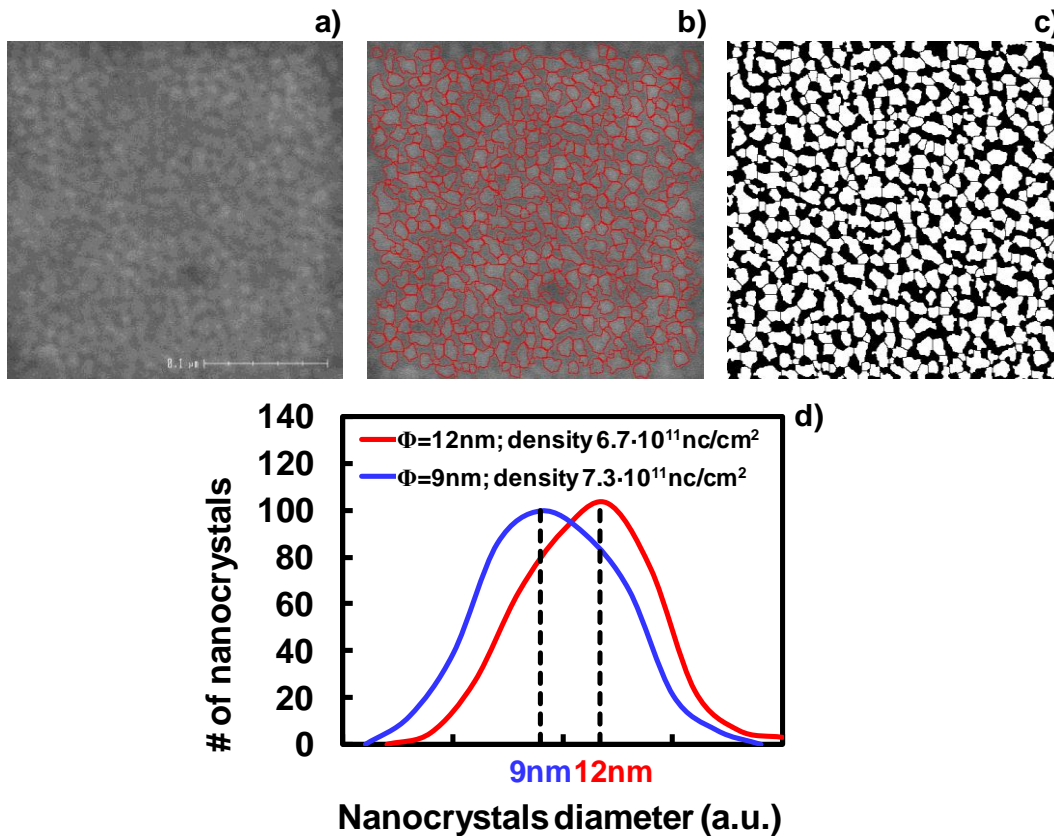


Figure 2. a-c) CDSEM image processing to calculate nanocrystals size and density, d) nanocrystals size distributions obtained for two different recipes.

A dedicated tool developed with Image-J software is used to automatically extract the Si-nc morphological parameters: diameter (Φ) and density (γ). After contrast optimization and image processing (Figure 2b-c), the mean values of Si-nc diameter and density have been obtained for two different recipes: $\Phi=9\text{nm}$ density= $7.3\cdot 10^{11}\text{nc/cm}^2$ and $\Phi=12\text{nm}$ with density= $6.7\cdot 10^{11}\text{nc/cm}^2$. In Figure 2d we plotted the silicon nanocrystal size distributions, the average diameter and density are also reported for two different recipes. The size dispersion is due to the high nuclei number generated during the silane diffusion time. More over the long time of growth used to have thick silicon nanocrystals increases the probability to achieve coalescence phenomena. In next paragraph the electrical results obtained with this kind of samples will be presented.

Experimental Details and Discussion

In this section the results concerning the programming window characterization and reliability experiments are presented. The silicon nanocrystal memory cell was characterized using a channel hot electron programming and Fowler-Nordheim erase operation. With this procedure we evaluated the impact of silicon nanocrystals size and temperature on threshold voltage kinetic during program/erase operations. Moreover we studied the reliability of silicon nanocrystal memory cell, in a wide range of temperature [-40°C ; 150°C]; we show the good cell functionality after 1M cycles. The impact of silicon nanocrystal size on data retention is also evaluated at 150°C starting from fixed programmed and erased states (8). The comprehension of experimental results will be useful to improve the cell performances for high reliability applications.

Effect of silicon nanocrystal size

The impact of silicon nanocrystals size on programming window has already been analyzed in literature, (9-11), nevertheless it is important to evaluate its effect on Si-nc cell in order to optimize the cell performances. The studied samples have a channel width of 90nm and a channel length of 180nm, the cell stack is described in Figure 3.

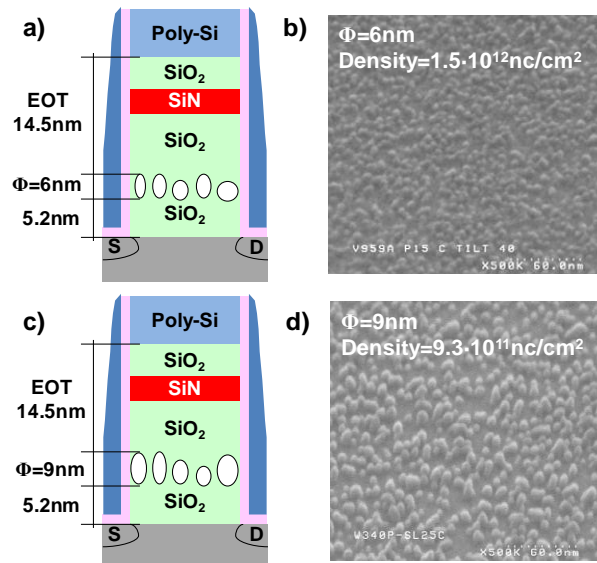


Figure 3. a) and c): silicon nanocrystal cells schematics used to evaluate the impact of nanocrystal size. b) and d) are the corresponding 40° tilted CDSEM pictures.

The 5.2nm thick tunnel oxide was grown on a p-type substrate. The silicon nanocrystals average size and density were measured in-line using Critical Dimension Scanning Electron Microscopy technique (7), in this case we compare the samples with two diameters $\Phi=6\text{nm}$ and $\Phi=9\text{nm}$. Then, to complete the stack, the ONO (Oxide-Nitride-Oxide) Inter-Poly Dielectric (IPD) layer was deposited to reach 14.5nm of Equivalent Oxide Thickness (EOT). The Figure 4a shows the dispersion of program/erase threshold voltages (V_t) obtained performing a full wafer statistical measurements (30 samples). The evaluation of programming window dispersion was performed using a fixed $5\mu\text{s}$ programming pulse, the gate voltage (V_g) of 9V, drain voltage (V_d) of 4.2V, the source and the bulk voltages (V_s and V_b respectively) of 0V. Concerning the erase, a pulse of 90ms was applied on gate terminal using $V_g=-18\text{V}$, while drain, source and body terminals were grounded. The minimum program/erase levels to have a good memory functioning are highlighted. Using our extrapolation it is necessary to increase the nanocrystal diameter up to 14nm, maintaining unchanged the cell stack, in order to achieve the attended levels. Using the measured size and density (Figure 3).we plot the correlation between the programming window and the percentage of covered area in Figure 4b; increasing the covered area, thus the coupling factor, the programming window increases. Using this cell structure to achieve the minimum programming window of 4V the 95% of covered area is needed, that is not coherent with the principle of Si-nc cell. Moreover the window increases with the silicon nanocrystals size as well as the dispersion on wafer. The diameter increasing of 3nm allows achieving the programming window increasing of 0.5V.

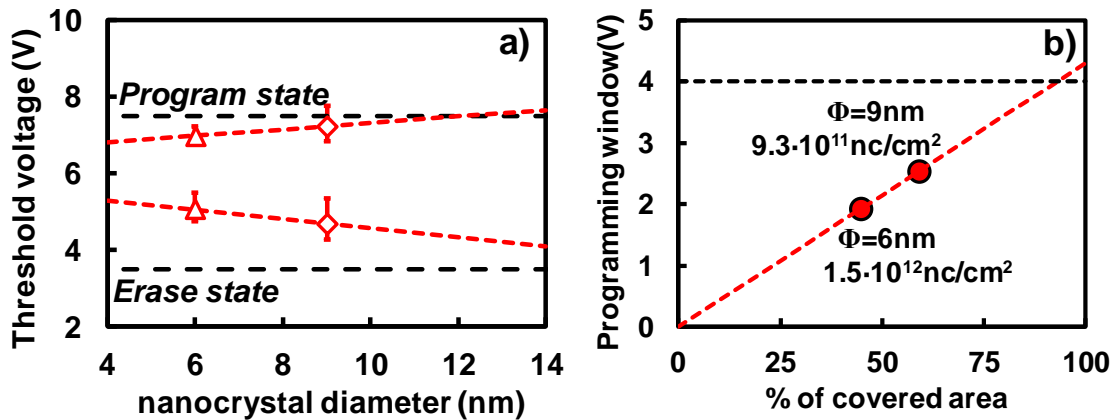


Figure 4. Statistical results of program/erase threshold voltage measured for samples with different silicon nanocrystal sizes ($\Phi=6\text{nm}$ and $\Phi=9\text{nm}$).

The program/erase kinetic characteristics using ramped gate signals are also evaluated and compared in Figure 5. The programming kinetic was performed applying 4.2V on drain terminal and a staircase from 3V to 9V with the step of 0.75V followed by an additional pulse of $0.5\mu\text{s}$ on gate terminal. The duration of each pulse was $0.5\mu\text{s}$ in order to obtain a $1.5\text{V}/\mu\text{s}$ ramp speed. For the erase kinetic, 10V pulses were applied on bulk terminal while on gate terminal was applied a staircase from -4V to -10V, to reach the gate-bulk voltage of 20V. The steps amplitude was 0.25V, while the duration was $50\mu\text{s}$ in order to emulate the 5kV/s ramp. In Figure 5a we notice that increasing the nanocrystals size the programming window is improved, because the covering area increases as well as the cell coupling factor. In particular the impact of covering area increasing is evident

on erase threshold shift (Figure 5b). In literature is shown that the FN erase speed increases when the nanocrystals size decreases (10), this is true for specific cell architectures, and in particular for small nanocrystal diameters, but increasing the nanocrystal size and the covered area the coulomb blockade effect and quantum mechanisms can be neglected (9), thus the coupling factor dependence becomes predominant. It is important to notice that using the ramped gate voltage the program/erase efficiency decreases with respect to the box pulses used for the statistical measurements shown in Figure 4 (12).

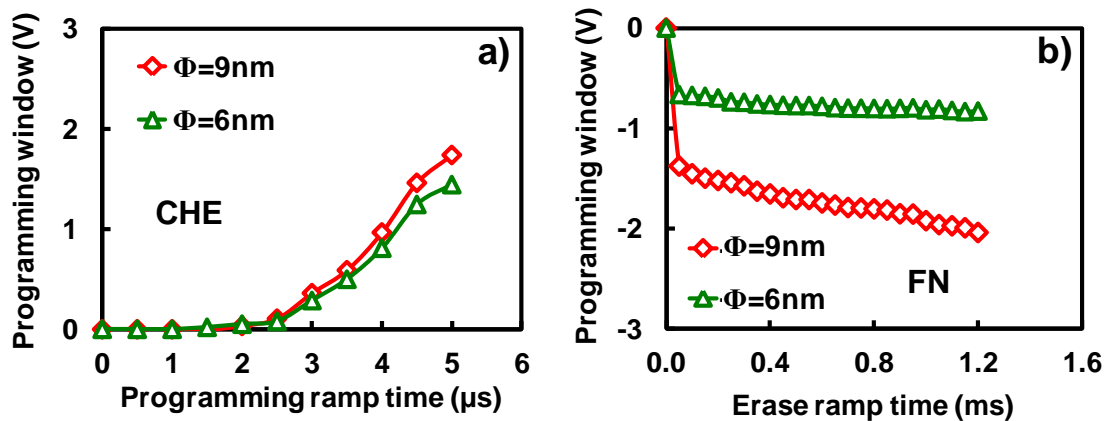


Figure 5. a) Channel hot electron (CHE) ramped programming kinetic and b) Fowler-Nordheim (FN) ramped erase kinetic measured on samples with $\Phi=6\text{nm}$ and $\Phi=9\text{nm}$.

Silicon nanocrystal cell optimization

In the last paragraph we evaluated the impact of silicon nanocrystal size on memory cell programming window. The reported trends have been found evidence in the literature. In order to optimize the silicon nanocrystal cell we have taken into account that increasing the silicon nanocrystals size, thus the covered area on channel, the programming window increases. Moreover to improve the cell performances we decided to increase the Fowler-Nordheim erase efficiency decreasing the tunnel oxide thickness. We decreased also the EOT of the ONO stack and increased the silicon nanocrystal size. We considered the capacitor model of floating gate device (13) for Si-nc cell (9) (Figure 6). The coupling factor (α_g) of standard floating gate is calculated as follow:

$$\alpha_g = C_{\text{ONO}} / (C_{\text{ONO}} + C_{\text{tun}}) \quad [1]$$

Where C_{ONO} is the IPD capacitance and C_{tun} is the tunnel oxide capacitance. Decreasing the EOT of IPD stack layer the C_{ONO} is increased and the coupling factor increases. The programming window of the Si-nc cell also depends on the C_{ONO} :

$$\Delta V_t = (-Q_{\text{fg}} / C_{\text{ONO}}) * \Phi \quad [2]$$

Where ΔV_t is the programming window, Q_{fg} the charge stored in silicon nanocrystals and Φ is the Si-nc diameter. In this case to compensate the C_{ONO} increasing, we decided to increase the diameter, keeping electrical isolation between the silicon nanocrystals (Figure 2).

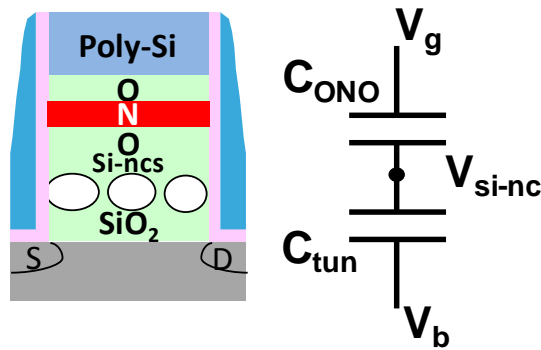


Figure 6. Memory capacitor model used for the floating-gate-like approach (9).

The layers stacked in the optimized nanocrystal cell are shown in Figure 7. The tunnel oxide thickness was chosen 4.2nm thick in order to improve the FN erase operation, while the EOT of ONO interpoly dielectric was thinned down to 10.5nm to increase the vertical electric field. We can observe in (1) that decreasing the ONO thickness, C_{ONO} is increased thus the programming window decreases. To compensate this effect the nanocrystal diameter is increased from 9nm up to 12nm increasing the covered portion of channel area thus the coupling ratio.

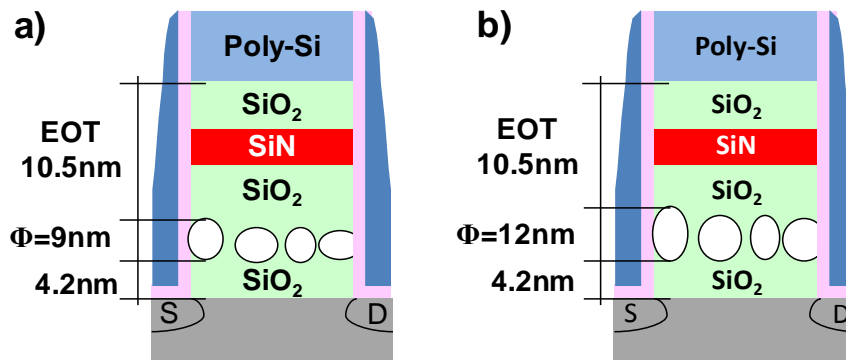


Figure 7. Schematic of optimized silicon nanocrystal memory stack; two different types of nanocrystals are implemented: a) $\Phi=9\text{nm}$, b) $\Phi=12\text{nm}$.

In Figure 8 are plotted the program/erase kinetic characteristics for the optimized stack comparing the memory devices with two different nanocrystal size: $\Phi=9\text{nm}$ and $\Phi=12\text{nm}$. The dispersion on wafer is also highlighted (30 tested samples); it results to be limited with respect the nanocrystals diameter. One can notice that the dynamic of CHE programming operation is not affected by the silicon nanocrystals diameter, while the evidence of covering area increasing is shown on the erase kinetic. In this case the quantum and Coulomb blockade effects are negligible because the big size of nanocrystals (9); using $\Phi=12\text{nm}$ the time of erase to reach a 4V programming window is lower than 1ms. The cell optimization allows achieving best results using $\Phi=9\text{nm}$ with respect the non-optimized stack shown in Figure 5; the same types of program/erase ramped gate voltages are used.

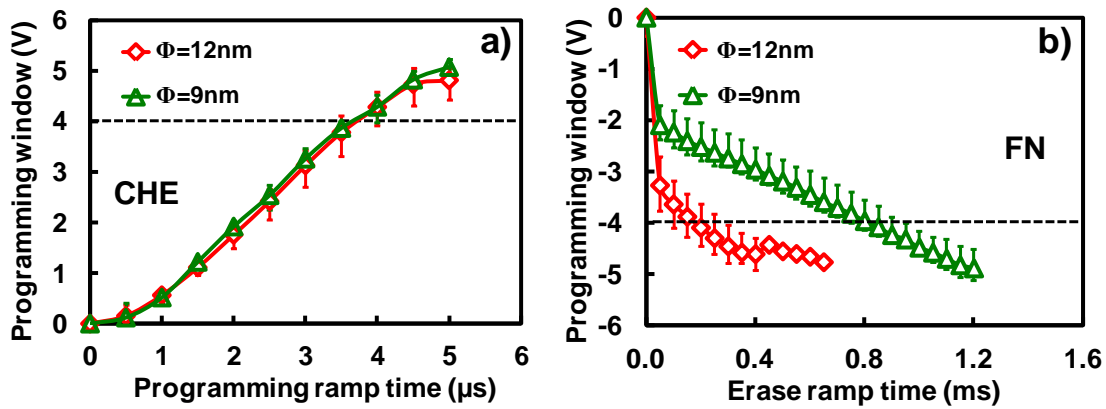


Figure 8. a) Channel hot electron (CHE) ramped programming kinetic and b) Fowler-Nordheim (FN) ramped erase kinetic measured on samples with optimized memory stack and two different nanocrystals size: $\Phi=9\text{nm}$ and $\Phi=12\text{nm}$.

We complete the optimized cell characterization with the results concerning the endurance cell degradation. The optimized Si-nc cells were programmed by CHE: $V_g=9\text{V}$; $V_d=4.2\text{V}$; $t_p=1\mu\text{s}$; and erased by FN: $V_g=-18\text{V}$; $t_e=\text{ramp}=5\text{kV/s} + \text{plateau}=1\text{ms}$. Using this memory stack it is possible to decrease the programming and erase time thanks to the higher covered area and associated coupling factor. The very weak shift of program/erase threshold voltages allows achieving a good programming window after 100k cycles that is the typical Flash memories target. This result was reached without a pre-cycling cell treatment (14). We show in Figure 9 the 1Mcycles endurance characteristics using two different nanocrystal sizes ($\Phi=9\text{nm}$ and $\Phi=12\text{nm}$). The cell with 12nm Si-nc is able to maintain a 4V programming window after 1M cycles (3), improving the results published in (15); in Table I the amounts of programming window before and after the cycling as well as the threshold voltage shifts are reported. The threshold voltage shift is due in particular to the charge trapping in defects generated at the interface and in the tunnel oxide, during the cycling.

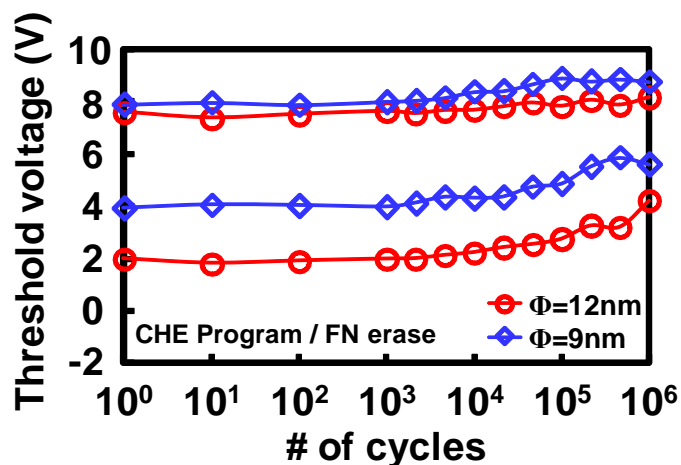


Figure 9. Endurance characteristics of optimized silicon nanocrystal memory comparing two different nanocrystal sizes: $\Phi=9\text{nm}$ and $\Phi=12\text{nm}$. The cells are programmed by CHE ($V_g=9\text{V}$, $V_d=4.2\text{V}$, $t_p=1\mu\text{s}$) and erased by FN ($V_g=-18\text{V}$, $\text{ramp}=5\text{kV/s}+\text{plateau}=1\text{ms}$).

TABLE I. Programming window before and after 1M program/erase cycles, and program/erase threshold voltage shifts; the studied samples have different nanocrystal sizes: $\Phi=9\text{nm}$ and $\Phi=12\text{nm}$.

Si-nc diameter	Programming window after 1cycle	Programming window after 1M cycles	Program threshold voltage shift	Erase threshold voltage shift
$\Phi=9\text{nm}$	4.0V	3.2V	0.9V	1.7V
$\Phi=12\text{nm}$	5.6V	4.0V	0.6V	2.2V

Temperature effect on silicon nanocrystal memories

In Figure 10a we show the impact of temperature during the channel hot electron programming operation on the sample with 12nm nanocrystals. The threshold voltage evolution is obtained using a drain voltage of 4.2V and applying the 1.5V/ μs ramp between 3V and 9V on gate terminal. The programming window decreases increasing the temperature because the channel current for high drain voltages decreases; also the injected current from the channel to nanocrystals decreases as well as the substrate current, hence decreasing the injection probability (16, 17). Moreover, at low temperature, an increase of mobility is observed for Si-nc transistors generating a quasi-linear increase of the threshold voltage (18). Opposite is the case of erase operation, in Figure. 10b the FN erase kinetic characteristics are obtained applying a 5kV/s ramp on gate terminal. In this case, the erase efficiency increases with the temperature. This is justified assuming that the dominant conduction mechanism is traps assisted (19). This cell is able to reach a 4V programming window independently on temperature in the range of $[-40^\circ\text{C}; 150^\circ\text{C}]$. The program/erase time are typical of low power and high speed applications.

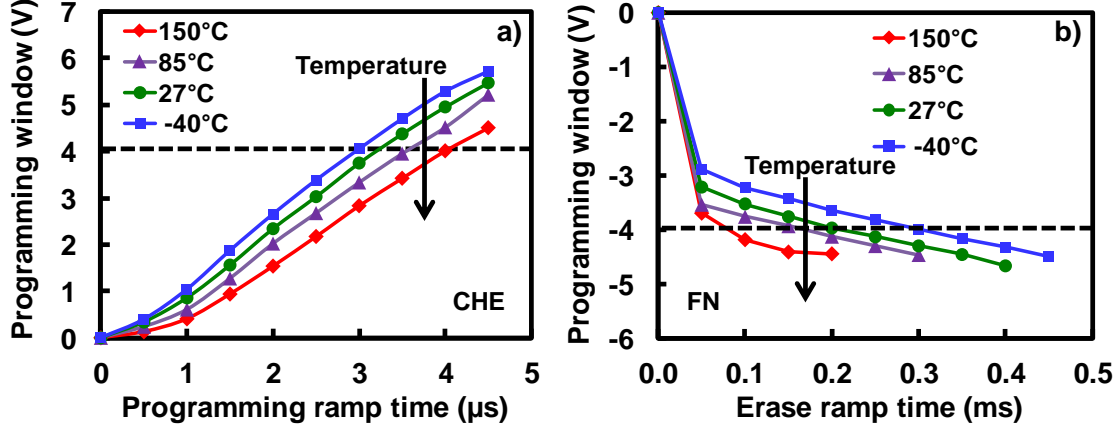


Figure 10. Temperature dependence of a) channel hot electron (CHE) ramped programming and b) Fowler-Nordheim (FN) ramped erase.

Using the program/erase conditions reported for the experiments at 27°C , we repeated the cycling varying the temperature ($T=-40^\circ\text{C}$ and $T=150^\circ\text{C}$). In Figure 11 the results are shown for the Si-nc cell with the higher covering ratio ($\Phi=12\text{nm}$). The programming window after 1Mcycles remains bigger than 4V independently on the temperature. One can notice that increasing the temperature the characteristic shifts toward lower voltages; specific algorithms of reading can be developed to adjust the sense amplifier reference levels. In Table II the programming window before and after the cycling as well as the threshold voltage shifts are reported for different temperatures: $T=-40^\circ\text{C}$, $T=27^\circ\text{C}$ and $T=150^\circ\text{C}$.

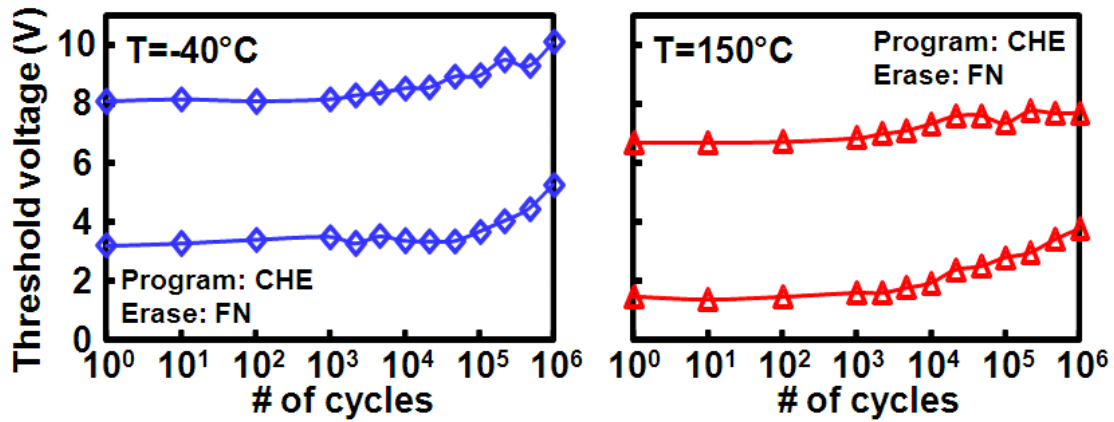


Figure 11. Endurance characteristics of Si-nc cells at $T=40^{\circ}\text{C}$ and $T=150^{\circ}\text{C}$. CHE programming and FN erase.

TABLE II. Programming window before and after 1M program/erase cycles, and threshold voltage shifts of Si-nc cell ($\Phi=9\text{nm}$ and $\Phi=12\text{nm}$), at different temperature: -40°C , 27°C and 150°C .

Temperature	Programming window after 1cycle	Programming window after 1M cycles	Program threshold voltage shift	Erase threshold voltage shift
-40°C	4.9V	4.9V	2.0V	2.0V
27°C	5.6V	4.0V	0.6V	2.2V
150°C	5.2V	4.0V	1.0V	2.3V

To complete our study we compare in Figure 12 the shift of programmed and erased states versus time at 150°C , of the optimized stack integrating silicon nanocrystals with two different sizes ($\Phi=9\text{nm}$ and $\Phi=12\text{nm}$). The impact of silicon nanocrystals size on data retention is limited, and the programming window closure due to the charge loss is unchanged (20, 21).

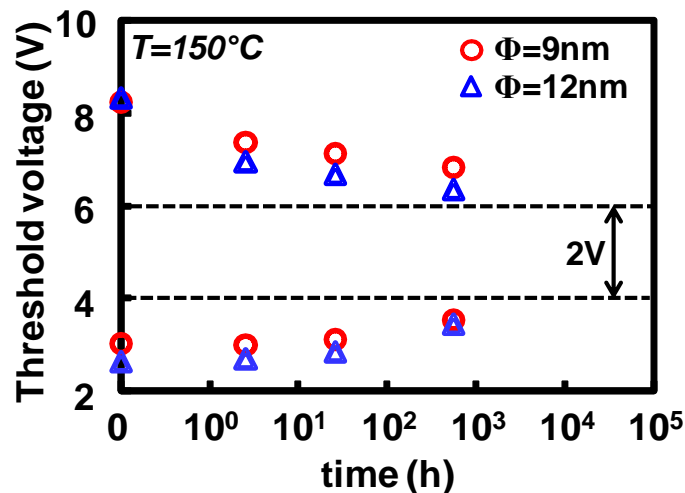


Figure 12. Data retention characteristics of programmed and erased states at 150°C . Silicon nanocrystals with different sizes ($\Phi=9\text{nm}$ and $\Phi=12\text{nm}$) are integrated in the optimized memory cell stack.

Conclusion

In this paper we presented the impact of silicon nanocrystal size and temperature on programming window and endurance characteristics. The nanocrystals size and density are controlled by a two steps fabrication process and measured in-line with a CDSEM image processing tool. We propose an optimization of cell architecture in order to improve its performances and increase the cell endurance up to 1M cycles maintaining a 4V programming window after degradation. Electrical characterization over a wide range of temperature [-40°C; 150°C] have been performed, in order to understand the cell behavior. We demonstrated that the optimized cell with higher coupling factor maintain however a good functioning after 1M cycles on the defined temperature range. Finally we have shown the limited impact of silicon nanocrystal size on data retention at 150°C.

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