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## Accélération matérielle pour l'imagerie cérébrale par EEG

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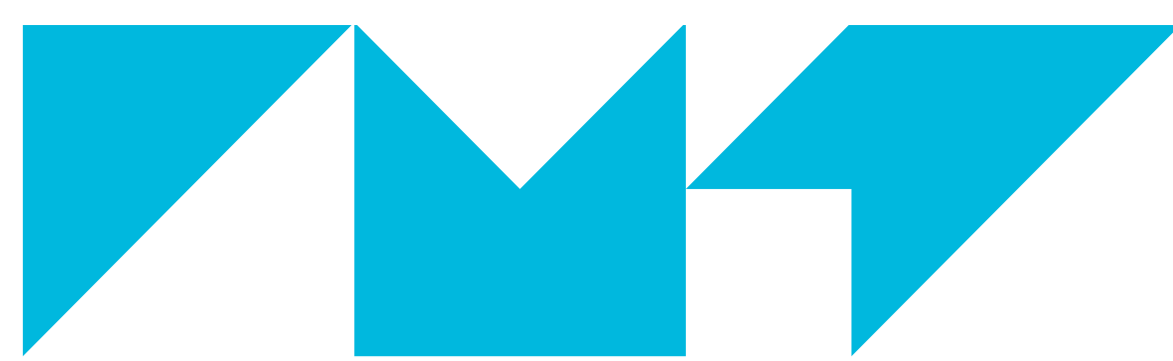
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# Hardware acceleration for EEG brain imaging

## Partner



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## Funding



## Context

### ► Brain Computer Interface (BCI)

- Invasive methods are risky for the patient, expensive but provide high accuracy)
- Non-Invasive methods are safer, cheaper but with less accuracy

### ► EEG BCI

- Non-Invasive method
- Machine learning techniques require long learning sequences
- Specific to the session, the patient

### ► From surface to volume model

- Increases the accuracy
- Requires to adress the EEG inverse-problem

## Algorithm

- Construction of the brain electrical model
- Number of operations increases in a **quadratic way** with the number of considered dipoles
- Need of **non-linear functions**:
  - Reciprocal
  - Square-root
  - Inverse square-root
  - Arctan
  - Natural logarithm

## Results

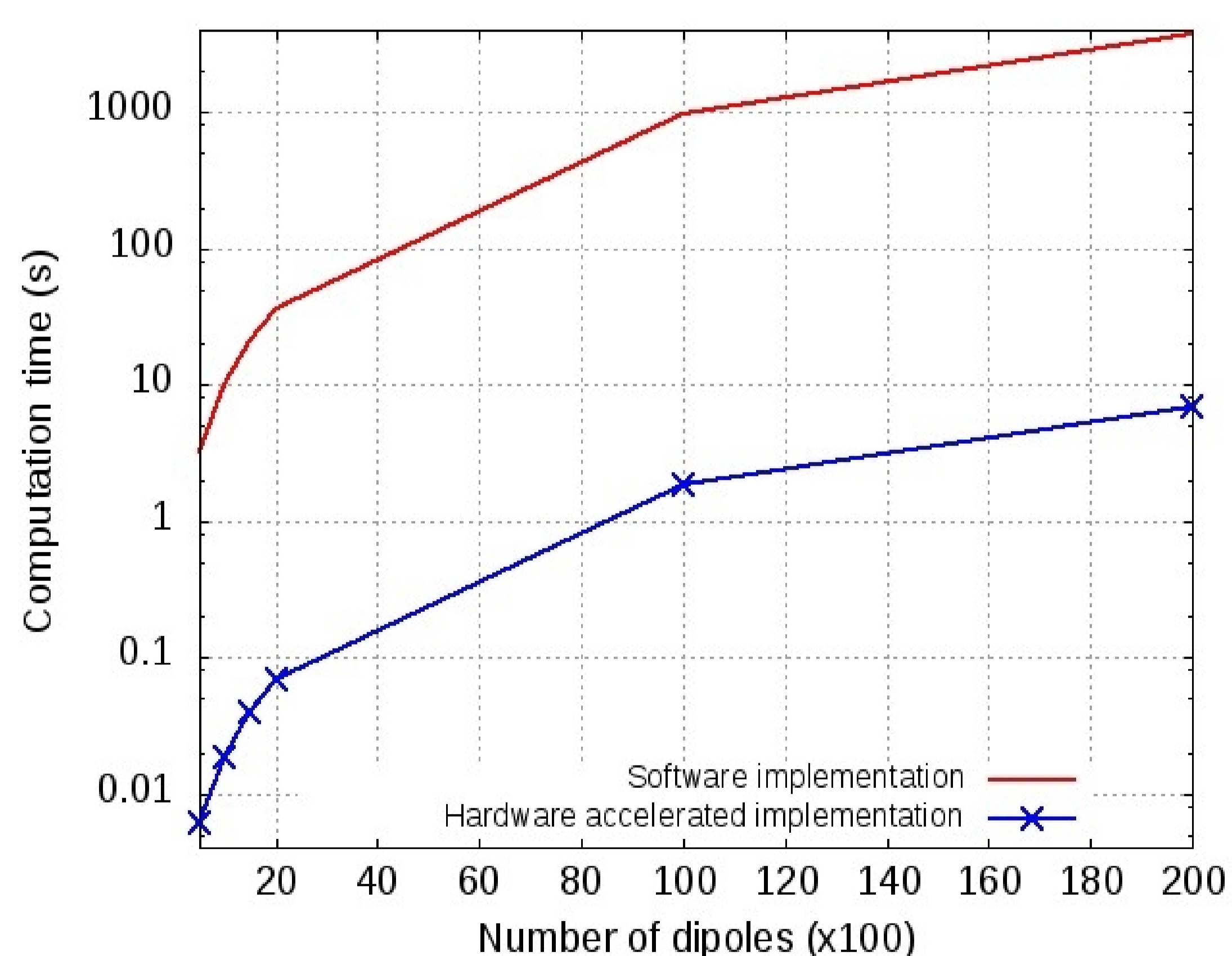
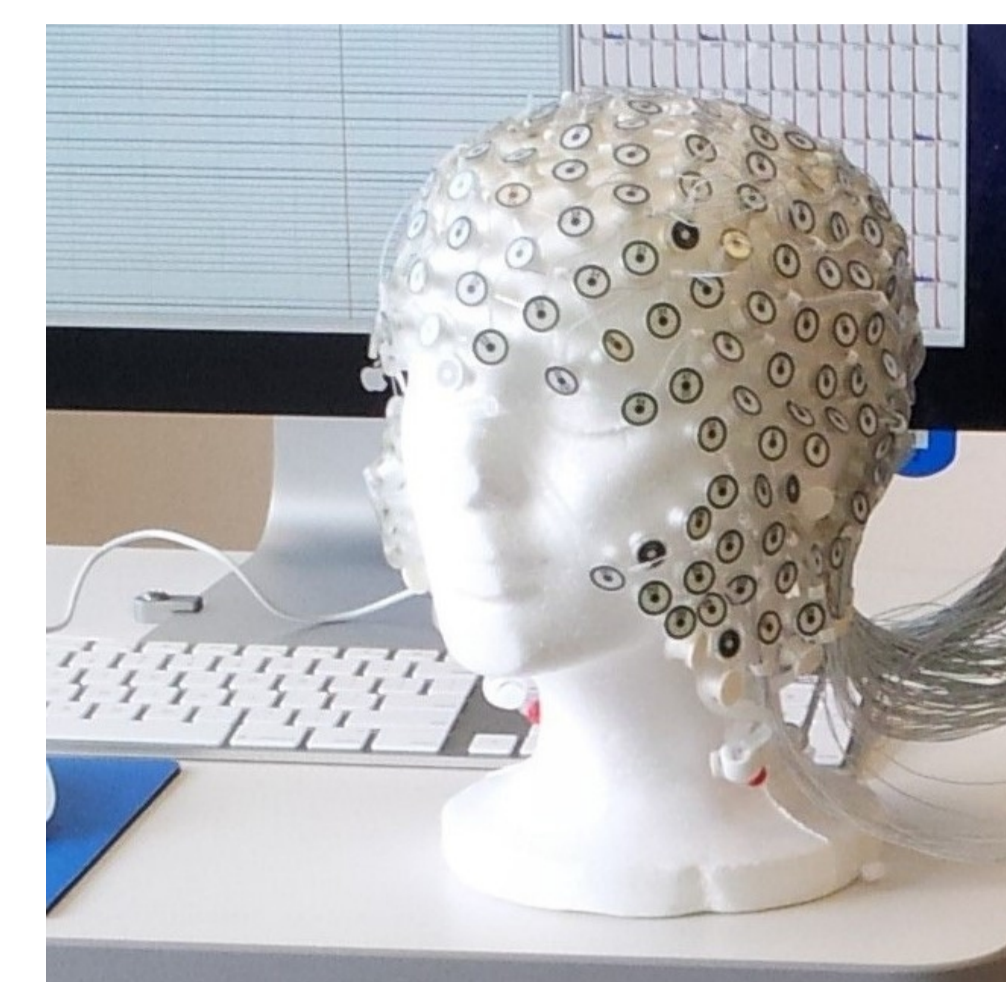


Figure 2: Computation times for the model construction expectations

- Test with a design using 50 % of the Virtex-7 690T
- Different tested functions (FFT, arctan, inverse square-root)
- **Speed-up by 530** (reference: Intel Xeon E5-1620 v2)
- 1 hour becomes 7 seconds !

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## Objectives

- **Explore the opportunity of hardware acceleration**
  - Choose the FPGA technology
  - Create a dedicated circuit
  - Use a PCIe link between the CPU and the acceleration block
- **Estimate the potential acceleration gain**

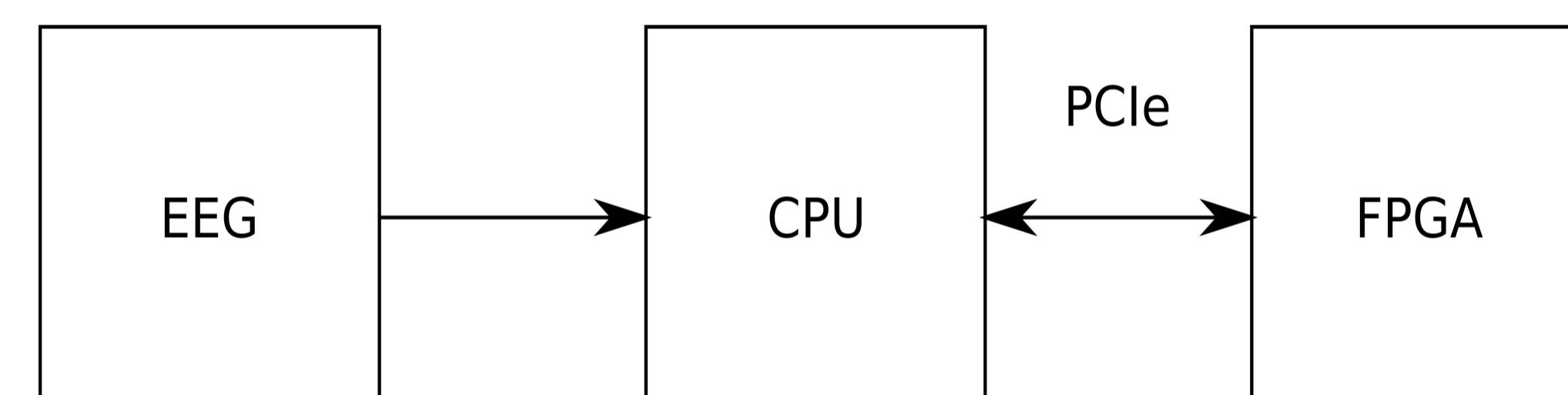


Figure 1: Representation of the accelerated system

## Hardware acceleration

- PCIe Gen.2 link with RIFFA project [1], for a Virtex-7 690T FPGA
- **Dedicated architectures** for non-linear functions (i.e: [2])
- Fixed-point and **totally pipelined computation**
- Maximisation of the throughput:
  - Optimisation of DSP cells usage
  - Preventing BRAMs usage

[1] M. Jacobsen, D. Richmond, M. Hogains, and R. Kastner. Riffa 2.0 : A reusable integration framework for fpga accelerators. ACM Transactions on Reconfigurable Technology and Systems (TRETs), 2015

[2] E. Libessart, M. Arzel, C. Lahuec, and F. Andriulli, 'A Scaling-Less Newton-Raphson Pipelined Implementation for a Fixed-Point Reciprocal Operator', IEEE Signal Processing Letters, vol. 24, no. 6, pp. 789-793, Jun. 2017.

	Max frequency
DSP48E1	740 MHz
BRAM	601 MHz

Table 1: Maximal frequency comparison between DSP cell and BRAM for the Virtex-7 690T FPGA

## Conclusion and future work

- Usual BCIs using EEG lack of accuracy
  - Transition from a surface to a volume model
  - Dramatical increase of the computation load
- Acceleration by FPGA, through a PCIe Gen.2 link
- Potential acceleration by 530
- Possibility to use new PCIe generations
- Possibility to use floating-point IP provided by Xilinx and Intel FPGA