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Mathieu Moreau, Daniela Munteanu, Jean-Luc Autran, Florence Bellenger, Jérôme Mitard, et al.. Quantum Simulation of C-V and I-V Characteristics in Ge and III-V Materials/High- κ MOS Devices. MRS Online Proceedings Library, 2009, 1194, pp.1194-A02-02. <10.1557/PROC-1194-A02-02>. <hal-01745840>

HAL Id: hal-01745840

<https://hal.science/hal-01745840v1>

Submitted on 16 Jul 2018

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Quantum Simulation of C-V and I-V Characteristics in Ge and III-V Materials/High- κ MOS Devices

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ABSTRACT

We present a one-dimensional simulation study of the capacitance-voltage (C-V) and current-voltage (I-V) characteristics in MOS devices with high mobility semiconductors (Ge and III-V materials) and non-conventional gate stack with high- κ dielectrics. The C-V quantum simulation code self-consistently solves the Schrödinger and Poisson equations and the electron transport through the gate stack is computed using the non-equilibrium Green's function formalism (NEGF). Simulated C-V characteristics are successfully confronted to experimental data for various MOS structures with different semiconductors and dielectric stacks. Simulation of I-V characteristics reveals that gate leakage current strongly depends on gate stacks and substrate materials and predicts low leakage current for future CMOS devices with high mobility materials and high- κ dielectrics.

INTRODUCTION

In order to improve complementary metal-oxide-semiconductor (CMOS) technology performances for future technological nodes (sub 22-16 nm), high mobility (high- μ) semiconductors with high permittivity (high- κ) dielectric-based gate stacks have been recently considered to replace the historical SiO₂/Si structure [1].

Due to low values of the carrier conductivity effective masses in both valence and conduction bands, which leads to higher hole and electron mobilities than in Si, Ge and III-V materials are seriously considered in recent works to respectively enhance p-MOSFET and n-MOSFET performances, especially the on-state current in high-performance logic applications. Moreover, the introduction of high- κ dielectrics can reduce tunneling current through the gate stack while maintaining control of the current in the channel by the gate even for structures with very low equivalent oxide thickness (EOT) [2].

However, the fabrication of high- κ /Ge (or III-V) devices in terms of surface passivation between gate oxide and channel material is still not well controlled and remains a challenge to meet ITRS roadmap requirements. Over the past few years, countless techniques and materials have been used to manufacture devices (GeO₂ [3-5], La₂O₃ [6], Ga₂O₃(Gd₂O₃) [7], Al₂O₃ [8], HfO₂/SiO₂/Si [9], HfO₂ [10]); all these technologies lead to complicated structures with multi layer gate stacks, for which it is difficult to precisely extract key parameters and predict future performances.

In this context, we present a one-dimensional (1D) simulation study of capacitance-voltage and current-voltage characteristics in MOS devices with high- μ channel materials and multi layer high- κ gate stacks. We self-consistently solve Poisson and Schrödinger equations to compute the

quantum carrier density and we use it to calculate the capacitance and the gate leakage current as a function of the applied gate voltage.

The simulation code is based on the 1D self-consistent numerical solving of the Poisson and Schrödinger equations coupled with the computation of the high/low frequency capacitance and the calculation of the gate current in MOS devices.

Once the Schrödinger-Poisson system is solved, the resulting quantum carrier density in the substrate is used for calculating the low and high-frequency capacitance of the structure [12]. The gate current density is evaluated from the 2D carrier gas in the inversion regime using the formalism presented in [13,14], where the carrier transmission probability is calculated with the Wentzel-Kramers-Brillouin (WKB) classical approximation.

Figure 1. Schematic band diagram of a MOS structure (p-type semiconductor) for $V_G > 0$ and the main physical parameters used in the simulation (listed in Table I). The discretization of the 1D structure using a uniform mesh in oxides and non-uniform mesh in semiconductor is also represented.

The main material parameters used in simulations are presented in Table I. It is important to note that these constants (dielectric constant, effective mass...) strongly depend on the fabrication process and are not exactly known, especially for dielectric materials. Thus, the values in the simulation code can be adapted in order to improve the fit between experimental and simulation results.

Table I. Main material parameters [3,18,19] of different semiconductors and dielectric materials used for MOS device simulation. The band offsets between oxides and semiconductors (not shown here) are the same as in reference [20] except for Ge/GeO₂ interface [18].

Materials	Physical Parameters (300 K)						
	E _G (V)	ϵ/ϵ_0	$m_{e,j}^*/m_0$ (g _i)	$m_{e,i}^*/m_0$ (g _i)	m_{hh}^*/m_0	m_{lh}^*/m_0	m_{so}^*/m_0
Si	1.12	11.8	0.916 (2)	0.19 (4)	0.20	0.291	0.29
Ge	0.66	16.0	0.949 (4)		0.044	0.28	0.084
GaAs	1.424	10.9	0.063 (1)		0.082	0.51	0.15
GaSb	0.726	14.4	0.041 (1)		0.050	0.40	0.14
InP	1.34	9.61	0.080 (1)		0.089	0.60	0.17
InAs	0.354	12.3	0.014 (1)		0.026	0.41	0.16
InSb	0.17	15.7	0.014 (1)		0.015	0.43	0.19
SiO ₂	9.0	3.9	0.5				
GeO ₂	4.3	6.7	0.5				
Al ₂ O ₃	6.1	9.0	0.35				
HfO ₂	5.6	20.0	0.17				

RESULTS AND DISCUSSION

We first illustrate C-V characteristics by comparing, in figure 2, our simulated results and experimental data [3] for high-frequency curves in two different double-layer gate stacks with a p-doped Ge substrate. Simulated and experimental data are in good agreement in depletion and accumulation regimes, which show the possibility to use the simulated curves to extract oxide material parameters such as dielectric constant, interfacial layer physical thickness and flat-band voltage [12].

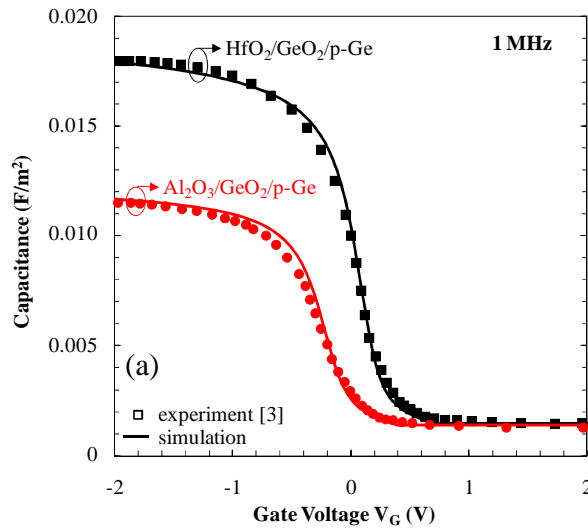


Figure 2. Comparison between experimental data [3] (symbol) and simulated (line) C-V curves for HfO₂/GeO₂/p-Ge (black, $\Phi_M = 4.83$ eV) and Al₂O₃/GeO₂/p-Ge (red, $\Phi_M = 4.50$ eV) MOS structures ($N_A = 10^{17}$ cm⁻³, $T_{HfO_2} = T_{Al_2O_3} = 4.0$ nm, $T_{GeO_2} = 1.4$ nm).

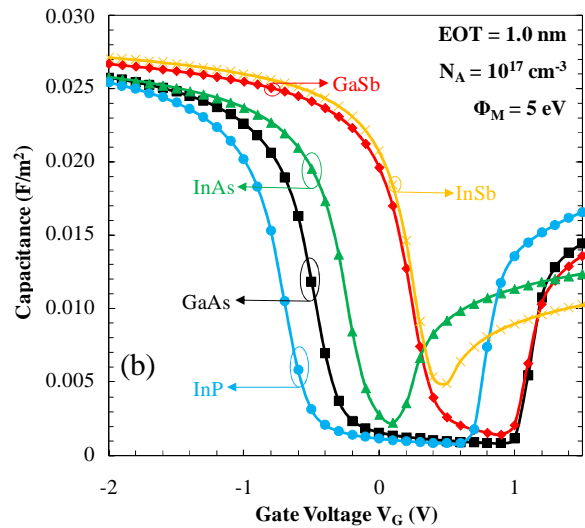


Figure 3. Simulated C-V characteristics for five different III-V p-doped semiconductors ($N_A = 10^{17}$ cm⁻³) with an Al₂O₃ gate dielectric layer of 2.3 nm (EOT = 1.0 nm) and $\Phi_M = 5$ eV (fixed for all structures).

We have also adapted our simulation code to calculate C-V characteristics for different III-V semiconductors. Figure 3 compares simulation results for various Al_2O_3 /III-V materials MOS devices ($T_{\text{Al}_2\text{O}_3} = 2.3$ nm, i.e. $\text{EOT} = 1.0$ nm) for which the gate work function is equal to 5 eV for all structures. We can see in this figure that the depletion zone strongly depends on the semiconductor bandgap, i.e. smaller is the bandgap and shorter is the depletion zone thickness (in terms of gate voltage). Moreover, the very low effective density of state in the conduction band of III-V semiconductors is clearly evidenced in inversion regime, which leads to low capacitance values in C-V characteristics.

Figures 4 and 5 show the I-V curves of the structures related to figures 2 and 3, respectively. The gate current curves in double-layer gate stacks with Ge substrate (figure 4) show very low values principally due to a large physical thickness of high- κ layer (HfO_2 and Al_2O_3), which strongly reduces the tunneling current. The gate current in experimental devices (not shown here) seems to be higher probably due to different additional conduction mechanisms, such as trap-assisted conduction in the high- κ layer (which is not taken into account in our simulation code). However, we observe that the conduction band offset between the two oxide layers is one of the main parameters influencing the gate leakage tunneling current. Indeed, the conduction band offset between Al_2O_3 and GeO_2 is higher than the case between HfO_2 and GeO_2 [18], which leads to higher gate current for $\text{Al}_2\text{O}_3/\text{GeO}_2$ structure. We also show in figure 5 (the gate current of structures of figure 3 is plotted) that the substrate material is also crucial to reduce the gate current. In other words, semiconductors with very low bandgap (InAs or InSb) give high currents (besides we do not take into account band-to-band tunneling, which will additionally increase the current) whereas GaAs and InP seems to be very promising substrate materials in terms of low leakage current.

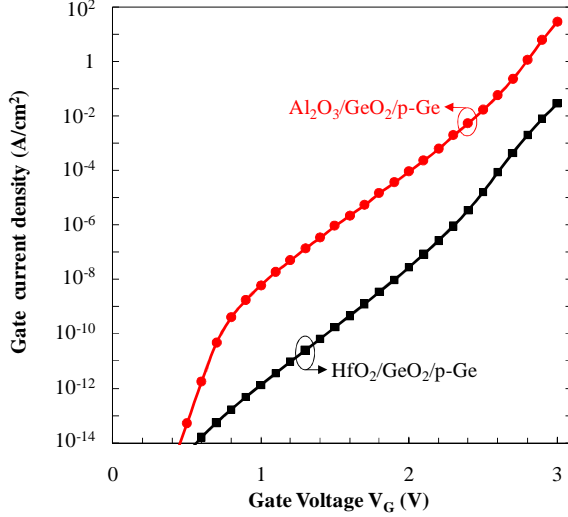


Figure 4. Simulated I-V characteristics for the same devices as figure 2.

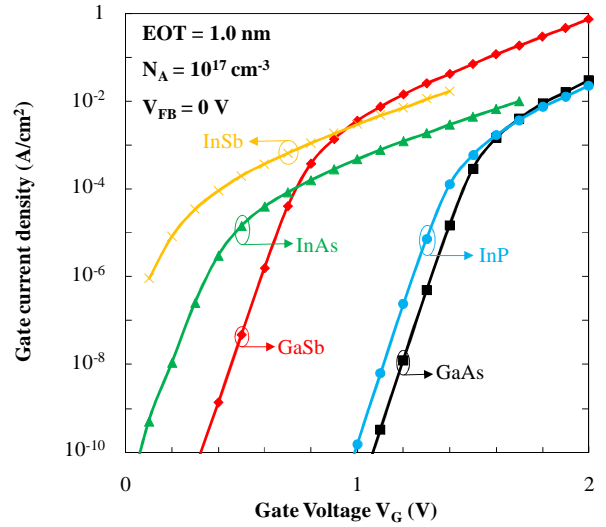


Figure 5. Simulated I-V characteristics for the same devices as figure 3. In this figure, V_{FB} is fixed at 0 V for all structures.

In order to study the influence of oxide material parameters, we now present results concerning MIM capacitors using a full quantum-mechanical calculation (NEGF formalism). Figure 6 compares the tunneling transmission probability through the gate stack between NEGF and WKB calculations for a double-layer gate stack [SiO_2 (6 Å) + HfO_2 (20.5 Å)]. We can

observe that classical (WKB) and quantum (NEGF) calculation lead to significant differences between the two transmission curves due to strong potential discontinuities (metal/insulator and insulator/insulator band offset) [16]. The quantum reflections are clearly revealed when the energy-resolved LDOS is plotted (insert of figure 6). The LDOS structure presents a subband energy splitting similar to those corresponding to a quantum well, formed by the barrier discontinuities at the insulator boundaries. The peaks in the transmission probability correspond to a resonant tunneling condition due to a reinforced DOS at the considered energy levels [16,17].

We finally plot, in figure 7, the evolution of gate current density as a function of EOT for different MIM structures at $V_G = 1$ V. From these results, we clearly see that the gate current depends on several parameters such as oxide band offsets or dielectric constants. The best way to reduce the leakage current seems to be using dielectric materials with a high permittivity value and a very low band offset between the high- κ and interfacial layers. One can also observe that simulated double-layer gate stacks always give better results than the single SiO_2 layer.

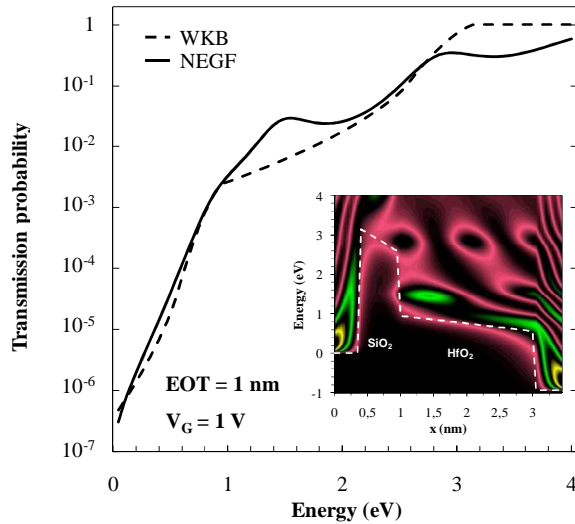


Figure 6. Carrier transmission probability calculated using WKB and NEGF formalisms as a function of energy in MIM capacitor with a double-layer gate stack SiO_2 (6 Å) + HfO_2 (20.5 Å). The insert show energy-resolved LDOS and energy band diagram.

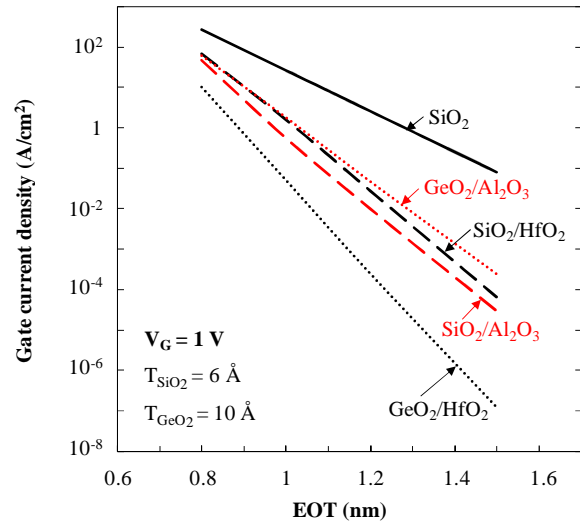


Figure 7. Calculation of gate current density (NEGF formalism) vs EOT for different MIM devices [SiO_2 , SiO_2 or GeO_2 + HfO_2 (long dash), SiO_2 or GeO_2 + Al_2O_3 (short dash)] with $T_{\text{SiO}_2} = 6$ Å or $T_{\text{GeO}_2} = 10$ Å in double-layer gate stacks at $V_G = 1$ V.

CONCLUSION

We developed a 1D numerical simulation code for the calculation of the C-V and I-V characteristics of MOS devices with high- μ materials and high- κ gate stack. The code self-consistently solves the Schrödinger and Poisson equations and the resulting quantum carrier density in the substrate is used to calculate the capacitance of the structure. The electron transport through the gate stack is treated using the NEGF formalism. Comparison with C-V experimental data shows that the code can be used to extract the value of key parameters in MOS structures with arbitrary multi layer high- κ gate stacks. Simulation of I-V characteristics reveals

that gate leakage current strongly depends on gate stacks and substrate materials. These results also predict promising performances in terms of low leakage current confirming the possibility of enhancing CMOS performances with high- μ materials and high- κ gate stacks.

ACKNOWLEDGMENTS

This work was supported by the CNRS International Project of Scientific Collaboration (PICS) between IM2NP, Marseille, France and IMEC, Leuven, Belgium.

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