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Design Challenges for Prototypical and Emerging Memory Concepts Relying on Resistance Switching

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Abstract—Integration of functional materials in memory architectures led to emerging concepts with disruptive performances as compared to conventional charge storage technologies. Beside floating gate solutions such as EEPROM and Flash, these alternative devices involve voltage or current-controlled switching mechanisms between two distinct resistance states. The origin of the resistance change straightforwardly depends upon the nature and fundamental physical properties of functional materials integrated in the memory cell. After a general overview of non volatile memories, this paper is focused on prototypical and emerging memory cells and on their ability to withstand a downscaling of their critical dimensions. In addition, despite different maturity levels, a peculiar attention is turned toward common guidelines helpful for designing embedded or distributed resistive switching memory circuits.

Keywords—Prototypical and emerging memory concepts; resistance switching; operation mechanisms; memory design; embedded or distributed memory circuits.

I. OVERVIEW

Currently, the microelectronic industry is facing new technological challenges for continuously improving performances of memory devices in terms of access time, storage density, endurance or power consumption. The major bottleneck to overcome is the downsizing of memory cell dimensions necessary to integrate a larger number of elementary devices and subsequently more functionalities on a constant silicon surface. This drastic size reduction is constrained, in particular, by the intrinsic physical limits of materials integrated in the memory architecture.

Beside volatile random access memories (RAM) such as Dynamic (DRAM) or Static (SRAM), non volatile memory technologies may be subdivided in two categories depending upon the mechanism used to store binary data. A first group of solid state devices is based on charge storage in a polysilicon floating gate. In this family, gathering usual EEPROM and Flash technologies [1], new concepts or architectures are required to satisfy CMOS “More Moore” scaling trends. For instance, $\text{Si}_{1-x}\text{Ge}_x$ “strained silicon” technology enables boosting the charge carrier mobility and discrete charge trapping improves data retention and enables an extension towards “multi-bits” storage. Presently, Flash technology still remains the undisputed reference, regardless of its NAND (dense and cheap) or NOR (fast) architecture. However, as the scaling of the conventional floating gate

cell becomes ever more complicated below 32 nm node, opportunities for alternative concepts are rising. In the last two decades, several major semiconductor Companies have explored new solutions integrating a functional material, whose fundamental physical property enables data storage.

Older technology, called FRAM for Ferroelectric RAM [2], is in small volume production for several years by Fujitsu and Texas Instruments which license Ramtron patents. With their DRAM-like architecture FRAM memories integrate ferroelectric capacitors that permanently store electrical charges. Thanks to their low voltage operations, fast access time and low power consumption, FRAM devices mainly address “niche” applications such as contactless smart cards, RFID tags and nomad devices.

Excluding FRAM technology, recent R&D efforts also led to a new class of disruptive technologies based on resistive switching mechanisms. These memories, presenting two stable resistance states controlled by an external current or voltage, attract much attention for future solid state devices. The physical origin of the resistance change depends upon the nature and fundamental physical property of materials integrated in the memory cell. As a result, a broad panel of new concepts is currently rising: magnetoresistive memories (MRAM) and derived concepts; phase change memories (PCM); resistive memories (RRAM) including oxide resistive (OxRRAM) and “nanoionic” memories (CBRAM and PMC) [3]. As compared to other technologies, PCM and RRAM memories are more favourably positioned as alternatives to Flash for sub-22 nm nodes. Nevertheless, these two technologies have different maturity levels: while first PCM products are available (e.g. Omneo™ by Micron, former Numonyx), RRAM memories are still at early R&D stage. Following 2010 ITRS’s report, MRAM, PCM and FRAM are categorized as “prototypical” memories whereas RRAM is an “emerging” memory [4].

Hence, alternative non volatile memory concepts, either evolutionary or revolutionary, are being explored to satisfy the need for higher storage capacity and better performances. Within a broad panel of innovative solutions, this review specifically addresses resistive switching technologies. After a brief description of memory cells and their ability to withstand downscaling of their critical dimensions, peculiar attention is turned toward common guidelines helpful for designing embedded or distributed memory circuits.

II. MEMORY MARKETS FOR RESISTIVE TECHNOLOGIES

To penetrate the markets currently covered by SRAM, DRAM and Flash memories, prototypical and emerging concepts are facing stringent requirements of process compatibility and scalability at material, device and circuit levels. Status and outlook may be proposed as follows:

- MRAM arising from spintronics may be viewed as a credible candidate to replace existing technologies in many applications requiring standalone or embedded solutions combining Flash-like non volatility, SRAM-like fast nanosecond switching and DRAM-like infinite endurance. For future, “Spin Torque Transfer” (STT-MRAM) concept appears as a promising technology able to merge aforementioned advantages and scalable for aggressive technological nodes (*cf.* §III).
- PCM is probably the most advanced alternative memory concept in terms of process maturity, storage capacity and access time. Furthermore, the phase change memory element exhibits an excellent ability to withstand a downsizing of its critical dimensions. Considering limitations in terms of high reset current and low performances in retention, PCM is rather positioned as a NOR Flash substitute. Nevertheless, it may be also envisaged to rethink PCM subsystem architecture to bring the technology within competitive range of DRAM. To exploit PCM’s scalability as a DRAM alternative, new design solutions are expected to balance long latencies, high energy writing and finite endurance [5].
- RRAM concept is in an earlier stage of development compared with MRAM and PCM. Since RRAM memory elements can be integrated into Back-End Of Line (BEOL), this technology is of particular interest for high density storage with possibly multi-levels three-dimensional architectures. Metal-organic complex-based RRAM [6], transition metal oxide (TMO) based Ox-RRAM [7,8] and chalcogenide-based CBRAM appear as promising candidates [9]. However, retention and endurance still remain to be demonstrated for CBRAM devices, while the high reset current is an issue in TMO-based memory devices. As a consequence, RRAM concepts, still in their infancy, require further academic and industrial investigations (i) to validate integration and scalability capabilities; (ii) to uncover the physical origin of resistance switching which remains sometimes controversial; (iii) to model the reliability.

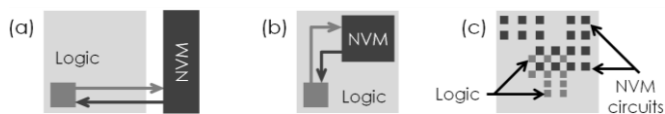


Figure 1. Circuit/architecture of non volatile systems: (a) Conventional implementation with logic block and standalone non volatile memory (NVM) on separated chips. This configuration enables integrating separately optimized technologies but requires tradeoffs in terms of cost and communication speed between chips. (b) Embedded implementation with NVM and logic block on a single monolithic substrate. (c) Implementation with distributed NVM circuits on a single chip.

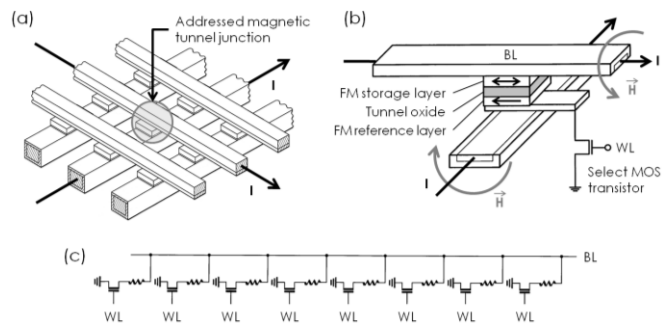


Figure 2. (a) To write MRAM bit, currents are passing through perpendicular metal lines surrounding MTJ. (b) The resultant magnetic fields enable programming a bit in reversing magnetization of upper FM storage layer (select MOS transistor is OFF). To read a bit, a current is passing through the MTJ and its resistance is sensed (select MOS transistor is ON). (c) Schematic diagram of series-parallel architecture for 1T/1MTJ cells.

Beside conventional standalone (Fig. 1a) and embedded (Fig. 1b) memories, emerging resistive concepts also enable designing innovative electronic functions such as field programmable gate array (FPGA) or logic devices (*e.g.* Flip Flop) in which non volatile memory circuits are distributed over a single chip (Fig. 1c). This latter distributed implementation requires CMOS compatible, low cost, low voltage and low power non volatile memory elements.

Before investigating novel architectures, it is of primary importance to develop design kits compatible with microelectronics design suites like Cadence or Mentor. Design kits dedicated to memories require first compact models describing cell’s properties and verification tools that enable designing and checking the circuit layout [3].

III. MAGNETORESISTIVE MEMORIES, MRAM

In magnetoresistive devices, data are no longer stored by electrical charges, as in semiconductor-based memories, but by a resistance change of a complex magnetic nanostructure [10]. MRAM cells integrate a magnetic tunnel junction (MTJ) consisting of a thin insulating barrier (*i.e.* tunnel oxide) separating two ferromagnetic (FM) layers. Using lithographic processes, junctions are etched in the form of sub-micron sized pillars connected to electrodes. In conventional FIMS (Field Induced Magnetic Switching), each MTJ is located at the intersection of two perpendicular metal lines (Fig. 2a). MTJ resistance depends upon the relative orientation of magnetizations in the two FM layers: the magnetization in FM reference layer is fixed whereas the one in FM storage layer is switchable (Fig. 2b). Magnetization reversal in FM storage layer is controlled by two external magnetic fields produced by currents injected in the surrounding metal lines. Tunnel magneto-resistance (TMR) is due to tunnelling of electrons through the thin oxide layer sandwiched between two FM films having either antiparallel (high resistance state “0”) or parallel (low resistance state “1”) magnetizations.

In MRAM technology three major issues are identified: (i) low resistance discrimination between “0” and “1” states (*i.e.* small sensing margin); (ii) high sensitivity to disturb

during writing (“bit fails”); (iii) high currents (few mA) required for magnetization reversal. To overcome these issues, different solutions are proposed:

- To enlarge the sensing margin, the tunnel barrier in amorphous aluminium oxide AlO_x of first device generations was progressively replaced by crystallized magnesium oxide MgO .
- Everspin Company (former Freescale), world’s first volume MRAM supplier, already sells a 4, 8 and 16 Mb MRAM chips based on 180 nm CMOS technology and relying on the “Toggle” concept to limit disturbs during writing [11]. Thanks to a new free layer magnetic nanostructure called “synthetic antiferromagnet” (SAF), an appropriate bit orientation and a current pulse sequence, MRAM cell bit state is programmed *via* Savtchenko switching. In that configuration, a single metal line alone cannot switch the bit, providing greatly enhanced selectivity over the conventional FIMS MRAM.
- In October 2010, French startup Crocus Technology and TowerJazz completed the first stage integration of “Thermally-Assisted” MRAM into 130 nm CMOS platform. In TA-MRAM cell, a current injected in MTJ during writing induces a Joule heating in FM layers and the subsequent temperature increase facilitates the magnetization reversal [12]. TA-MRAM concept enables (i) shrinking the memory cell size with only one metal line to produce magnetic field; (ii) reducing the power consumption thanks to limited writing current; (iii) improving bit fails immunity.
- More recently, STT (“Spin Torque Transfer”) switching was proposed to solve aforementioned issues and make MRAM memory compatible with more aggressive nodes. Large Companies (*e.g.* Renesas, Hynix, IBM, Samsung...) and few startups (*e.g.* Grandis, Avalanche, Everspin, Crocus...) are actively working on this new concept and state they can push the integration limits beyond 45 and 65 nm nodes for standalone and embedded memories respectively [13]. In STT writing mode a spin-polarized current, which flows through MTJ, exerts a spin torque on the magnetization of FM storage layer [14]. Technologically, STT concept requires the integration of a polarizer to select the spin of electrons injected into the magnetic nanostructure and ensuring the magnetization reversal. As compared to conventional MRAM cells, STT-RAM solution is said to consume less power, to improve bit selectivity and to reduce the memory cell size to approximately $6\text{-}9\text{ F}^2$.

Similarly to DRAM, EEPROM or NOR Flash memories and whatever the writing mode (Toggle, TA or STT), MRAM core-cell is based on the association of 1 select MOS transistor with 1 magnetic junction (*i.e.* 1T/1MTJ). To individually access each memory cell, magnetic tunnel junctions are located at each intersection of a bottom “Word Line” (WL) connected to the transistor gate and an upper “Bit Line” (BL) (Fig. 2c). In contrast to multi-layer structure

proposed for RRAM technology, such 1T/1MTJ cells disable stacking memory layers due to disturbs between neighbouring cells during magnetic field-assisted writing.

Polarization of “Word”, “Bit” and “Source” (SL) lines used to select one core-cell in the memory matrix straightforwardly depends on the writing mode. In TA-MRAM, writing requires a heating current injection in MTJ obtained in applying a positive voltage on the gate of the select transistor (WL) of the addressed core-cell whereas the source line is grounded. Concomitantly, a current is injected in single metal line (BL) to create a magnetic field that enables switching of FM storage layer. In STT writing mode, a positive voltage is applied on the select transistor gate (WL) of the addressed cell [15]. Since writing does not require magnetic field, only bipolar voltage is applied between BL and SL to inject a top-down or bottom-up spin polarized current enabling magnetization reversal.

Beside memory architectures, TA [16] or STT [17] MTJs may be also integrated in reconfigurable FPGA. Using a heterogeneous design there is no need to load the configuration data from an external non volatile memory as required in SRAM-based FPGA. Non volatility enables reducing both power consumption and configuration time required at each start-up of the circuit in comparison with classical static random access memory-based FPGAs.

IV. PHASE CHANGE MEMORIES, PCM

Since the 1970s, chalcogenide phase change materials attract much attention for data storage applications [18], particularly in rewriteable optical media such as compact, digital versatile or more recently Blu-ray discs. In addition, they offer a great potential for non volatile phase change memories abbreviated as PCM [19,20]. This concept exploits the resistance change (few orders of magnitude) due to reversible amorphous (state “0”) to crystalline (state “1”) phase transitions. As depicted in Fig. 3, to reach amorphous state (*i.e.* reset operation), GST material is heated above the melting temperature T_M (typically $600\text{-}700^\circ\text{C}$) and then rapidly cooled. In contrast, GST material is placed in the crystalline state (*i.e.* set operation) when “slowly” (few tens of ns) cooled from a temperature in between melting point T_M and crystallization temperature T_X (Fig. 3).

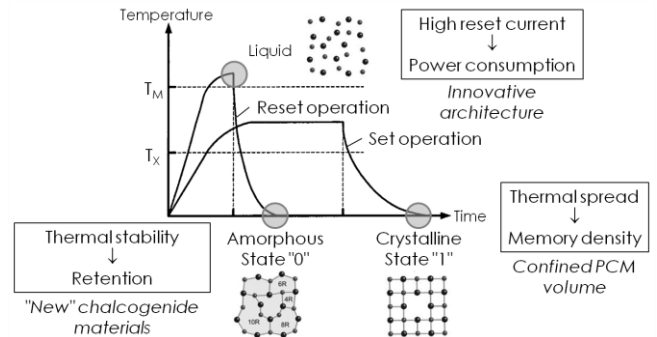


Figure 3. Temperature profiles used for set and reset operations in PCM. Innovations are mandatory to improve data retention, reduce power con-

sumption and increase memory density.

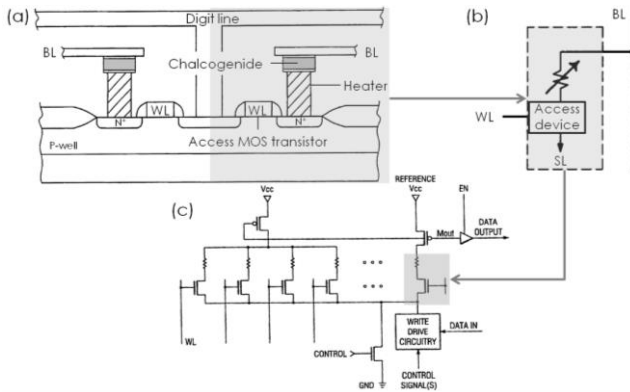


Figure 4. (a) Conventional PCM architecture in which two adjacent memory cells are coupled to a common digit line. Access MOS transistor driven by a word line WL is connected to phase change element through a conductive plug acting as a "heater". (b) 1 access device/1 resistor memory cell. (c) Electrical schematic arrangement of a PCM memory array.

Technologically, a layer of chalcogenide alloy (*e.g.* $\text{Ge}_2\text{Sb}_2\text{Te}_5$, GST) is sandwiched between top and bottom electrodes: the phase change is induced in GST programmable volume through an intense local Joule effect caused by a current injected from bottom electrode contact acting as a "heater" (Fig. 4a). As illustrated in Fig. 3, improvement of PCM performances needs to overcome three main issues:

- Design innovative cell architectures that enable reducing reset current which remains quite high in existing prototypes (typically 0.5 mA).
- Propose new chalcogenide materials exhibiting a higher crystallization temperature to improve data retention (spontaneous amorphous-to-crystalline transition) and crystallizing rapidly to decrease switching time.
- Fabricate confined phase change volume to limit heat spread toward neighbouring cells during reset operation.

As compared to MRAM technology, PCM memories have a better ability to withstand size reduction. Indeed, although the endurance is still limited (less than 10^{10} cycles), the memory cell is much more compact (typically 10 F^2) and downsizing should be extended beyond 25 nm node by shrinking programmable volume. PCM is rather positioned as a NOR Flash substitute: on this market segment, PCM technology displays significant improvements in terms of endurance, access time and bit alterability (*i.e.* state switching without intermediate erase operation required in floating gate technologies).

PCM technology basically uses 1X/1R core-cells (Fig. 4b), X being one access device associated with one phase change resistor R. As shown in Fig. 4c, each core-cell is addressed thanks to WL connected to access device, BL and SL. Considering the high reset current required to switch chalcogenide material from crystalline to amorphous phase, access device must be able to drive high current during this operation. Access may be controlled by a bipolar junction transistor (BJT) [21], a diode [22] or a MOS transistor [23].

Dedicated peripheral circuits have to be designed to write

and read data in PCM memory cell: during writing, access device injects current into the storage material and thermally induces phase change, which is detected during reading. Contrary to MRAM concept, a special emphasis is required on write drivers. The time-dependent temperature profiles used to switch chalcogenide material have to be carefully controlled through the monitoring of set and reset currents injected in the programmable volume. For instance, Woo Yeong Cho *et al.* have proposed a solution based on a current mirror source belonging to a local column constituted of 1NTMOS/1R cells [20]. The main advantage of such a structure is the reuse of the current source for all columns through the entire memory chip. For read operations, PCM memory circuits require sense amplifier able to discriminate the two resistance states. As compared to MRAM devices, the resistance margin ΔR is larger (at least 1 decade) and constraints on sense amplifier are slightly relaxed. Bedeschi *et al.* have proposed a solution based on current measurement mode implemented in 8 Mb PCM memory matrix using a BJT as selector [24]. Current passing through the cell is measured thanks to a mirror biased structure and the current is compared to a reference 1BJT/1R dummy cell.

V. REDOX MEMORIES, RRAM

Last ten years have seen the emergence of new memories labelled as RRAM for Resistive RAM and based on various mechanisms of resistance switching excluding phase change as used in PCM (*cf.* §IV). In its simplest form, RRAM element relies on MIM structures (Metal/Insulator/Metal) whose conductivity can be electrically switched between high (state "0") and low (state "1") resistance states (Fig. 5a). RRAM memory elements are gaining interest for (i) their intrinsic scaling characteristics compared to the floating gate Flash devices; (ii) their potential small size; (iii) their ability to be organized in dense crossbar arrays (Fig. 5b). Hence, RRAM concept is seen as a promising candidate to replace Flash memories at or below 22 nm technological nodes.

Following the latest ITRS classification published in 2010 on "Potential and Maturity of Selected Emerging Research Memory Technologies" [4], different "flavours" of RRAM memory elements are disclosed depending on the mechanism involved in the resistance change [25,26].

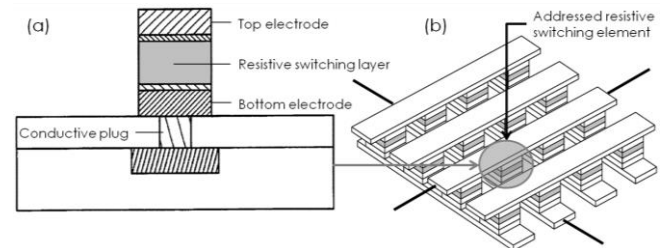


Figure 5. (a) Scheme of typical RRAM memory element: resistive switching layer is sandwiched between top and bottom electrodes to form simple MIM (Metal/Insulator/Metal) structures. (b) Crossbar-type memory architecture in which memory elements are located at the intersections of per-

pendicular metal lines.

In the ITRS's report, all RRAM concepts are categorized as "Redox RAM" that encompasses a wide variety of MIM structures and materials sharing reduction/oxidation (*i.e.* redox) electrochemical processes [26]. Redox mechanisms can operate in the bulk I-layer, along conductive filaments formed within the I-layer, and/or at the I-layer/metal contact interfaces in MIM structure. The following sub-categories are proposed:

- In "Fuse/anti-fuse" memories, the resistance switching is driven by local reduction/oxidation mechanisms leading to formation/dissolution of conductive filaments within a transition metal oxide [7,8,25,26]. Operations do not depend upon applied voltage polarity (unipolar switching).
- In "valence change mechanism", the resistance switching relies on redox electrochemistry that changes the conductivity of the I-layer. Field-induced oxygen vacancies drift plays a predominant role in few specific oxide-based memory elements: TiO₂-based "Memristors" [27] recently demonstrated by Hewlett-Packard Company; CMO_xTM elements developed by Unity Semiconductor [28]; NiO layers obtained from nickel oxidation in small via structures [29-31]. Memory operations require polarity reversal (*i.e.* bipolar operations).
- CBRAM ("Conductive Bridge RAM") [32] and PMC ("Programmable Metallization Cells") [9] belong to "nanoionic" memories. MIM-like memory elements consist in an inert electrode (W, Pt ...), an ionic conductor used as solid electrolyte (WO₃, MoO₃, GeSe, Ag-GeSe...) and an active electrode (Ag, Cu...) producing, through an electrochemical reaction, ions (Ag⁺, Cu⁺...) drifting within solid electrolyte. For this type of mechanism, a polarity change of applied voltage is mandatory (*i.e.* bipolar operations).

As previously underlined, RRAM memories are still in a R&D stage and only few memory circuits have been published in the literature. As memory elements may be integrated into BEOL, RRAM technology is of particular interest for high density storage with possibly multi-levels three-dimensional architectures (Fig. 6a) [33,34]. Nevertheless, it has to be stressed out that from a memory cell and array design point of view, unipolar operations are preferred over bipolar operations.

For this promising class of memories, two cell architectures are generally proposed depending on the nature of RRAM element: 1T/1R (*i.e.* one transistor associated with one resistive element) for CMOS-based active matrix; 1R enabling crossbar-type memory passive matrix. The first demonstrators integrated memory cells with size of 4-8 F² for active matrix and (4/n) F² for a passive matrix (*i.e.* crossbar) with *n* storage layers [25,32]. Nevertheless, in passive crossbars, the memory elements cannot be electrically isolated while neighboring cells are addressed. This problem can be solved by adding serial elements with a specific (high) non-linearity (*e.g.* diode as shown in Fig. 6b)

at each resistively switching cell, depending on the resisting properties and the array size.

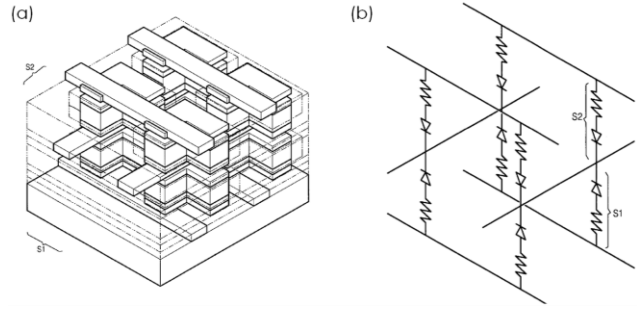


Figure 6. Three-dimensional view (a) and schematic (b) of a two-layer crossbar memory array integrating 1 diode/1 resistor (1D/1R) core-cells. 1D/1R cell enables isolating a memory element while neighbouring cells are addressed.

Samsung Company already demonstrated a "non-CMOS" solution with a two-layer architecture based on 1D/1R memory cells associating a diode with a nickel oxide-based resistive element exhibiting unipolar switching [35]. Such a crossbar memory matrix was easily designed with the help of BL and WL to access each cell individually.

CBRAM derives from parent technology PMC, which was developed by Axon TC in collaboration with Arizona State University. In 2007, Qimonda/Altis/Infineon consortium demonstrated a 2 Mb CBRAM test chip with read-write control circuitry implemented in a 90 nm technological node with read/write cycle time less than 50 ns [36]. The corresponding CBRAM circuit was developed using 8 F² core-cells associating 1 MOS transistor with 1 Conductive Bridging Junction (*i.e.* 1T/1CBJ). The chip design was based on a fast feedback regulated CBJ read voltage and on a novel program charge control using dummy cell bleeder devices. It has to be mentioned that Adesto startup has acquired intellectual property and patents related to CBRAM technology from Qimonda in October 2010. In addition, Adesto announced in November 2010 a manufacturing partnership with Altis Semiconductor.

The low power resistive switching at voltages below 1 V, the ability to scale to minimum geometries below 20 nm and the multi-level capability make CBRAM a very promising non volatile emerging memory technology. Nevertheless, as compared to prototypical MRAM, FRAM and PCM memories, CBRAM concept requires refresh operations due to the poor retention capability in low resistance state (contrary to the high resistive state which is usually much more stable in time). Thus, a refresh voltage is applied to the CBRAM memory element at a predetermined time to strengthen and stabilize low resistance state. This smart refresh enables preserving the resistance margin ΔR necessary to unambiguously discriminate high and low resistance states during read. This refresh is performed without destroying data stored in CBRAM element whereas in DRAM a rewriting of respective state is mandatory.

To conclude, RRAM technology is very promising and once again many design solutions exist for implementation.

However, depending on RRAM concept, specific peripheral circuits are required to guaranty reliable memory operations.

VI. TWO GUIDING PRINCIPLES

For both prototypical (MRAM, PCM) and emerging (RRAM) technologies, two guiding principles are shared for designing generic resistive switching memory circuits:

- The first guideline is related to the implementation of bistable resistive elements in a memory array. In most of cases, memory cells rely on the association of a select/access device with a resistive element. Depending on the resistive concept (magnetic, phase change or redox), the select/access device can be a BJT, a MOS transistor or a diode. Even if MOS transistor is frequently preferred, access device is adapted to electrical characteristics of resistive element (set and reset currents and voltages, resistance levels, memory window...). To access each 1T/1R memory cell individually, suited bias conditions are applied to Bit (BL), Source (SL) and Word (WL) Lines of the addressed cell, other lines being grounded and/or floating. For illustration, Hush and Baker [37] have proposed an architecture for sensing the resistance state of a programmable conductor random access memory element (Fig. 7a). The design is based on complementary memory elements, one holding the resistance state being sensed and the other holding a complementary resistance state. A sense amplifier detects voltages discharging through high and low resistance elements to determine the resistance state.
- Resistance in “0” and “1” states represents the second common guideline (Fig. 7b). Indeed, reliable read operations require an unambiguous discrimination of low and high resistances, below and above the median resistance R_{Ref} defined as $\Delta R/2 = [R_{High} - R_{Low}]/2$. Moreover, the bit cell resistance distributions must be narrow to avoid any overlap between “0” and “1” states (*i.e.* large $\Delta R/\sigma$ ratio, with σ the distribution standard deviation). Finally, as the maximum current consumed during read operation is linked to R_{Low} , resistance in “1” state must be as large as possible to decrease overall power consumption.

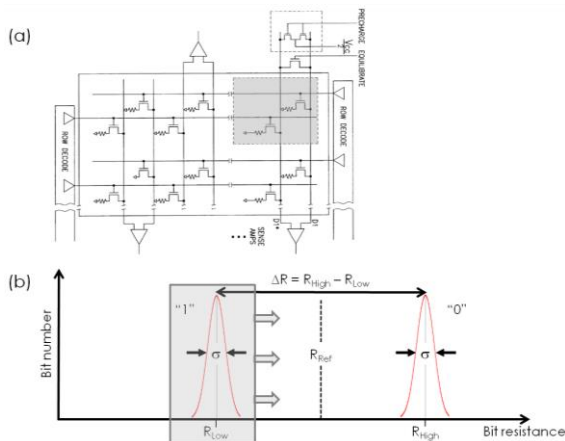


Figure 7. (a) Architecture that enables sensing the resistance state of a programmable conductor random access memory element using complementary resistive elements (dashed square). (b) Bit cell resistance distributions of “0” and “1” resistance states.

VII. CONCLUSION

In summary, reliable memory operations require a close matching between electrical characteristics of resistive elements and design rules. In other words, to reach suitable sensing margin (*i.e.* large ΔR) shifted toward high resistances altogether with narrow bit cell resistance distributions (*i.e.* low σ), it is of primary importance to:

- Control materials microstructure, critical dimensions of memory element, process variability...;
- Understand physical mechanisms explaining resistance switching;
- Develop relevant compact models to be implemented in electrical simulators.

Hence, the development of prototypical and emerging memory concepts emphasizes the necessity to make stronger links between memory cell materials and processes, modeling and circuit design.

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