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Simulation Analysis of Quantum Confinement and Short-Channel Effects in Independent Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistors

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A two-dimensional (2D) numerical simulation code of drain current including self-consistent solving of the Schrödinger and Poisson equations coupled with the drift-diffusion transport equation in double-gate (DG) metal-oxide-semiconductor field-effect transistor (MOSFET) devices has been developed. This code has been used to investigate the operation of independent DG (IDG) MOSFETs compared with classical DG MOSFETs in terms of short-channel effects (SCEs) and carrier quantum confinement. Simulations show that IDG MOSFET operation is different from that of DG MOSFETs due to the presence of a transverse electric field in the first structure that induces significant enhancement of quantum mechanical confinement. This leads to subthreshold performance degradation and to SCE enhancement in IDG MOSFETs compared with DG MOSFETs. We show that, in contrast to DG MOSFETs, quantum confinement effects must be taken into account in IDG MOSFET operation even for thick silicon films (> 10 - 15 nm).

KEYWORDS: independent double-gate MOSFETs, short-channel effects, quantum confinement effects, numerical simulation

1. Introduction

Because metal-oxide-semiconductor field-effect transistor (MOSFET) scaling is approaching its limits, double-gate (DG) MOSFETs are envisaged as a possible alternative to conventional bulk MOSFETs. Despite excellent electrical performance characteristics due to its multiple conduction surfaces, conventional DG MOSFETs allow only three-terminal operation because the two gates are tied together. DG structures with independent gates have been recently proposed[1-5], allowing a four-terminal operation. Independent DG (IDG) MOSFETs offer additional advantages, such as dynamic threshold voltage control by one of the two gates and transconductance modulation, in addition to the conventional switching operation[1,3].

In this study, we propose a two-dimensional (2D) numerical simulation code for the drain current including self-consistent solution of the Schrödinger and Poisson equations coupled with the drift-diffusion transport equation. This quantum drift-diffusion code is used to analyze the variation with the back gate bias of electrical parameters, such as threshold voltage (V_T), V_T roll-off, drain-induced barrier lowering (DIBL) effect, and subthreshold swing (S). The difference between classical (i.e., without quantum confinement) and quantum threshold voltages (ΔV_{Tq}), as a function of different silicon film thicknesses (3-10 nm) in IDG MOSFETs, is also thoroughly investigated. An extensive comparison between the IDG mode (the front and back gates are biased independently) and the DG mode (the front and back gates are tied together, i.e. conventional DG MOSFETs) is also performed to show the effects of the transverse electric field on carrier quantum confinement and subthreshold performance characteristics of IDG MOSFETs.

2. Simulation Details

2.1 Simulated devices

The IDG MOSFET considered in this study is schematically shown in Fig. 1(a). The structure is symmetric with an intrinsic thin silicon film and a highly doped source and drain regions ($N_{SD} = 3\times10^{20}$ cm^{-3}). Identical midgap metal gates ($\Phi_{mf} = \Phi_{mb} = 4.61$ eV) and front and back gate-oxide layers of 1.0 nm thickness ($T_{oxf} = T_{oxb} = T_{ox}$) have been also considered. The front and back gates are biased with V_{Gf} and V_{Gb}, respectively. In order to investigate the SCEs and quantum mechanical confinement in IDG MOSFETs, different gate lengths (L = 200, 50, and 20 nm) and silicon film thicknesses (T_{Si} = 10, 5, and 3 nm) have been simulated.

2.2 Quantum drift-diffusion simulation code

In this study, we developed a 2D numerical simulation code that describes the operation of IDG MOSFETs. The code can take into account asymmetric devices (i.e., with independent gate bias, different gate work functions, or different gate-oxide thicknesses) and both n-channel and p-channel IDG MOSFETs.

The code is based on the numerical solution of the Poisson equation or Poisson-Schrödinger system coupled with the standard drift-diffusion transport equation (DDTE). The charge density (and consequently, the drain current) can be evaluated in both classical (Poisson + DDTE) and quantum-mechanical (Poisson-Schrödinger + DDTE) cases; the latter being commonly called “quantum drift-diffusion” in the literature[6-8)].

Poisson, Schrödinger, and DDTE equations are solved using a finite difference scheme with a uniform mesh on a 2D domain including the channel, source and drain regions, gate-oxide layers, and gate electrodes. Electric field penetration in the source and drain regions and electron wave function penetration in the gate-oxide layers can thus be taken into account. A flowchart of the code is shown in Fig. 1(b).

In the following, we briefly describe the equations for an n-channel fully depleted IDG device. Similar equations can be derived for p-channel structures. For a given channel

geometry and bias conditions, the 2D Poisson equation is solved [see the flowchart in Fig. 1(b)] considering the charge density given as[9)]

$$\rho(x,y) = q \times \left[N_{DOP} - n(x,y) \right], \tag{1}$$

where q is the absolute value of the electron charge, N_{DOP} is the doping atom concentration in the Si film (N_{DOP} = +N_D in the source and drain regions and N_{DOP} = -N_A in the channel), and n(x,y) is the electron density.

In the classical case, n is evaluated using the well-known Fermi-Dirac or Boltzmann statistics

$$n(x,y) = N_C \exp\left[-\beta \left(E_C(x,y) - \Phi_F(x) \right) \right], \tag{2}$$

where $\beta = q/kT$, $\Phi_{Fn}(x)$ is the 1D electron quasi-Fermi level (carrier transport is purely 1D in the channel device if the ratio of channel length to film thickness is typically greater than 3, which is the case in this study), $E_C(x,y)$ is the minimum of the conduction band, and N_C is the effective three-dimensional (3D) density of states for the conduction band.

In the quantum case, Poisson and Schrödinger equations [Fig. 1(b)] are self-consistently solved[6-8)]. Owing to the thin body, a strong vertical confinement (in the y-direction) causes the separation between carrier subbands to be large in energy. Every subband is then treated individually and the quasi-Fermi level populates only a few modes even at a high bias. The quantum charge density n_Q is given as[10)]

$$n_Q(x,y) = \frac{qkT}{\pi\hbar^2} \sum_{l,t} \sum_{i=1}^{N_{lev}} m_{2D}^{t,l} g_{t,l} \times \left| \Psi_{t,l}^{i}(x,y) \right|^2 \times \ln\left\{ 1 + \exp\left[-\beta \left(E_{t,l}^{i}(x) - \Phi_F(x) \right) \right] \right\}, \tag{3}$$

where subscript t refers to transverse electrons (m_t^* = 0.19×m_0, g_t = 4, $m_{2D}^t = \sqrt{m_l^* m_t^*}$), subscript l refers to longitudinal electrons (m_l^* = 0.98×m_0, g_l = 2, $m_{2D}^l = m_t^*$), $E_{t,l}^i(x)$ is the *i*th (t or l) carrier energy subband induced by the one-dimensional (1D) vertical confinement, $\Psi_{t,l}^i(x,y)$ is the corresponding normalized wave function, and N_{lev} is the maximum number of

modes considered (we assume here N_{lev}=20 to correctly treat both source/drain and channel regions).

The next solving step concerns the continuity equation [Fig. 1(b)], which is numerically solved to ensure a constant drain current along the channel (x-direction). The continuity equation gives the numerical solution of the quasi-Fermi level $\Phi_F(x)$ used in eqs. (2) or (3). After reaching convergence, the drain current density is finally evaluated from the drift-diffusion expression[10,11)]

$$J(x,y) = -q \times \mu(x,y) \times n(x,y) \times \frac{d\Phi_F(x)}{dx}, \qquad (4)$$

where μ is the electron mobility. To facilitate our understanding of quantum confinement effects in IDG MOSFETs, we considered here a constant mobility (the mobility dependences as function of transverse and longitudinal electric fields, lattice temperature, and doping level and the subband modulation on the channel mobility are not taken into account in our simulations[12)]). Note that the solution of the Poisson-Schrödinger system can also be coupled with the ballistic transport equation, as was presented in a previous work[11,13)].

The code provides considerable additional information and valuable physical insights (such as the 2D profile of electrostatic potential, classical and quantum carrier densities in the channel, energy levels, and total inversion charge) used to investigate the SCEs and quantum-mechanical effects in IDG MOSFETs. Simulated $I_{DS}(V_{Gf})$ characteristics in DG and IDG MOSFETs have been compared in the classical case with data obtained from simulation with a commercial code[14,15)] (Atlas Silvaco[16)]). An excellent fit has been obtained for large ranges of gate lengths, silicon film thicknesses, and V_{Gb} values.

We end this section with a discussion of the domain validity of our simulation approach. As device dimensions continue to decrease, the channel lengths (widths and/or thicknesses) are approaching the characteristic wavelength of particles (for example, the de Broglie wavelength at the Fermi energy) and quantum effects are expected to be increasingly

significant. Quantum effects (related to both carrier confinement and quantum ballistic transport) may dominate the operation of nanoscale devices: for example, it is expected that direct source-to-drain tunnelling will be a serious limiting physical phenomenon for future device scaling (typically below 6-8 nm channel length[11,17]). The drift-diffusion transport model considered in this study does not have predictive capability for simulating quantum transport in ultra small structures; quantum transport tools are thus required for accurate description of nanoscale device operation. Different approaches have been developed, one of the most precise being the solving of the Schrödinger equation with open boundary conditions, as performed using the non-equilibrium Green's function (NEGF) formalism[13,18-20]. However, in this paper, the smallest channel length considered in simulation is L=20 nm. For channel lengths larger than 20 nm, it can be considered that quantum transport is still limited and that carrier transport can be described by the drift-diffusion approach with a sufficient accuracy.

3. Results and Discussion

For all simulations, a constant carrier mobility [$\mu(x,y) = 200\ cm^2/(V.s)$] in the silicon film (source-channel-drain) has been considered. $I_{DS}(V_{Gf})$ characteristics of an n-channel IDG MOSFET in classical (dash lines) and quantum (solid lines) cases for different back gate biases are shown in Fig. 2(a). We can firstly note that V_{Gb} modulates $I_{DS}(V_{Gf})$ characteristics in both the classical and quantum cases. Then, the main electrical parameters in the subthreshold regime (threshold voltage V_T, subthreshold swing S, and off-state current I_{off}) are also modulated by V_{Gb}. These parameters depend on the transverse electric field E_{xC} in the structure, given as[21]

$$E_{xC} = \frac{(V_{Gf} - V_{Gb}) - (V_{FBf} - V_{FBb})}{T_{Si} + 2\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right)T_{ox}}, \qquad (5)$$

where V_{FBf} and V_{FBb} are the flat-band voltages at the front and back gates (in our case $V_{FBf} = V_{FBb}$, because the two gates are considered identical), and ε_{Si} and ε_{ox} are the silicon film and oxide-gate permittivity, respectively. We can also observe in Fig. 2(a) the marked effect of quantum mechanical confinement on the electrical parameters of the IDG MOSFET even when the silicon film is relatively thick. To compare the effects of quantum confinement in IDG MOSFETs ($V_{Gb} \neq V_{Gf}$) and DG MOSFETs ($V_{Gb} = V_{Gf}$), $I_{DS}(V_{Gf})$ curves in the classical and quantum cases are presented in Fig. 2(b) for $V_{Gb} = 0$ V. In DG MOSFETs, the $I_{DS}(V_{Gf})$ characteristic in the quantum case simply shifts towards the right side and the subthreshold swing is the same as that obtained in the classical case. In IDG MOSFETs, the subthreshold swing is degraded in addition to the shift of the $I_{DS}(V_{Gf})$ characteristics in the quantum case compared with the classical case. Figure 2(b) shows that the effects of quantum mechanical confinement are more important in IDG MOSFETs than in DG MOSFETs. The explanation is that carriers are confined in a triangular quantum well in IDG MOSFETs and not in a rectangular quantum well, as is the case in DG MOSFETs. Therefore, in IDG MOSFETs, carriers are subjected to electric-field-induced quantum confinement, in addition to T_{Si}-induced structural confinement. In DG MOSFETs, the transverse electric field is very weak ($E_{xC} \sim 0$ V/m) and quantum effects are predominantly due to structural quantum confinement. Thus, the quantum-induced shift in $I_{DS}(V_{Gf})$ curves is larger in IDG MOSFETs than in DG MOSFETs.

Figure 3 shows the threshold voltage [extracted by the constant current method at a current of 100 nA/L(nm) from $I_{DS}(V_{Gf})$ curves at $V_D = 1.0$ V] in the IDG MOSFET, as a function of V_{Gb} for L = 50 nm and two different silicon film thicknesses in both the classical and quantum cases. The high threshold voltages are due to the midgap metal gates chosen for DG MOSFET structures. As expected, the threshold voltage varies linearly when V_{Gb} increases from -1.0 to ~0.1 V in both the classical and quantum cases. This V_T linear variation

of the threshold voltage and other peculiarities of IDG MOSFETs, such as the gain in sensitivity to V_{Gb}, can be practically used for circuit applications such as signal mixers and memory cells[1-5]. Figure 3 shows that the quantum threshold voltage is always higher than the classical one owing to quantum confinement that causes electron density reduction in the silicon film. We also note that the classical and quantum threshold voltages are nearly equal when V_{Gb} reaches $V_{Gf} = V_T$, i.e., when E_{xC} tends to zero. Thus, the effect of carrier quantization in IDG MOSFETs is minimal when the transverse electric field is close to zero, i.e., when the electric-field-induced quantum confinement is weak.

The threshold voltage as a function of T_{Si} in the IDG MOSFET (at $V_{Gb} = 0$ V) and the DG MOSFET for L = 50 nm in the classical and quantum cases is presented in Fig. 4. In the DG MOSFET, the reduction in T_{Si} only induces a slight increase in threshold voltage. The difference between the quantum and classical threshold voltages is small in the DG MOSFET for all silicon film thicknesses. A different behaviour is obtained for the IDG MOSFET: the increase in threshold voltage when T_{Si} decreases is large, particularly in the quantum simulation. The difference between the classical and quantum V_T is found to be markedly increased in the IDG MOSFET compared with the DG MOSFET, owing to the occurrence of electric-field-induced quantum confinement in the IDG MOSFET in addition to structural quantum confinement. These results illustrate the significant impact of quantum confinement on electrical parameters of IDG MOSFETs, particularly for thin silicon films.

In order to investigate SCEs in IDG MOSFETs, the V_T roll-off variation versus T_{Si} in both the classical and quantum cases at different V_{Gb} is shown in Fig. 5. The V_T roll-off for a specific channel length L is calculated at $V_D = 0.1$ V as $V_T(L = 200\text{ nm}) - V_T(L)$. The V_T roll-off is higher in the quantum case, because the quantum confinement tends to move the charge centroid away from the front interface, and thus, the control by the front gate of SCEs is less effective. This effect is confirmed by the V_T roll-off behaviour with V_{Gb}: the quantum V_T roll-

off is higher for V_{Gb} = -0.6 V than for V_{Gb} = 0 V, because in the first case, the transverse electric field is larger, leading to a significant quantum confinement. The charge centroid is moved towards the back interface and the control of SCEs is more difficult [3,21] for V_{Gb} = -0.6 V than for V_{Gb} = 0 V. In this latter case, the quantum confinement is notably reduced and the charge centroid is near the front interface. When T_{Si} is reduced (e.g., T_{Si} = 3 nm), the V_T roll-off strongly decreases for all V_{Gb} and in both the classical and quantum cases, owing to better control by the front gate of the electrostatic potential in the channel. The comparison between the quantum and classical simulations in Fig. 5 shows that, although SCEs are reduced when silicon film is thinned, quantum confinement markedly degrades the SCE immunity of IDG MOSFETs.

For short-channel devices (e.g., L = 20 nm), it is important to study the impact of quantum mechanical effects on the DIBL effect [calculated as [$V_T(V_D = 0.1$ V) - $V_T(V_D = 1.0$V)]/ΔV_D]. In Fig. 6, DIBL is plotted as a function of V_{Gb} in both the classical and quantum cases and compared with DIBL in DG MOSFETs. This figure confirms that quantum confinement is more important in IDG MOSFETs than in DG MOSFETs. Our results show that for a V_{Gb} less than about 0.2 V, DIBL in an IDG MOSFET is weaker than that in a DG MOSFET for the classical simulation, whereas, for the quantum simulation, DIBL in a DG MOSFET is always weaker than that in an IDG MOSFET. Similarly to V_T roll-off, this is due to the effect of quantum confinement on the charge centroid that is pushed towards the back interface and makes the SCE control more difficult[3,21]. This result illustrates the difference in electrical behaviour between DG and IDG MOSFETs, particularly for short-channel devices.

The effect of quantum confinement, i.e., carrier-energy quantization, can be particularly well illustrated by plotting the difference between the quantum threshold voltage and the classical threshold voltage (ΔV_{Tq}) as a function of V_{Gb} [Fig. 7(a)] and T_{Si} [Fig. 7(b)]. To better understand the effect of V_{Gb} variation on quantum confinement, the transverse electric

field as a function of V_{Gb} is shown in Fig. 8 for L = 50 nm and three silicon film thicknesses in the quantum case. The transverse electric field is calculated using eq. (5), where V_{Gf} is used under the threshold voltage conditions ($V_{Gf} = V_T$ with $V_D = 0.1$ V). We can firstly note that when the transverse electric field is minimum in the structure (for V_{Gb} approximately 0.4 V), ΔV_{Tq} is minimum. When V_{Gb} moves away from this value and decreases towards a negative value or increases above 0.4 V, the transverse electric field increases and quantum confinement is enhanced (then ΔV_{Tq} increases). Furthermore, when T_{Si} is reduced, the transverse electric field further increases and ΔV_{Tq} strongly increases with the reduction in T_{Si} [as shown in Figs. 7(a) and 7(b)]. For comparison, Fig. 7(b) also shows ΔV_{Tq} variation as a function of T_{Si} in the DG MOSFET: in this case, ΔV_{Tq} is almost negligible for $T_{Si} > 5$ nm owing to the weak structural quantum confinement in thick films. This figure confirms that quantum confinement is less important in DG MOSFETs than in IDG MOSFETs, where both T_{Si}-induced structural and electric-field-induced quantum confinements occur. The main conclusion drawn from Fig. 7(b) is that while in DG MOSFETs one can consider that quantum confinement is negligible for $T_{Si} > 5$ nm, in IDG MOSFETs quantum confinement cannot be neglected even for thick films ($T_{Si} > 10$ nm, depending on V_{Gb}). For negative V_{Gb}, quantum confinement is significant even for $T_{Si} > 15$ nm. These results show that quantum effects must be considered in the modeling of IDG MOSFET operation not only for thin films, but also for relatively thick silicon films, for which quantum confinement can be neglected in DG MOSFET operation.

Finally, the last parameter extracted from the $I_{DS}(V_{Gf})$ characteristics is the subthreshold swing. Figure 9(a) shows the subthreshold swing as a function of V_{Gb} in both the classical and quantum simulations for IDG and DG MOSFETs with $T_{Si} = 10$ nm and L = 50 nm. The variation in S for a V_{Gb} higher than 0.2 V is not shown, because S is very large (for example, if $V_{Gb} = 0.4$ V, S > 140 mV/dec) owing to SCEs and the device cannot be used under these

bias conditions. The subthreshold slope is higher in the IDG MOSFET than in the DG MOSFET. The DG MOSFET has a nearly ideal subthreshold slope (S = 62mV/dec), while the best (minimum) subthreshold swing in the IDG MOSFET is 76mV/dec in the classical simulation. This value increases with V_{Gb} owing to a strong electron accumulation near the back gate. The quantum mechanical effects also modify this parameter in IDG MOSFETs due to the shift of the charge centroid away from the front interface, which enhances the SCEs. Figure 9(b) shows the effect of T_{Si} on the subthreshold swing in IDG and DG MOSFETs. Since the reduction in T_{Si} does not significantly affect the subthreshold swing in DG MOSFETs, in IDG MOSFETs, the subthreshold swing is enhanced in both the classical and quantum cases for $V_{Gb} = 0$ V. The difference between the classical and quantum simulations is quasi constant but not negligible (~15 - 20 mV/dec).

4. Conclusions

In this study, short-channel effects and quantum confinement in IDG MOSFET devices have been investigated using a 2D numerical simulation code that calculates the drain current. The main electrical parameters of IDG MOSFETs (threshold voltage, V_T roll-off, ΔV_{Tq}, and subthreshold swing) have been compared with those of DG MOSFETs for different gate lengths and silicon film thicknesses. The results show that the electrical operation of IDG MOSFETs differs from that of DG MOSFETs owing to the presence of an important transverse electric field in the first structure. This transverse electric field significantly modifies the quantum well shape and leads to the occurrence of electric-field-induced quantum confinement in IDG MOSFETs, in addition to T_{Si}-induced structural quantum confinement. This phenomenon leads to subthreshold performance degradation and to the enhancement of SCEs in IDG MOSFETs compared with DG MOSFETs. This study shows that in IDG MOSFETs, quantum effects can be important even for $T_{Si} > 10$ - 15 nm (depending on V_{Gb}), while in DG MOSFETs quantum confinement is negligible for $T_{Si} > 5$

nm. We demonstrate that quantum confinement must be taken into account in the modeling of IDG MOSFETs, not only for thin silicon films but also for relatively thick silicon films, for which quantum confinement can be neglected in DG MOSFET operation.

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Figure captions

Figure 1. (a) Schematic view of simulated IDG MOSFET. The main device electrical and geometrical parameters of the structure are also defined. (b) Flowchart of 2D numerical simulation code developed for calculation of drift-diffusion drain current characteristics including classical and quantum simulations.

Figure 2. Impact of quantum-mechanical effects on drain current of n-channel IDG MOSFET: (a) $I_{DS}(V_{Gf})$ characteristics for different back gate biases (V_{Gb} = -0.4 to 0.4 V, step 0.4 V) for studied architecture (L = 200 nm, T_{Si} = 10 nm, V_D = 1.0 V); (b) comparison between $I_{DS}(V_{Gf})$ characteristics in IDG MOSFET (V_{Gb} = 0 V) and DG MOSFET ($V_{Gb} = V_{Gf}$).

Figure 3. Impact of SCEs and quantum confinement on threshold voltage as function of back gate voltage, extracted in V_D = 1.0 V characteristics of n-channel IDG MOSFET. Comparison between quantum (solid lines) and classical (dash lines) simulations for L = 50 nm and different silicon film thicknesses (T_{Si} = 3 and 10 nm).

Figure 4. Threshold voltage versus silicon film thickness in classical and quantum cases for IDG MOSFET (V_{Gb} = 0 V) and DG MOSFET with L = 50 nm and V_D = 1.0 V.

Figure 5. Comparison between V_T roll-off in quantum and classical cases versus silicon film thickness for different back gate biases (V_{Gb} = -0.6 and 0 V) with L = 50 nm and V_D = 0.1 V.

Figure 6. Quantum and classical simulations of IDG MOSFET DIBL versus back gate bias for L = 20 nm and T_{Si} = 10 nm. Predicted DIBL in DG MOSFET in classical and quantum simulations is also indicated.

Figure 7. Difference between threshold voltages calculated in classical and quantum simulations (ΔV_{Tq}) of n-channel IDG MOSFET at V_D = 1.0 V: (a) ΔV_{Tq} versus back gate bias for L = 50 nm and different silicon film thicknesses (T_{Si} = 3, 5, and 10 nm); (b) comparison of $\Delta V_{Tq}(T_{Si})$ characteristics for L = 50 nm in IDG MOSFET (V_{Gb} = -0.8, 0, and 0.4 V) and DG MOSFET.

Figure 8. Transverse electric field in L = 50 nm n-channel IDG MOSFET in quantum simulation versus back gate voltage for different silicon film thicknesses. The transverse electric field is calculated using eq. (5), where V_{Gf} is used under the threshold voltage conditions ($V_{Gf} = V_T$ with V_D = 0.1 V).

Figure 9 (a) Subthreshold swing as function of back gate voltage in classical and quantum cases for n-channel IDG MOSFET in IDG mode (V_{Gb} = 0 V) and DG mode. The simulation parameters are L = 50 nm, T_{Si} = 10 nm, and V_D = 1.0 V; (b) $S(T_{Si})$ characteristics in classical and quantum simulations for n-channel IDG MOSFET in IDG mode (V_{Gb} = 0 V) and DG mode with L = 50 nm and V_D = 1.0 V.

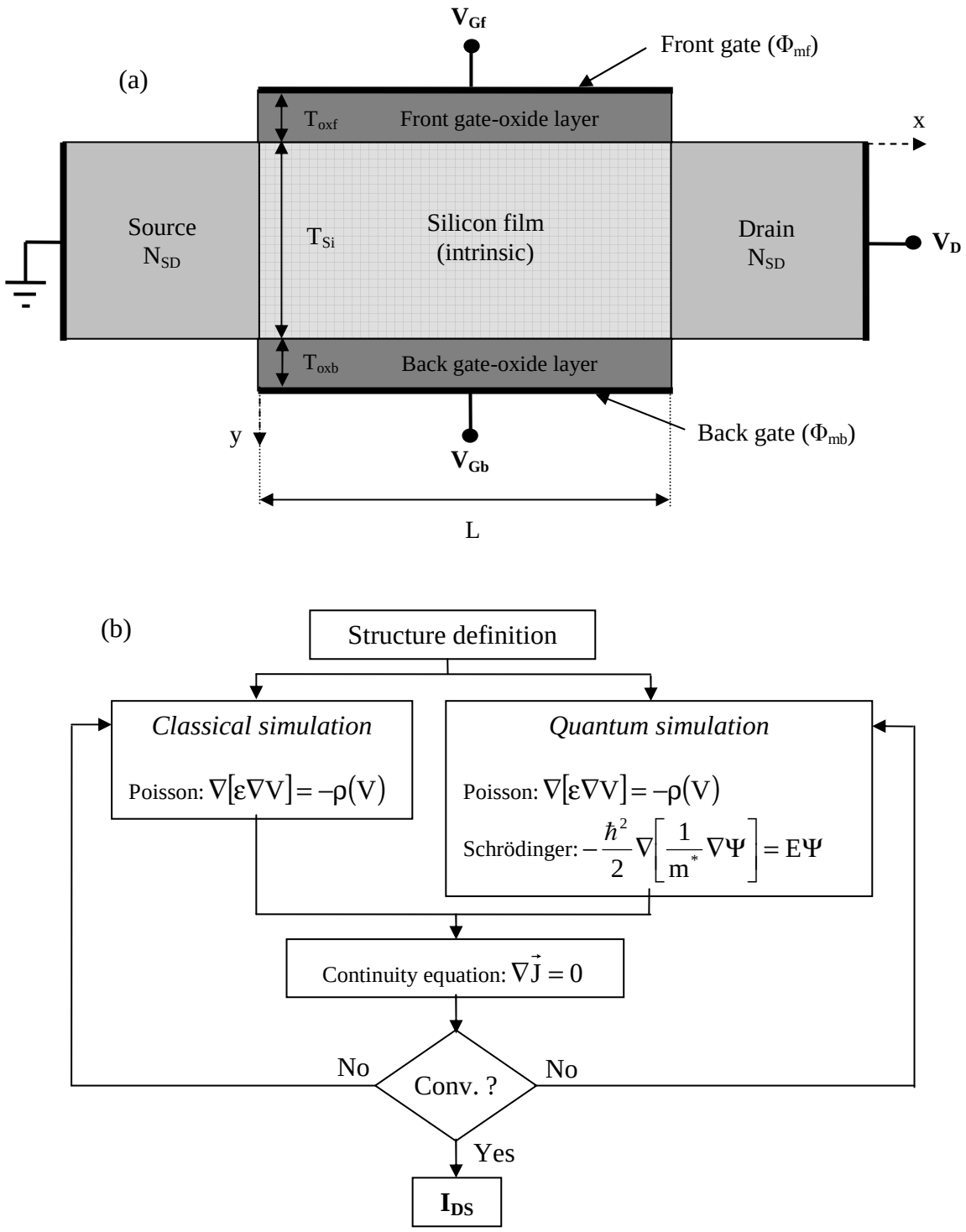

Figure 1. Moreau et al.

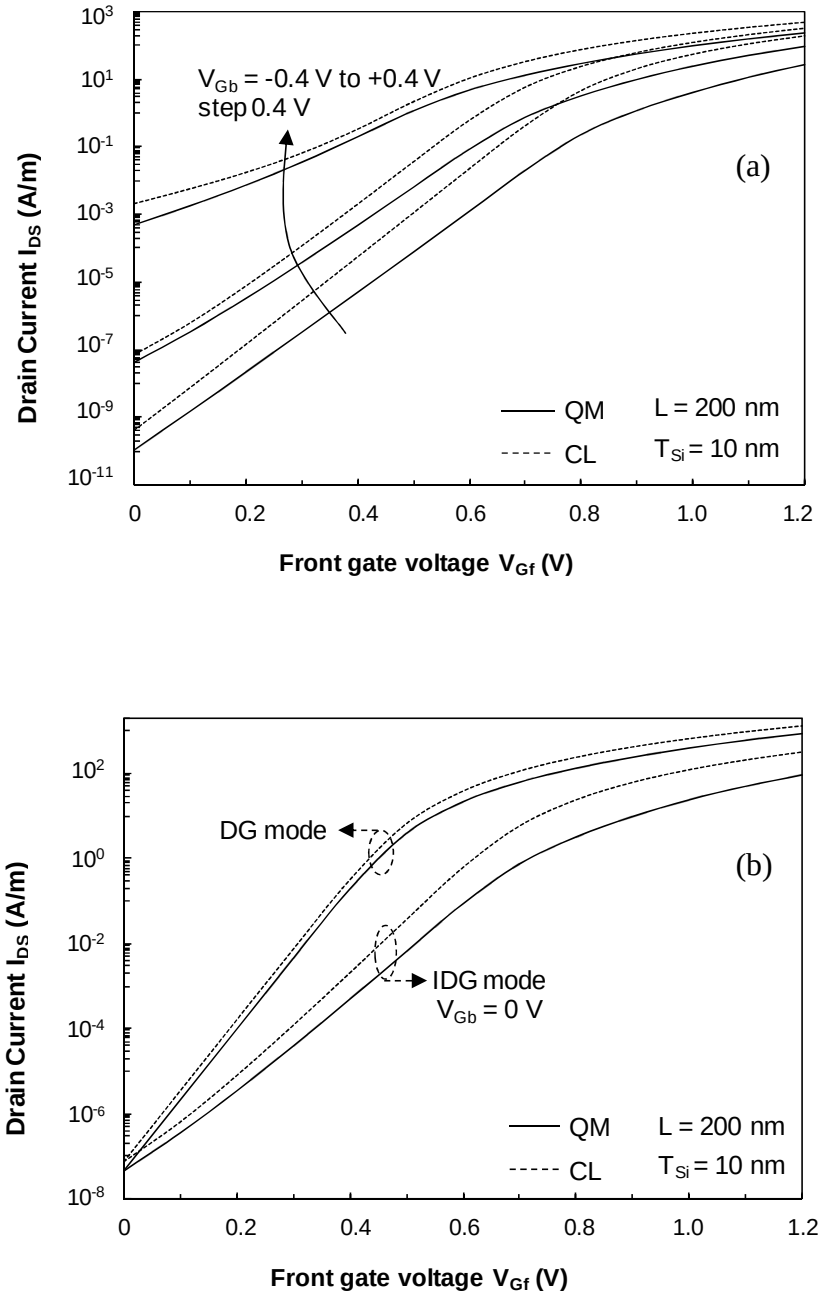

Figure 2. Moreau et al.

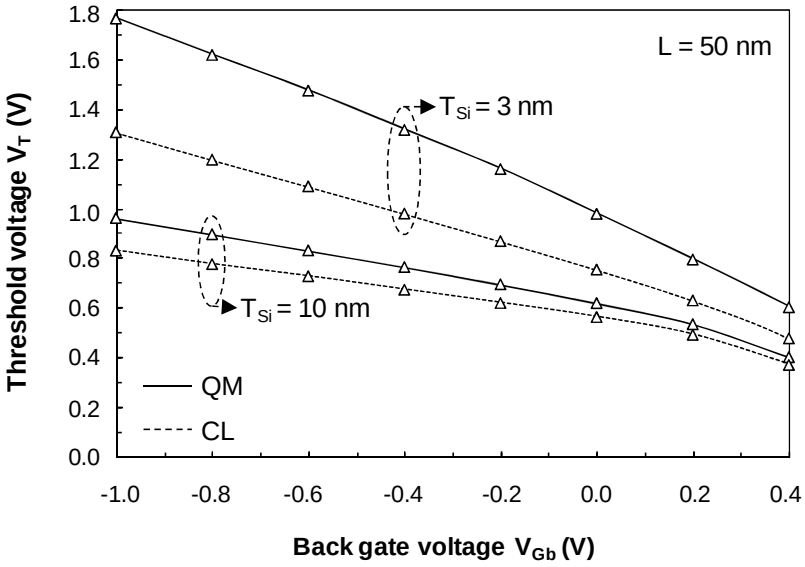

Figure 3. Moreau et al.

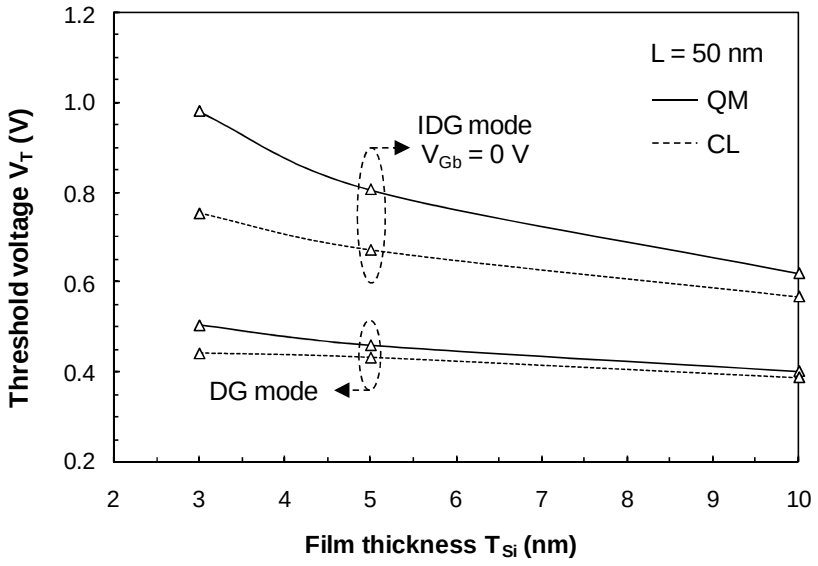

Figure 4. Moreau et al.

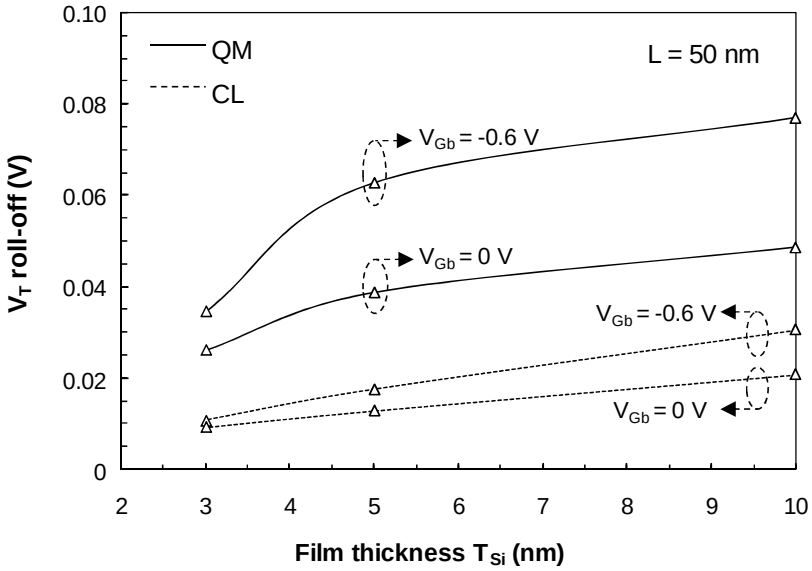

Figure 5. Moreau et al.

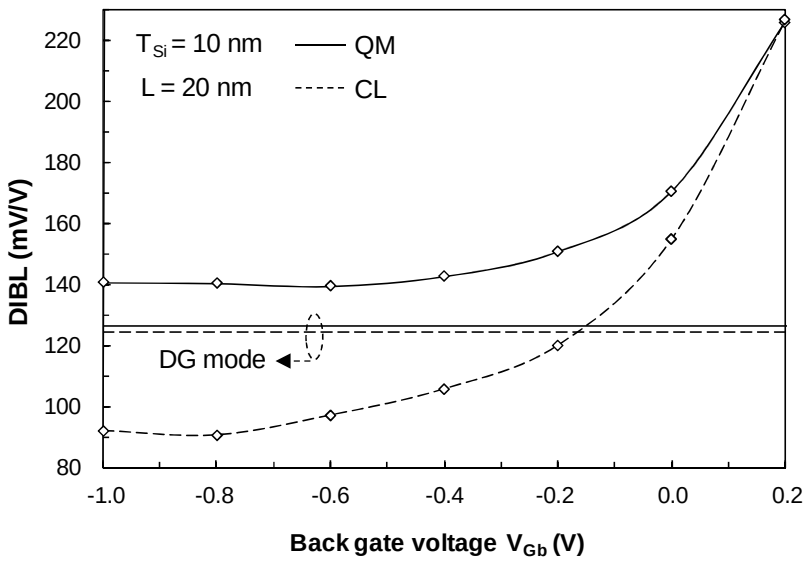

Figure 6. Moreau et al.

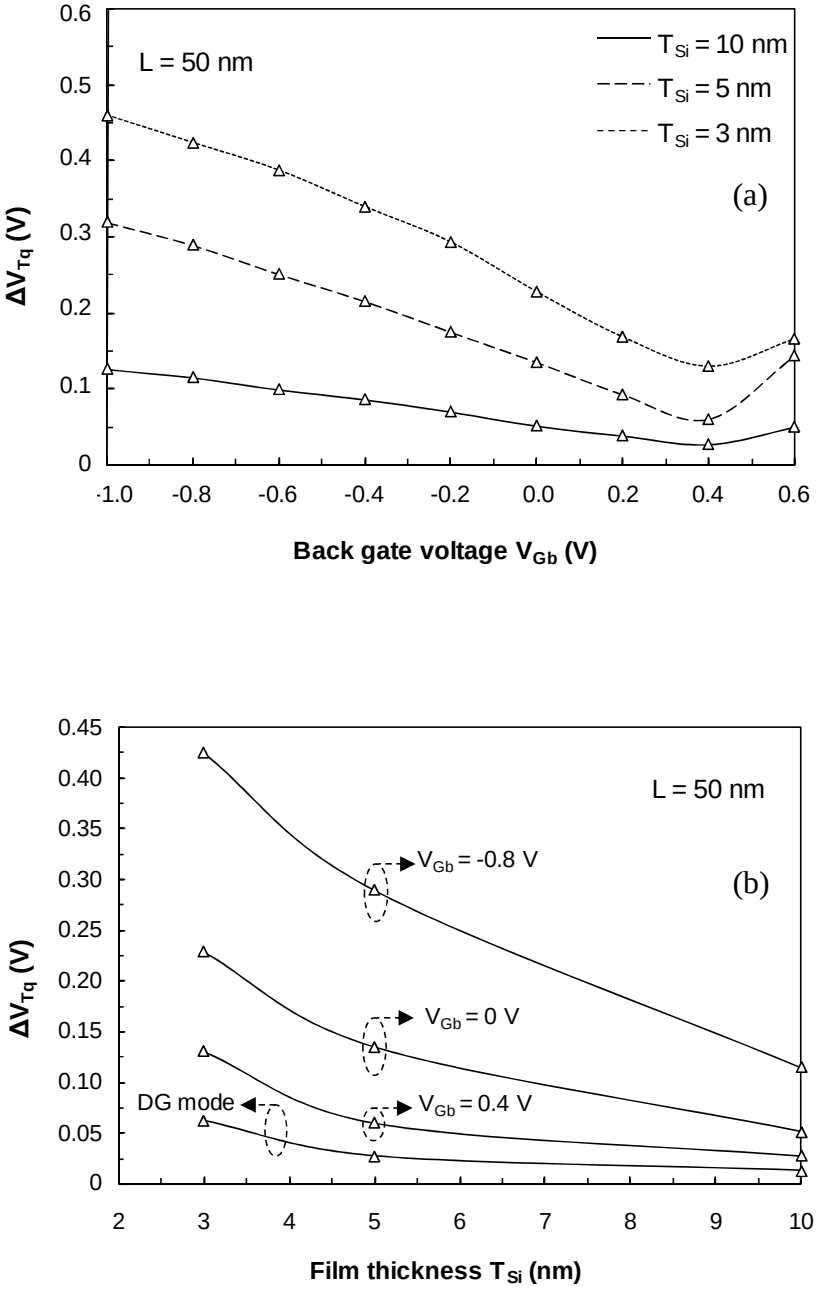

Figure 7. Moreau et al.

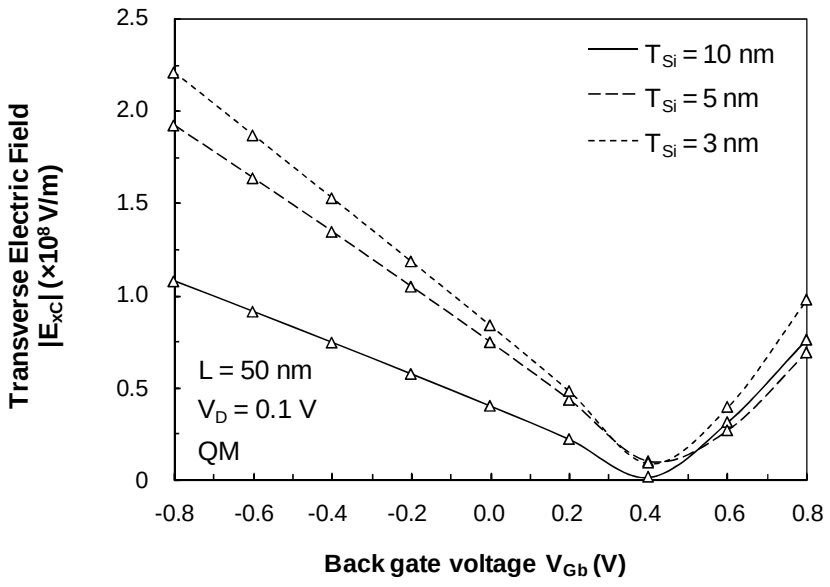

Figure 8. Moreau et al.

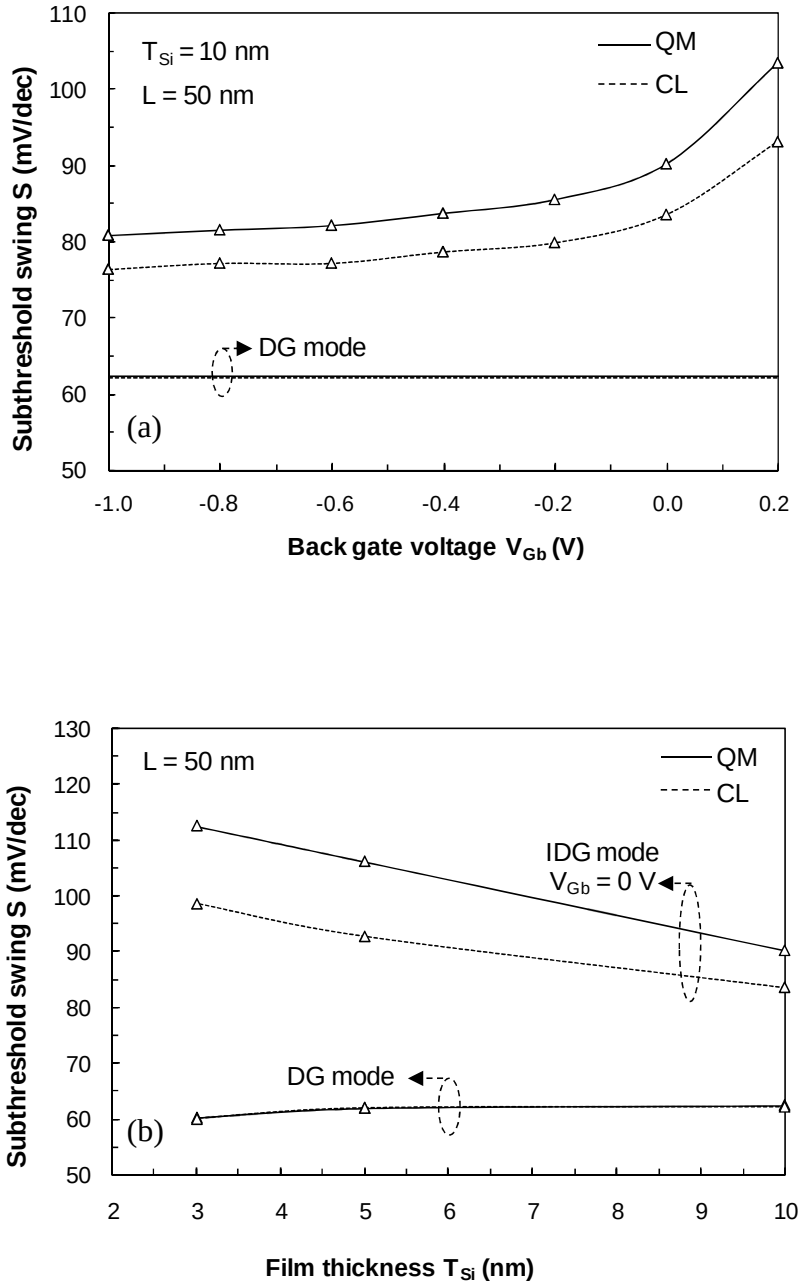

Figure 9. Moreau et al.