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## **NH 3 treatments of Hf-based layers for application as NVM active dielectrics**

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**Abstract**— The goal of this work is to investigate the effect of NH<sub>3</sub> nitridation on high-κ materials in view of application to non-volatile memories (NVMs). Our study focuses on the trapping properties of thick HfO<sub>2</sub> and HfAlO layers (6-14nm-thick). Through in-depth physical and electrical analyses, we demonstrate that an appropriate nitridation of these layers significantly reduces the charge trapping phenomena. Based on morphological analyses and analytical models, we argue that the lower trapping capability can be related to a smaller ratio of the crystalline phase of the high-κ layers.

**Introduction** — High-κ materials are currently under strong investigation for non-volatile memory (NVM) applications. They can offer important benefits both when they are used as interpoly (IPD) layer [1,2], in terms of coupling and insulating properties, and as tunnel stacks [3,4], due to the improved injection properties. However, the important trap density which characterizes these new materials constitutes a serious roadblock for the large-scale device integration, due to the VT instability and the trap-assisted gate leakage currents [5]. However, it is also possible to benefit from high-κ deep traps when they are used for charge storage in charge-trap memory applications [6]. Hence, today a major challenge is the process control of the high-κ trap properties.

## Sample description

### Trapping layers capacitor devices :

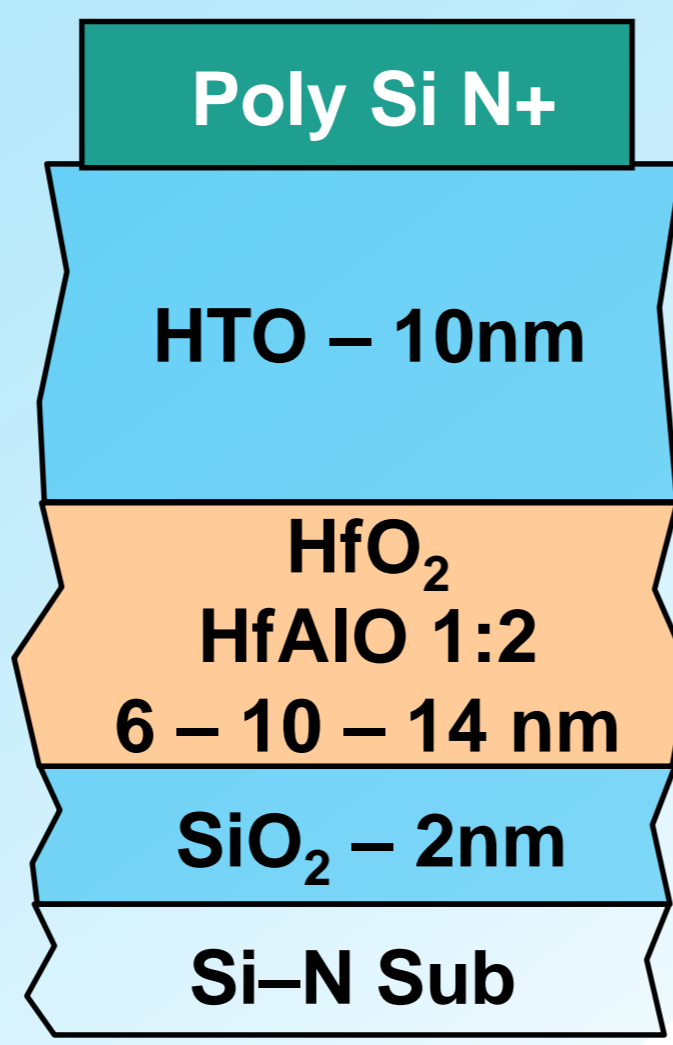
High-κ were integrated as charge trapping layers in capacitors in order to investigate their trapping properties, depending on the thermal treatments

- ✓ Tunnel oxide: SiO<sub>2</sub> – 2nm
- ✓ Trapping layer : HfO<sub>2</sub> or HfAlO (57% Hf) – 6nm, 10nm or 14nm.
- ✓ Blocking oxide: High Thermal Oxide (HTO) – 10nm

### High-κ thermal treatments :

- Post-deposition anneals (PDA):
  - (i) nitridation treatment, under NH<sub>3</sub> at 750°C during 30min. Role: trap passivation
  - (ii) inert treatment, under N<sub>2</sub> at 750°C during 1 min
- High temperature anneals, simulating the dopant activation :
  - (iii) spike anneal under N<sub>2</sub> at 1050°C.
  - (iv) 950°C under N<sub>2</sub> during 15s.

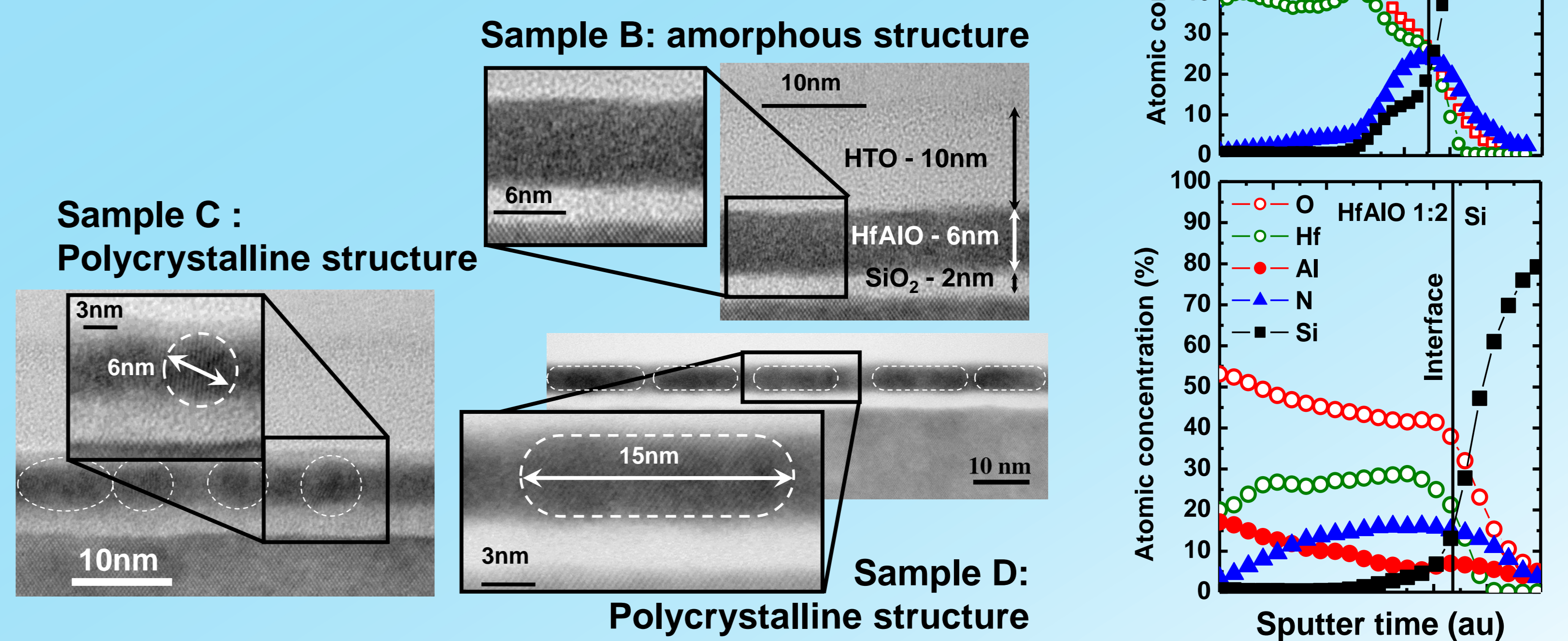
Thermal treatment	Sample					
	A	B	C	D	E	F
(i) NH <sub>3</sub> 750°C 30min	X		X		X	
(ii) N <sub>2</sub> 750°C 2min		X		X		X
(iii) N <sub>2</sub> 1050°C spike			X	X		
(iv) N <sub>2</sub> 950°C 15s					X	X



## Materials study

Based on Auger measurements, the nitrogen incorporation after NH<sub>3</sub> anneal was found localized:

- HfO<sub>2</sub> layer ▶ At the Si-sub/high-κ interface.
- HfAlO layer ▶ In the high-κ bulk layer: nitrogen absorption~15%.



→ The NH<sub>3</sub> anneal limited the crystallization of the HfAlO layer.

## Results and discussion

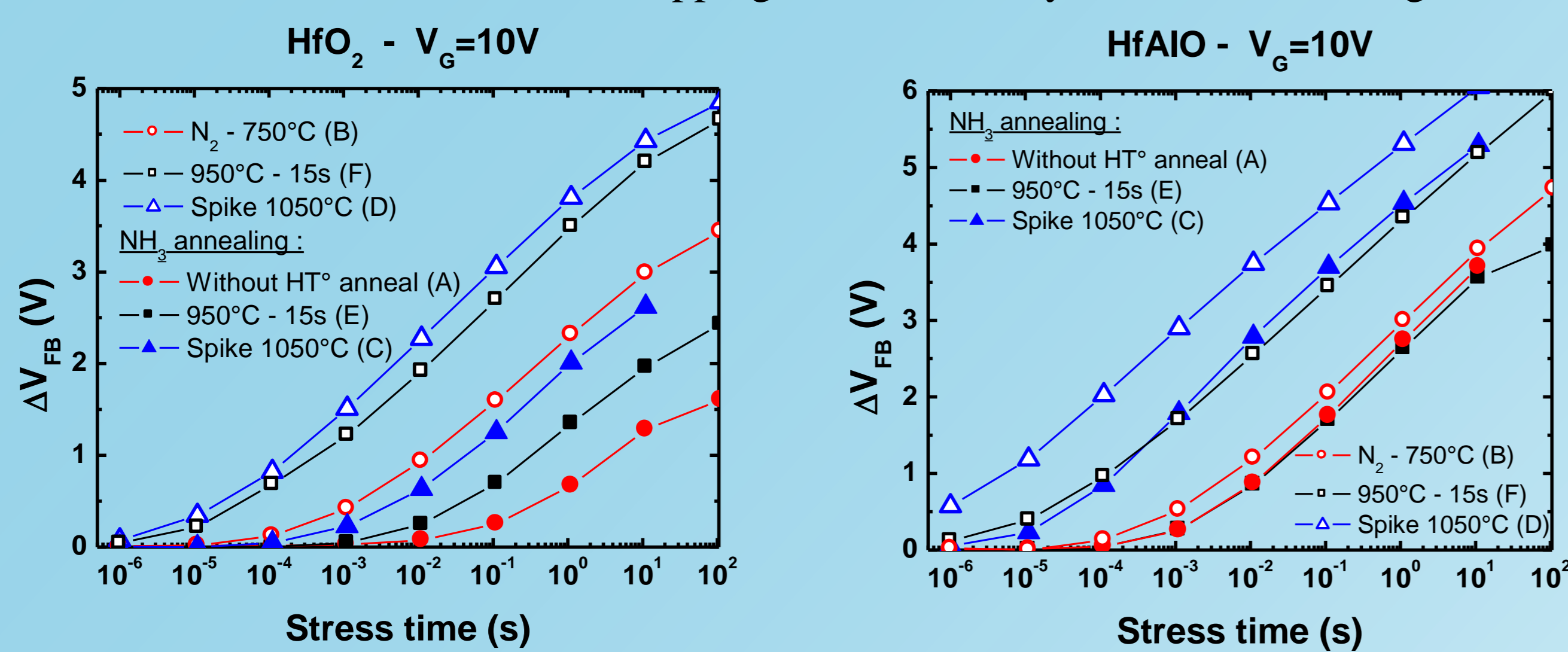
### Programming characteristics of the capacitors

#### HfO<sub>2</sub> layer:

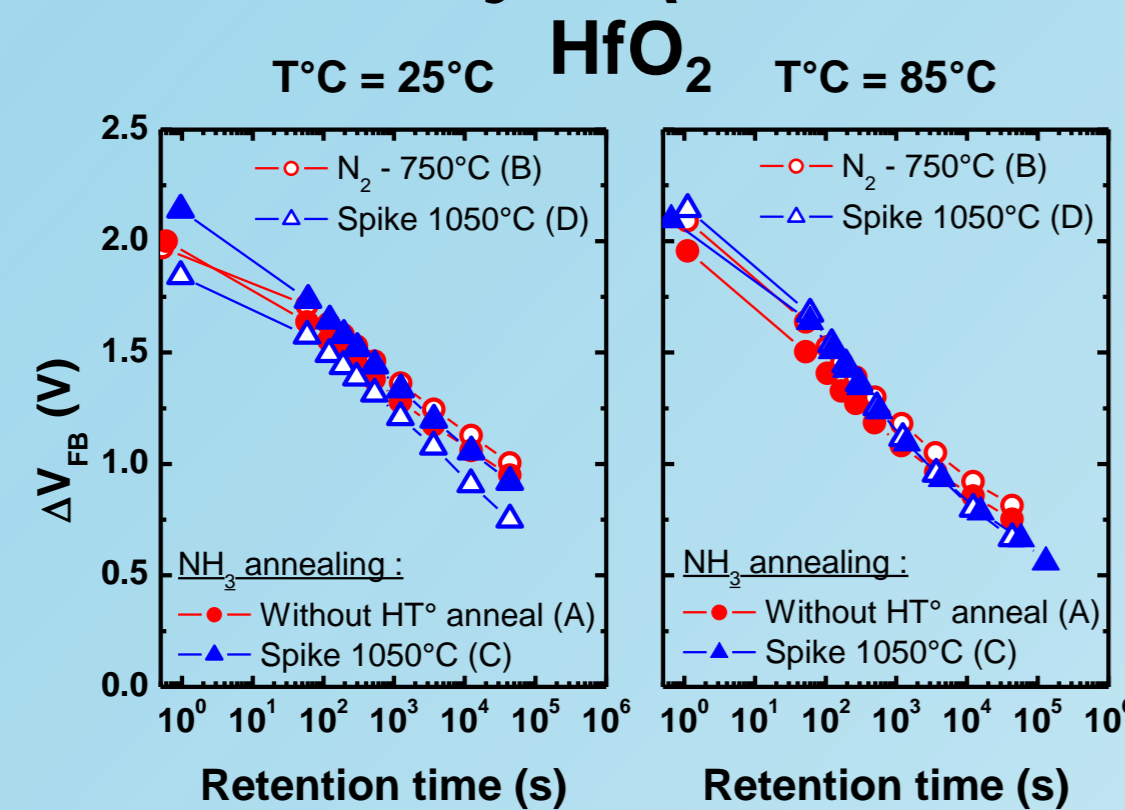
- High temperature anneal ▶ Trapping increasing
- Nitridation treatment ▶ Trapping reduction

#### HfAlO layer:

- High temperature anneal ▶ Trapping increasing
- Nitridation treatment ▶ Trapping reduction of layers that have undergone a high T° anneal



→ Correlation with the smaller ratio of crystalline phase of nitridated HfAlO layer (see TEM images)

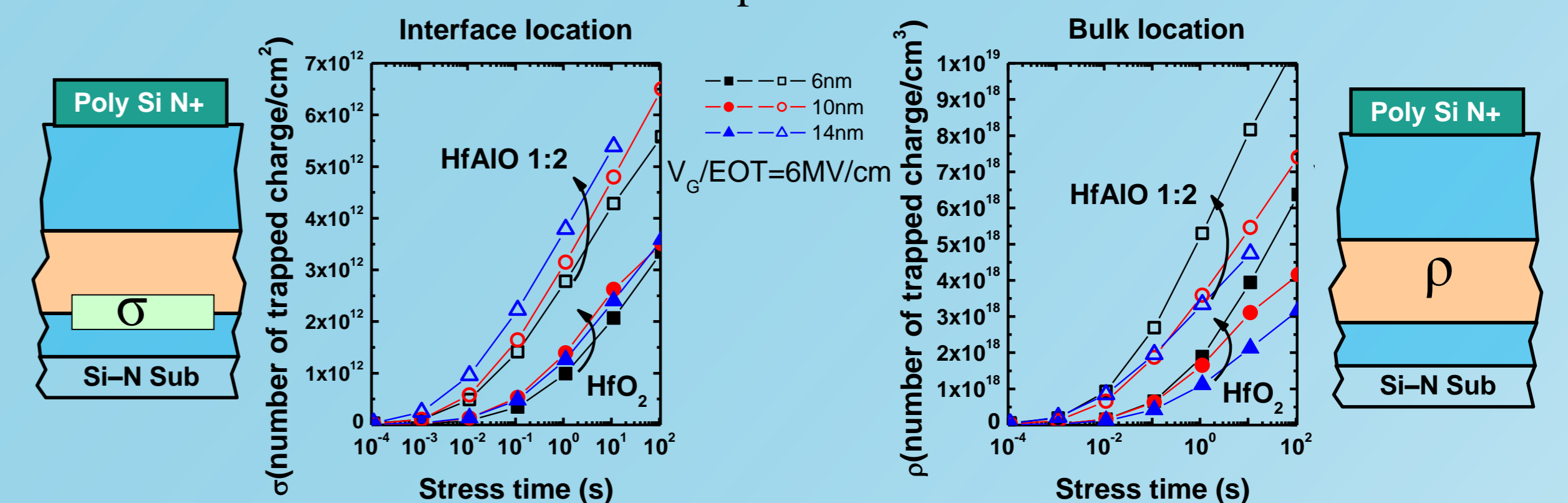


Charge loss rate does not increase after anneals

→ Tunnel oxide is not modified after high temperature anneals or nitridation treatment

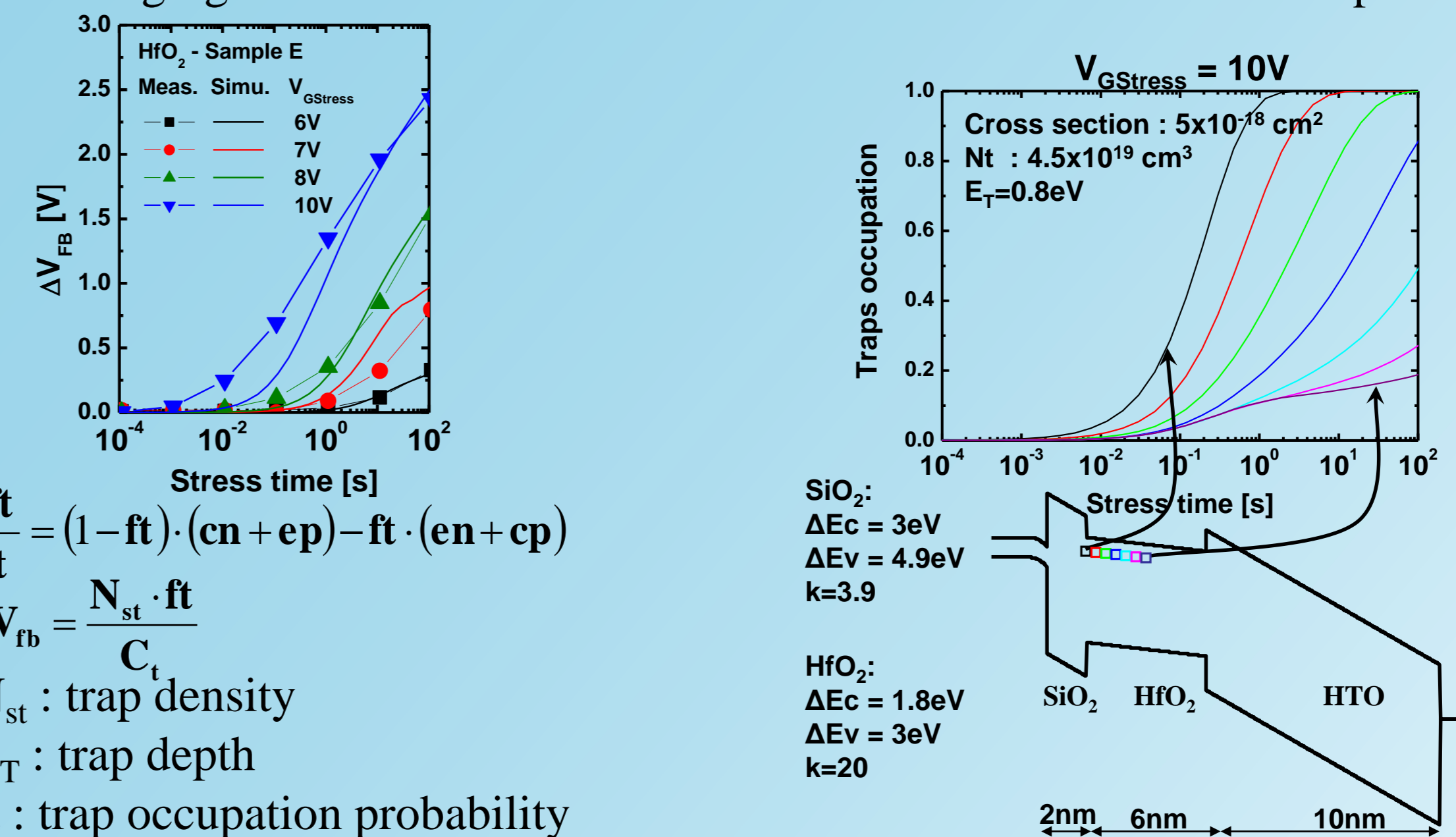
## Localization of the trapped charge: interface or bulk distribution?

- Interface normalization is consistent with the experimental results
  - Bulk normalization do not match with the experimental data
- Interface rather than bulk distribution



## Simulations of trapping in the high-κ layer

- Analytical model based on the SRH statistics presented in [6] and [7]
- Good fit with the experimental data
- The charging time constants increase with the distance between the traps and the cathode



$$\frac{dft}{dt} = (1-ft) \cdot (cn+ep) - ft \cdot (en+cp)$$

$$\Delta V_{fb} = \frac{N_{st} \cdot ft}{C_t}$$

■ N<sub>st</sub> : trap density

■ E<sub>T</sub> : trap depth

■ ft : trap occupation probability

■ cn/en & cp/ep : electron and hole capture/emission rates

→ Most of the trapped charges are located close to the High-κ/bottom oxide interface (the charging time constants increase with the distance between the traps and the cathode).

## Conclusion

- The trapping capability of the studied high-κ layers increases with the crystalline ratio (electrical results + TEM observations)
- The electron trapping mainly occurs at the bottom oxide/high-κ interface due to faster charging time constants (electrical results + simulations)
- NH<sub>3</sub> anneals can be used to reduce the parasitic trapping in high-κ layers: suitable for interpoly or tunnel applications

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