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Intrinsic fixed charge and trapping properties of HfAlO interpoly dielectric layers

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Abstract

The objective of this work is to investigate the fixed charge and the trapping properties of SiO₂ – HfAlO – SiO₂ (OHO) tri-layer stacks as interpoly dielectrics of NVMs. This study focuses on the key role played by the HfAlO composition. We show that the intrinsic fixed charge content increases with the Al concentration, while the trapping capabilities, during a gate stress, increases with the Hf ratio of the compound. We argue also that the charge trapping happening during a gate stress is mainly located at the high-k interface rather than in the volume. Retention characteristics are also shown. Finally, the experimental data are explained through a model based on a SRH approach.

1. Introduction

In order to meet the performance requirements of future generations of Flash memory [1], one of the nearest major improvements will concern the scaling of the InterPoly Dielectric (IPD) stack. For the 45nm and 35nm nodes, in order to compensate the loss of the vertical sidewalls of the poly-Si floating gate and keep high the coupling ratio [2, 3], the IPD thickness should be reduced. In a previous work [4], we proposed HfAlO high-k materials to replace the nitride layer in ONO interpoly dielectric stacks for future Flash memories, arguing the advantages both in terms of coupling and insulating properties. We showed that the leakage current was strongly governed by the trapping in the high-k layer, with a strong temperature activation. Indeed, a Poole-Frenkel conduction, probably assisted by the traps in the HfAlO layer, was identified.

In this paper, we further developed the analysis of HfAlO high-k materials, embedded in OHO stacks, by focusing on the trapping properties and fixed charges. In particular, we investigate: (1) the intrinsic negative fixed charge in the oxides, (2) the trapping phenomena which take place in the high-k dielectrics with various compositions and thicknesses during a gate stress, (3) the retention properties of these layers, and (4) finally, we present simulations based on a Shockley Read Hall (SRH) approach which allow us to model the electron trapping in the OHO stacks.

2. Experimental results

2.1 Sample description

The schematic of the triple layer capacitors studied in this work is shown in Figure 1. The high-k films were sandwiched between two HTO (High Thermal Oxide) deposited at 730°C, with a thickness of 4nm.

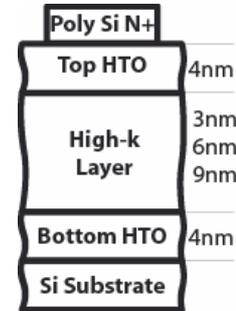


Fig. 1: Schematic showing the capacitor device stack studied in this work. Various high-k were investigated: HfO₂, Al₂O₃ and HfAlO with different Hf:Al ratios (9:1, 1:4 and 1:9).

Three different high-k materials, deposited by ALCVD, were studied: Hafnium Oxide (HfO₂), Aluminum Oxide (Al₂O₃) and Hafnium Aluminate (HfAlO). In HfAlO films, the Hf concentrations were controlled by the HfCl₄:Al(CH₃)₃ deposition cycle ratio, which are respectively: 9:1 (94% of Hf), 1:4 (31% of Hf), and 1:9 (27% of Hf). Different high-k physical thicknesses ranging between 3nm and 9nm were fabricated by controlling the number of ALD deposition cycles.

2.2 Intrinsic negative fixed charge

In this section we investigate the intrinsic fixed charge of the HfAlO layers.

Figure 2 plots the capacitance-voltage characteristics of the studied OHO triple layers in the virgin state.

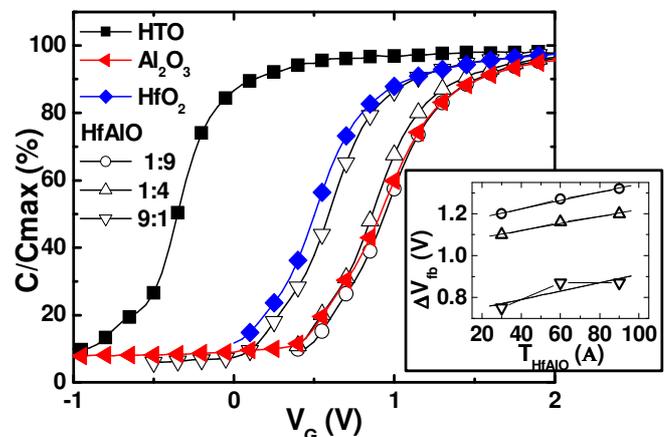


Fig. 2: C–V_G characteristics (in the virgin state) of OHO stacks with various high-k materials (Al₂O₃, HfO₂ and HfAlO with different compositions) compared to a 10nm HTO reference device. Inset: Flatband voltage shifts as a function of the HfAlO physical thickness.

We can observe that the flatband voltages of OHO samples are shifted compared to the 10nm-thick HTO reference sample, due to the presence of intrinsic fixed charge in the high-k layers. The shift increases monotonically when the Al concentration of the HfAlO alloy increases.

The origin of the intrinsic negative fixed charge in HfAlO materials is nowadays still not clear [5]. In amorphous Al₂O₃ layer, it was suggested that the Al₂O₃ could be dissociated into (AlO_{4/2})⁻ and Al³⁺ [6] and that, at the SiO₂/Al₂O₃ interface, the charge compensation does not take place.

The inset of Figure 2 shows that ΔV_{FB} is a linear function of the HfAlO thickness, which suggests a surface rather than a volume distribution of the fixed charge according to Equation 1, being in agreement with previous works reported in the literature [7-9].

$$\Delta V_{fb} = \frac{t_T}{\epsilon_{SiO_2}} \cdot (\sigma + t_H \cdot \rho) + \sigma \cdot \frac{t_H}{\epsilon_H} + \rho \cdot \frac{t_H^2}{2 \cdot \epsilon_H} \quad (1)$$

with :

- σ : charge density at high-k/Bottom HTO interface.
- ρ : volume charge density in high-k.
- t_H : thickness of high-k layer.
- t_T : thickness of HTO top layer.
- ϵ_H : high-k dielectric constant.
- ϵ_{SiO_2} : SiO₂ dielectric constant.

Table 1 summarizes the number of equivalent fixed charge localised at the bottom HTO/High-k interface, calculated from the V_{FB} shifts.

HfAlO composition	Number of fixed charge nb/cm ²
9:1	3 · 10 ¹²
1:4	3.5 · 10 ¹²
1:9	4 · 10 ¹²

Table 1: Number of equivalent fixed charge (extracted from the characteristics reported in Figure 2) localised at the bottom HTO /High-k interface.

2.3 Trapping properties

In this section, we investigate in more details the charge trapping phenomena of OHO samples during a gate stress.

The gate current density as a function of the electric field is reported in Figure 3. On the same graph is also reported the time evolution of the gate current at constant gate bias (J_G -Time) on virgin devices. The hysteretic behaviour, and the continuous decreasing of the leakage current with the elapsing time demonstrate that trapping phenomena take place in the high-k materials. Note that the charge trapping could be an issue for IPD applications, as it may degrade the reliability of the memory, generating threshold voltage instabilities.

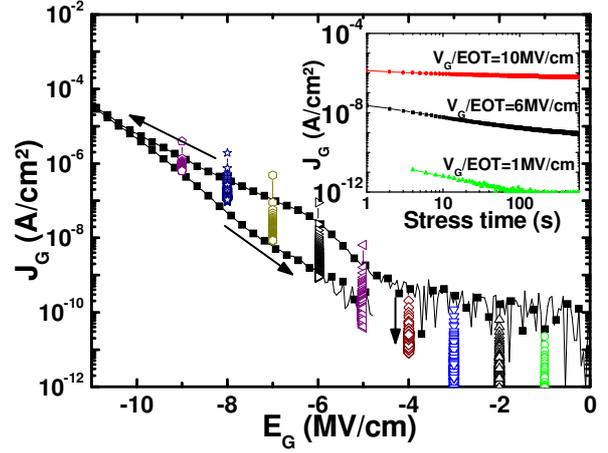


Fig. 3: Current density J_G versus equivalent electric field E_G of HTO /HfAlO 9:1 – 9nm/HTO stack. J_G -time measurements on virgin devices are also represented for different electric fields. Inset: J_G -time measurements performed at different applied electric field (1MV/cm, 6MV/cm and 10MV/cm) as a function of time.

To evaluate more precisely the trapping capabilities of the interpoly stacks, we monitored the evolution of the flatband voltages as a function of time when the devices were submitted to different gate stresses (Figure 4). A continuous V_{FB} shift is observed, showing the progressive electron trapping in the stack as the stress time increases. It clearly appears that for a given stress condition, the trapping capability increases with the Hf concentration. As already reported in the literature [4, 10], this result could be correlated with the crystalline structure of the high-k materials: the larger the Hf concentration, the more crystalline the layer, and hence, the higher the trapping capability.

Based on these measurements, we extracted the charges trapped in the gate stack after programming. We assume that the charges are localized at the interface between the Bottom HTO and the HfAlO layer. Indeed, the further the traps are from the cathode, the slower the charging kinetics. Making this assumption, it appears that the extracted trapped charge value does not depend on the HfAlO thickness (Figure 5). This confirms (see Equation 1) that charges are mainly trapped at the high-k interface and that the bulk contribution is negligible at the first order.

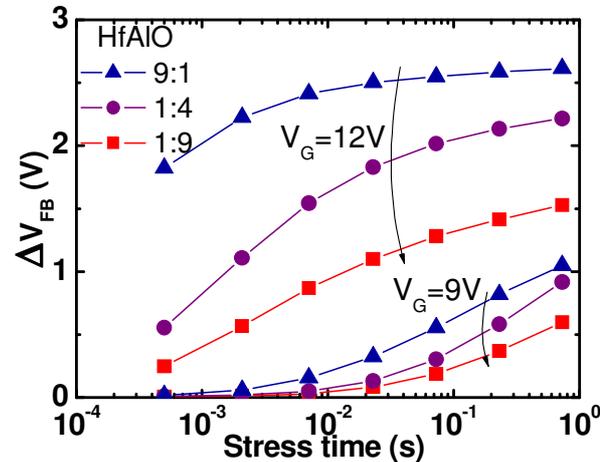


Fig. 4: Programming characteristics of OHO samples with various HfAlO compositions. The HfAlO thickness is 6nm.

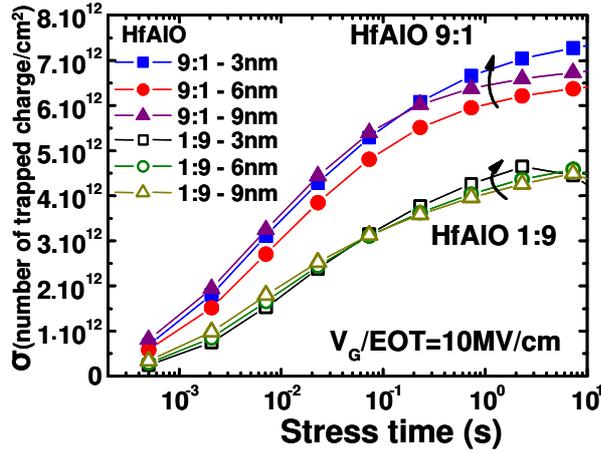


Fig. 5: Trapped charges in OHO samples, with various compositions and thicknesses of the HfAlO layer, as extracted from the programming characteristics. The stressing conditions are performed at constant V_G/EOT . We assume that the charges are localized at the interface between the Bottom HTO and the HfAlO layer.

2.4 Retention characteristics

In this section, we investigate the dynamic discharging of the charges previously trapped in the OHO layers by a writing stress. Figure 6 plots the room temperature retention characteristics of OHO samples with different compositions of the HfAlO layer. We observe that for the Hf-rich sample, the electron discharging rate is quite fast, whereas the HfAlO 1:4 and 1:9 keep most of the charge after 10^6 s.

Figure 6 also shows the strong temperature activation. Indeed, the charge loss is strongly accelerated at 85°C (within a factor 2 for the 9:1 sample). Nevertheless, the trend observed at room temperature is still conserved, i.e.: the 1:4 and 1:9 HfAlO layers exhibit the same charge decay, while for the 9:1 HfAlO sample, only 50% of trapped charge remains after 10^6 s. These observations are consistent with experiments performed on SONOS-like structures with high-k trapping layers [11].

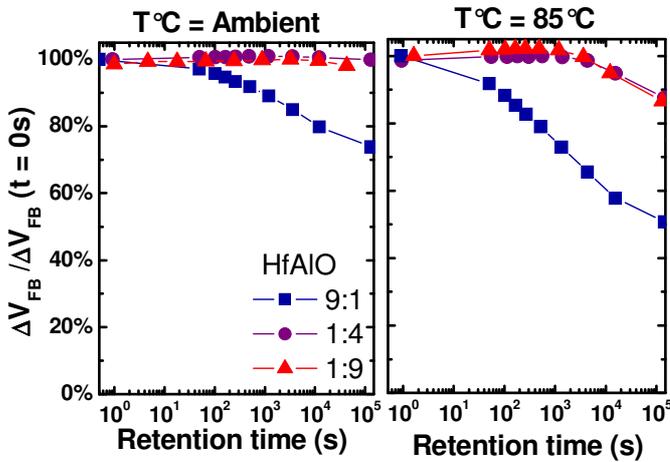


Fig. 6: Room temperature and 85°C retention characteristics of OHO samples with various compositions of HfAlO. The HfAlO thickness is 6nm. The programming conditions are fixed to have an initial flatband voltage shift of 1.5V for each sample.

3. Modelling

In this part, we introduce an analytical model to qualitatively explain the trapping characteristics of our IPD stacks. To this aim, we use the SRH model presented in [10], and we focus on the Hf-rich (9:1) OHO samples.

The simulations are performed assuming that:

- The trapped charge is localized at the bottom HTO / HfAlO interface, which is consistent with our experimental data. Note that in a more realistic approach, we should take into account the charge trapped in the HfAlO bulk, characterised by slower trapping time constants.
- The thermalization of electrons in the SiO_2 layer close to the cathode is neglected. In fact, in our range of programming voltages, the electron paths in the conduction band of the HTO, after tunneling, is inferior to 1nm (Figure 7), which is indeed shorter than the mean free path of electrons in SiO_2 [12]. In other words, we assume that the electron energy remains constant till the trapping in HTO/HfAlO interface states happens.
- The gap ($E_G=5.65\text{eV}$) and the permittivity ($\epsilon_r=17$) of 9:1 HfAlO were extracted by ellipsometry and by $C-V_G$ measurements, respectively. We also consider that the bottom and top HTO are 4.5nm and 5nm thick respectively, which is in agreement with TEM observations.
- The shift between the conduction band of Si and HfAlO, ΔE_C , and the trapping cross section, σ , were fixed based on literature data: $\Delta E_C=2\text{eV}$ [13,14], $\sigma=10^{-18}\text{cm}^2$ [15,10].
- N_{st} , the trap density, is adjusted to fit the experimental saturation level.

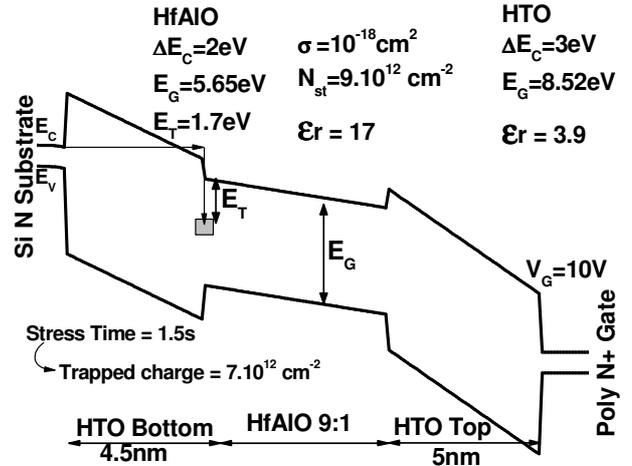


Fig. 7: Energy band diagram of OHO stack at $V_G=10\text{V}$ simulated in this work. Fitting parameters are indicated. The HfAlO thickness is 6nm, the concentration is 9:1. The charges trapped in the HTO-HfAlO interface are responsible for the different electric field values in the bottom and top oxide layers.

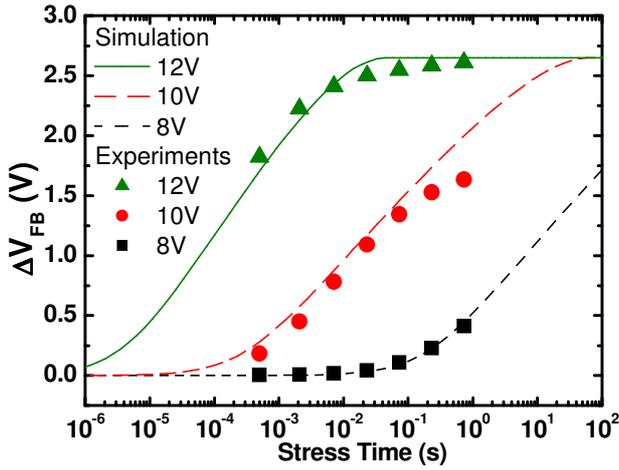


Fig. 8: Modeling of the trapping characteristics of OHO stack (HfAlO thickness is 6nm, concentration is 9:1), based on structure and parameters reported in Figure 7.

Based on these assumptions, we use the following equations to simulate the programming characteristics:

$$\Delta V_{th} = \frac{N_{st} \times ft}{Ct}$$

$$\frac{dft}{dt} = (1 - ft) \times (cn + ep) - ft \times (en + cp)$$

- cn/en and cp/ep are the electron and hole capture/emission rates which govern carrier exchanges between the traps and substrate.
- ft : trap occupation probability according to Shockley-Read-Hall statistics model [16].
- Ct : trap to gate coupling capacitance.

Figure 8 shows the experimental and the modelling trapping characteristics. We observe a very good correlation between the simulation and the experimental data for the three programming voltages, which validates our theoretical approach.

4. Conclusions

In this paper we investigated the intrinsic fixed charge and trapping phenomena happening under stress of HfAlO based interpoly dielectric stacks. We demonstrated that the fixed charge content increases with the Al concentration of the HfAlO layer. We showed that the trapping capability when the device is submitted to a constant voltage stress increases as the Hf ratio of the compound increases. Based on programming measurements, we proved that in our devices the electron trapping mainly occurs at the first interface, between the bottom HTO and the HfAlO layer, rather than in the volume of the high-k dielectrics. We also observed that the discharging rate of the previously trapped charges is more important for Hf-rich alloys. Finally, an analytical model based on a SRH approach allowed us to fit our experimental data and to extract the main trapping parameters of HfAlO high-k materials.

Acknowledgments

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