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# Operation and Stability Analysis of Bipolar OxRRAM-Based Non-Volatile 8T2R SRAM as Solution for Information Back-up

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## 1. Abstract

This work presents a Non-Volatile SRAM (NV-SRAM) cell, resilient to information loss. The cell features fast storage (20ns) for the operating voltage of 1.0V. The information is backed-up during POWER-DOWN/RECOVERY cycle in two bipolar Oxide Resistive RAMs (OxRRAMs). The proposed NV-SRAM is designed with an 8T2R structure using 22nm FDSOI technology and resistive memory devices based on HfO<sub>2</sub>. The stability and the reliability of the NV-SRAM cell is investigated by taking into account the variability of the transistors. It is shown that high R<sub>OFF</sub>/R<sub>ON</sub> is necessary to ensure reliable RECOVERY operation and high SRAM yield under cell area and power consumption constraints.

*Keywords: Resistive RAMs, NV-SRAM, Low power, Non-Volatile, Low leakage, FDSOI*

## 2. Introduction

The reduction of power consumption in integrated circuits (IC) becomes an ever more important challenge as the technology scales down and leakage currents increase. This is in particular true for portable systems which have the operation time limited by the battery capacity. In today's system on chip (SOC), the embedded SRAM can take even over half of the chip area and hence, its leakage can dominate the total power consumption. To reduce the static power dissipation, techniques like power-off of the unused logic blocks have been proposed [1, 2]. These approaches cannot be applied to memories though, as they will lead to the data loss. Scaling down the supply voltage (V<sub>DD</sub>) of memory blocks during standby is a potential solution. Its efficiency is limited however by the ever increasing transistor variability, not only making it difficult to predict the minimum V<sub>DD</sub> which can be applied to ensure no data loss, but also increasing the minimum V<sub>DD</sub> value [3].

An effective way of reducing the leakage currents is to use fast Resistive RAMs (RRAMs) in hybrid SRAM circuits, back-up the data from SRAM to RRAMs and switch the power off. This way the leakage is totally suppressed with no data loss. These hybrid memories, generally known as Non-Volatile SRAMs (NV-SRAMs), are able to combine high performance, low-voltage operation and low-leakage. NV-SRAM became an important research topic in the recent years [4-7]. The works presented in the literature, to the best of our knowledge, still do not fulfill the strict requirements of the SRAM in terms of speed, supply voltage and stability. The 16Kb NV-SRAM macro presented in [4] achieves a fast read access time, but the required high operating voltages do not comply with the modern SRAM technology [8]. Another group [5] proposed the use of MOSFETs to control the resistive switching devices. Their cell is fast at low voltages but the resistive devices used in this work are unipolar and therefore suffer from instability issues [9, 10] making the programming of resistances challenging at the circuit level. Yet another example of a NV-SRAM is the 6T2R cell [6, 7]. This cell however, suffers from stability degradation and high leakage coming from the resistive elements introduced in the cell architecture. This is caused by the formation of a direct current path during normal SRAM operation through the two RRAMs. Hence, in order to overcome these issues, a novel NV-SRAM architecture is required.

The influence of the transistor variability on the NV-SRAM operation has not been investigated yet. The variability is not mostly caused by the Random Dopant Fluctuations (RDF) [11-13] in the channel region, but also by other phenomena, such as oxide thickness variation [11, 14], Line Edge Roughness [11, 13, 15] and TiN grains with different workfunctions [12]. The relation between process parameters is typically defined as the Pelgrom coefficient (A<sub>VT</sub>) [16], which is proportional to the magnitude of threshold voltage variation (σ<sub>VT</sub>). For

32nm bulk CMOS designs,  $A_{VT}$  is over  $2.5\text{mV}\mu\text{m}$  [17]. Since the  $\sigma_{VT}$  is also inversely proportional to the root square of the product of transistor sizing [16] the SRAM becomes particularly susceptible to  $V_T$  variability as it typically uses smallest possible transistors to increase density. In this work the  $A_{VT}= 1.25\text{mV}\mu\text{m}$  corresponding to the 22nm FDSOI technology is assumed [18].

This work demonstrates a fast NV-SRAM cell operating at a relatively low voltage and which has the ability to eliminate the leakage current during a standby mode. The paper is structured as section 3 presenting the NV-SRAM structure and the cell operation, section 4 dealing with the static noise margin of the SRAM cell used in the NV-SRAM. Section 5 explains the influence of the  $V_T$  variability on the stability of the NV-SRAM cell.

### 3. NV-SRAM structure and operation

The structure of the non-volatile 8T2R NV-SRAM cell is presented in Fig. 1. The cell is designed with a classical 6T-SRAM cell ( $M_1$ - $M_6$ ) along with two additional P-type control transistors ( $CM_1$ ,  $CM_2$ ) connected between the data nodes (D, DN) of the SRAM cell and the OxRRAM ( $R_1$ ,  $R_2$ ).  $R_1$  and  $R_2$  are made accessible to the SRAM cell by  $CM_1$  and  $CM_2$ . TE1(2) and BE1(2) represent the top and bottom electrodes of OxRRAMs. The threshold voltages for the OxRRAM STORE and RESET operations are respectively 0.7V and -0.7V. In this work, a STORE operation on the OxRRAM corresponds to a logic '1' and the RESET corresponds to a logic '0'.

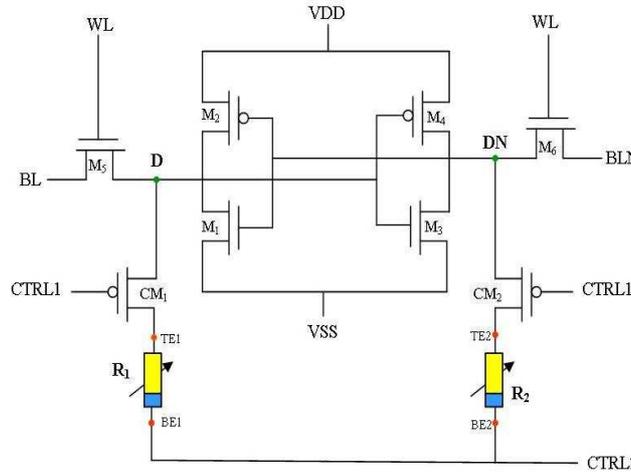


Fig. 1 Schematic representation of non-volatile 8T2R SRAM (NV-SRAM) cell.

All the simulations are performed using Eldo simulator. The results are validated on a 22nm CMOS-FDSOI technology process design kit developed by CEA-LETI. A bipolar OxRRAM model, calibrated on the experimental results obtained on  $\text{HfO}_2$  based devices [19], is used. The (W/L) of the pull-up, pull-down and the transfer transistor for the SRAM design are set to (100n/25n), (260n/25n) and (100n/25n), respectively. The cell is optimized as such it provides high speed (20ns per operation) while the transistors are operated at low voltage (maximum 1.1V).

The NV-SRAM cell operation follows the sequence: SRAM operation, RESET, STORE, POWER-DOWN, POWER-UP/ RESTORE. This cycle can be repeated as many times as necessary and its use is theoretically limited only by the reliability of the OxRRAM devices. The following sub-section explains the biasing conditions of different operation modes for a full sequence of SRAM operation – RESTORE cycle. Table 1 summarizes the biasing conditions of the control signals for all operations that involve OxRRAM.

Table1. Control signals during different operation phases of the NV-SRAM cell

	WL (V)	VDD (V)	VSS (V)	CTRL1 (V)	CTRL2(V)
<b>RESET</b>	0	1	0	0	1.5
<b>STORE</b>	0	1	0	0	0
<b>POWER DOWN</b>	0	1	1	1	1
<b>RESTORE</b>	0	1	0	0	1

#### 3.1. Normal SRAM operation

Normal SRAM operations (write/read) are not influenced by the presence of  $R_1$  and  $R_2$  as they are isolated from SRAM by  $CM_1$  and  $CM_2$  which remain OFF.

### 3.2. RESET

Before storing the information in OxRRAM, the RESET operation is performed to assure a high resistance state for the corresponding OxRRAM device. When the node D='0' and DN='1',  $R_1$  can be RESET by opening the control transistors  $CM_1$  and  $CM_2$  and putting CTRL2 to 1.5V. At this point, the resistance of  $R_2$  remains unchanged due to the low voltage drop on it (~0.4V). Whereas,  $R_1$  faces a negative voltage drop (0.8V) and RESET of  $R_1$  occurs as highlighted in Fig. 2a. Similar to  $R_1$  case,  $R_2$  can be reset if the SRAM nodes are flipped (D at '1' and DN at '0').

### 3.3. STORE operation

During the STORE operation, the logic state of the SRAM cell is stored in the  $R_1$ - $R_2$  pair. Consider that the node D has information '1' and DN has '0'. To back-up the information in the OxRRAM, the control transistors are turned ON by lowering CTRL1=0V and putting CTRL2=0V. The potential difference at the top and bottom electrode of  $R_1$  results in a positive voltage drop across  $R_1$  which sets this resistance to a low resistance state thereby, storing the information '1' in  $R_1$  (Fig. 2b). At the same time, since there is no voltage drop across  $R_2$ , its value remains unchanged in high resistive state thereby storing the value '0'.

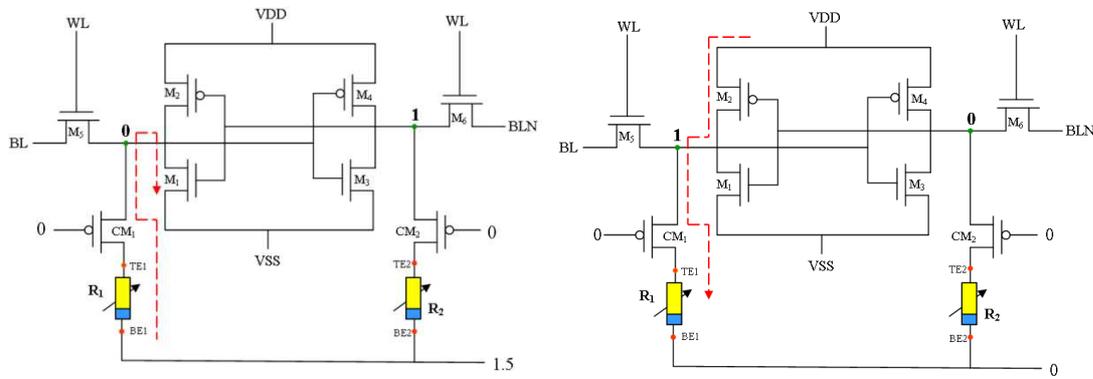


Fig. 2 (a) RESET operation (b) STORE operation.

### 3.4. POWER-DOWN operation

Normally, a POWER-DOWN in a circuit is performed by putting all the control lines to ground. In this work, however, POWER-DOWN operation is performed by raising the VSS pin of the cell to VDD and hence, the nodes D and DN are pulled up to VDD. This is basically done to avoid resetting the state of the OxRRAM during the RESTORE operation that would cancel the resistance asymmetry between  $R_1$  and  $R_2$  and would compromise the correct level restoration. The control lines – BL/BLN and CTRL2 are also raised to VDD to reduce the leakage through the transfer transistors and control transistors respectively. It is observed that a considerable time (2.8 $\mu$ s) is required to totally discharge all the capacitances of the NV-SRAM cell (see Fig. 3).

### 3.5. RESTORE operation

The logic state of the SRAM has to be restored after power-off. CTRL1 is lowered to the ground turning ON the control transistors ( $CM_1$ ,  $CM_2$ ). The signal VSS is put down to 0V with a delay of 5ns with respect to CTRL1. CTRL2 is kept at VDD as it was during the POWER-DOWN. The node D is strongly maintained at logic '1' due to the low resistance of  $R_1$ . Simultaneously, due to the resistance difference,  $M_3$  pulls the DN node down to '0', restoring in this way the logic in the cell (Fig. 3).

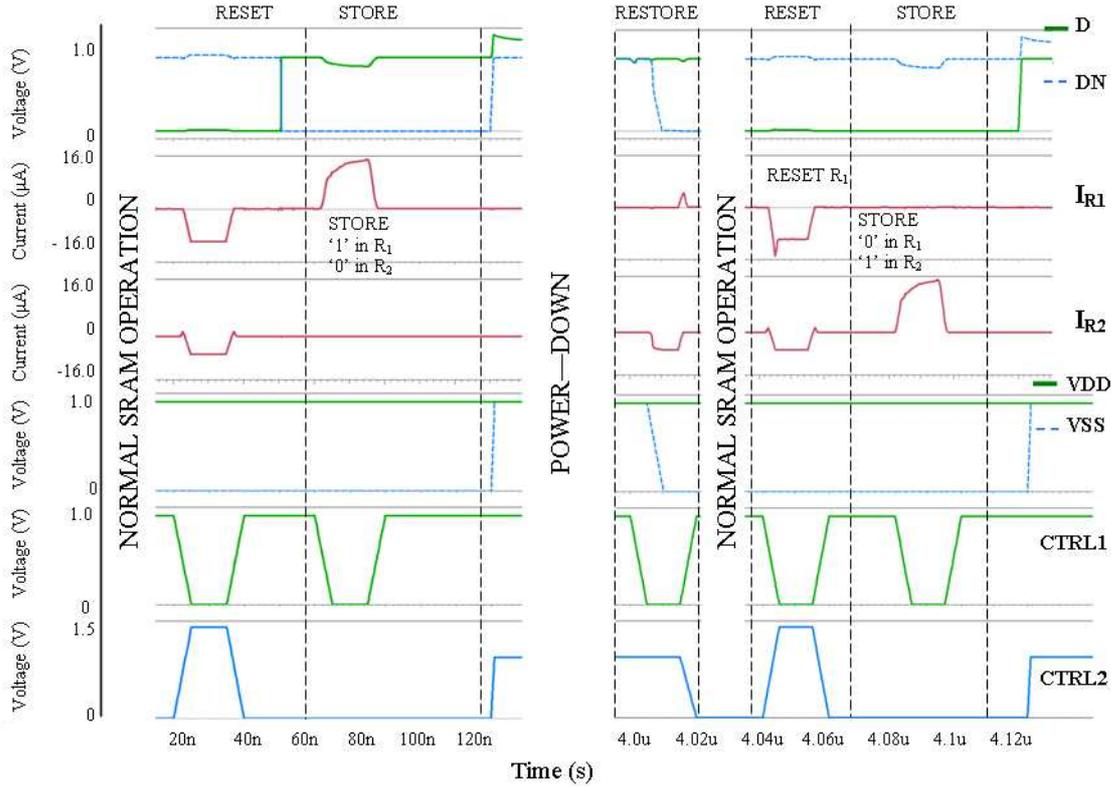


Fig. 3. Waveform for a POWER DOWN – POWER UP cycle.

### 3.6 RESET/STORE mechanism

Resistive RAMs are known to be fast ( $\sim 5\text{ns}$ ) [20], but they are limited by their lower reliability with respect to CMOS. The best performance up-to-date has been demonstrated by the resistive switching device developed by Samsung exhibiting  $10^{12}$  cycles of endurance [20] which is about four orders below the endurance of SRAM cell. To overcome this reliability issue and extend the lifetime of the system, the frequency of data back-up in RRAMs has to be minimized. There are various methods, at the circuit level, that allow avoiding the redundant writing of OxRRAMs and preserve the reliability to a certain extent. The technique developed in this work of RESET-ting the OxRRAMs just before the STORE operation, is used to avoid the unnecessary writing of the resistive devices. For example, we assume that we have  $D='1'$  and  $DN='0'$  before POWER-DOWN (i.e.  $R_1$  is low and  $R_2$  is high). After the POWER-UP, the levels are restored. Next, a new sequence 'normal SRAM operation-RESTORE' starts and the SRAM data is updated. Now, suppose the new data that has to be stored in OxRRAM is  $D='1'$  and  $DN='0'$ . In this situation, during the RESET operation that precedes STORE, when the CTRL2 is biased at 1.5V,  $R_1$  remains at the same state (i.e. low resistive state) and the state of  $R_2$  remains same as well (i.e. high resistive state). This RESET/STORE mechanism prevents the unnecessary flipping of the OxRRAM devices and improves the mean time between failure of the NV-SRAM cells.

## 4. SRAM cell static noise margin

The 6T SRAM cell core of the NV-SRAM has to be optimized such that even under the worst-case conditions, it still functions properly. The sizing of the SRAM cell (see section 3) does not comply with the regular sizing of the PMOS, which is usually kept at minimum due to the area constraints. The reason for having a wider PMOS transistor in the 8T2R NV-SRAM comes from the requirement of a few  $\mu\text{A}$  current in order to write the OxRRAM during STORE operation. Since in the 22nm FDSOI technology used in this work, the PMOS has a high threshold voltage ( $V_T$ ) of approximately 500mV, the STORE current could only be met by increasing the PMOS width. It can be expected though, that should the PMOS  $V_T$  be lower, the use of a minimum sized PMOS could be possible as well. The pull-up and the transfer transistor are considered to have the same strength to enable a reasonable value for the Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM). The Static Noise Margin (SNM) [21] is the key parameter in the SRAM analysis and can be defined as the highest value of noise between the two cell inverters for which the proper functionality in each operation mode is maintained. In the graphical representation SNM can be defined as the smallest (for retention and read) or the largest (for write) square which can be fitted between the "butterfly curves" consisting of the inverted and non-inverted curves corresponding to respective operation mode (Fig.4). With the above-mentioned sizing (section

3), the NV-SRAM cell has a pull-up ratio of 1 (defined as the ratio of W/L between the pull-up and transfer transistors) and a cell ratio of 2.6 (defined as the ratio of W/L between the pull-down and transfer transistors) ensuring a RSNM of 180mV (Fig. 4(a)) and WSNM of 320mV (Fig. 4(b)). The addition of the control transistors and the OxRRAM does not affect the normal operation of the SRAM cell as well as the SNMs. This is made possible due to the use of  $CM_1$  and  $CM_2$ , which block the current leakage path through the OxRRAMs during the normal operation of the SRAM cell.

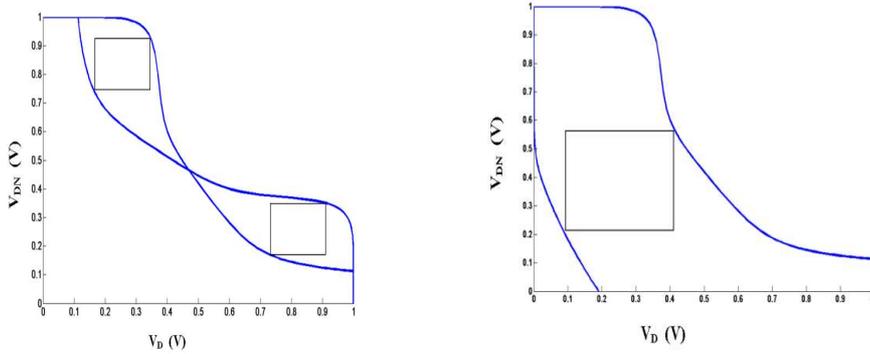


Fig. 4 (a) Static read noise margin:  $RSNM=180mV$  (b) Static write noise margin:  $WSNM=320mV$

## 5. The influence of $V_T$ variability on the stability of 8T2R SRAM cell

The influence of  $V_T$  variability on the Non-Volatile OxRRAM- based SRAM operation has not been investigated so far and can be expected to be a major constraint for obtaining a high yield. This is caused both by the potential difficulty in ensuring reliable NV-SRAM-specific operation modes (STORE, RECOVERY, RESET) if mismatch is considered and by the unorthodox 6T SRAM core sizing, with a larger than minimum PMOS which degrades write stability in the typical SRAM operation. The key yield-limiting factor of 8T2R NV-SRAM is the reliability of the RECOVERY operation as it strongly depends on the  $R_{OFF}/R_{ON}$  ratio obtained during STORE and hence can be unsuccessful. STORE operation never fails as the positive voltage applied on an OxRRAM device in OFF state is always going to lower its resistance by some value. However, under the random  $V_T$  variations, the obtained  $R_{ON}$  for a fixed operation time will vary and therefore, the RECOVERY reliability may be compromised. The optimization of STORE operation from the cell  $R_{OFF}/R_{ON}$  maximization perspective under timing and transistor sizing (and hence stability) constraints becomes therefore the starting point for the 8T2R NV-SRAM reliability analysis.

### 5.1. STORE operation: influence of cell sizing and timing on $R_{OFF}/R_{ON}$ ; Impact on SNMs

The  $R_{ON}$  value that can be obtained in the STORE operation is determined by 2 key parameters: the sizing of the pull-up transistor in the SRAM cell, here analyzed only through its width ( $W_{LP}$ ), and by the time of STORE operation. Figure 5 presents the dependence of the OxRRAM resistance as a function of STORE operation time for different values of  $W_{LP}$ . The decrease of resistance can be separated in two different parts regardless of the  $W_{LP}$ : i. the abrupt resistance drop in the first 20ns; and ii. the saturation of the resistance value as the STORE time increases. Figure 6 presents the dependence of  $R_{ON}$  as a function of  $W_{LP}$  extracted at different STORE periods. It can be noted, that the increase of  $W_{LP}$  has a significant impact on the shape of curves in Fig.6, decreasing the minimum achievable  $R_{ON}$  value and therefore increasing the resistance drop ( $R_{DROP} = R_{OFF} - R_{ON}$ ) for a fixed STORE operation time. The sensitivity of  $R_{ON}$  to STORE time decreases by a factor of 2 as the  $W_{LP}$  increases from 80nm to 200nm (Fig. 6).

The extracted  $R_{DROP}$  as a function of STORE time shows clearly a threshold like behavior for both widths of the pull-up transistor (Fig. 7). Once the decrease of the resistance enters the saturation region (Fig. 5) the time that is necessary for obtaining a significant  $R_{DROP}$  (i.e. low  $R_{ON}$  value and hence a high  $R_{OFF}/R_{ON}$ ) exponentially increases (Fig. 7). A consequence of the results presented in Figs. 5-7 is that if a specific, high,  $R_{DROP}$  from the  $R_{OFF}$  is targeted, either the STORE time or  $W_{LP}$  have to be increased. The former solution however, would cause a significant increase in the power consumption during STORE operation, since the currents needed for writing the OxRRAMs are in the order of at least a few micro-amps. The latter solution would lead to the increase of the cell pull-up ratio, decreasing the SRAM cell reliability during write operation. The magnitude of this stability drop will also depend on the initial  $V_T$  ratio between the NMOS and PMOS transistors [3], but should the  $W_{LP}$  increase from the 100nm to 200nm, it will always be non-negligible. In our case, with the  $V_{TP}$  approximately 50% larger than the  $V_{TN}$  and the access NMOS width of 100nm, changing  $W_{LP}$  between 100nm and 200nm leads

to the stability factor drop (represented as the  $\mu/\sigma$  extracted from the statistical distributions of write static noise margin in such a way, that the tail is properly evaluated) from 12.3 to 9.22. In order to meet the typical  $6\sigma$  yield target, the stability factor ( $\mu/\sigma$ ) should be higher than 6. In this particular case the SRAM yield is therefore still maintained, but the magnitude of this stability factor drop indicates a high importance of this analysis. The only way to avoid an excessively high  $W_{LP}$  and a long STORE time is therefore to reduce the targeted  $R_{OFF}/R_{ON}$ . This is in turn limited by the minimum  $R_{OFF}/R_{ON}$  required to ensure the reliability of RECOVERY operation, as explained in details in the following section.

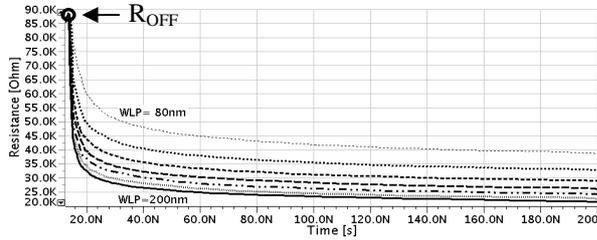


Fig. 5.  $R_{ON}$  vs. time during STORE operation for various  $W_{LP}$  in the 80nm to 200nm range.

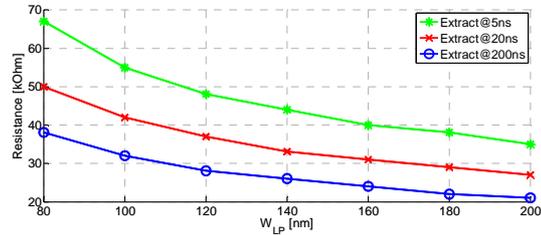


Fig.6  $R_{ON}$  during STORE operation vs. width size of the load PMOS extracted at 5ns, 20ns, and 200ns.

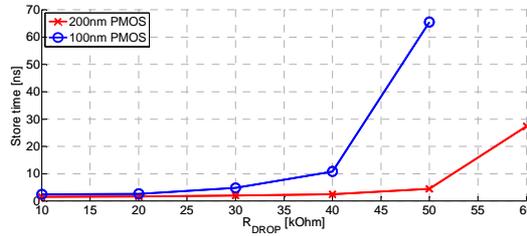


Fig.7 STORE time vs.  $R_{DROP}$  for  $W_{LP}$  of 100 nm and 200 nm.

## 5.2 RECOVERY operation: reliability analysis

In order to investigate the stability of RECOVERY mode, a worst case  $\pm n\sigma_{VT}$   $V_T$  variation was applied to each transistor in the SRAM cell, thus creating a situation where each device is working against the recovery of the correct values in the nodes of the SRAM cell. Increasing the value of  $n$  leads to a larger ‘worst case’ mismatch and allows analyzing the  $n\sigma_{VT}$  point where the recovery operation fails. The data recovery operation in our proposed scheme does not affect the resistance value of the OxRRAM, so the use of passive elements should correspond exactly to the case with OxRRAM devices and allow performing a general case analysis of recovery mode stability. Moreover, substituting the OxRRAM devices with resistors allows including  $R_{OFF}/R_{ON}$  cases not covered by our OxRRAM model, which is based on experimental data. Figure 8 depicts the values of  $n\sigma_{VT}$  fail points for different  $R_{OFF}/R_{ON}$  ratios. As depicted in Figs. 5-7, a high resistance drop can be obtained only if high  $W_{LP}$  and long delay values are used. However, even for  $W_{LP}=200\text{nm}$  and the delay of 200ns, the  $R_{ON}$  during STORE reaches only 21k $\Omega$ , corresponding roughly to the  $R_{OFF}/R_{ON}=4$ . The worst case mismatch analysis reveals that for this resistance ratio the RECOVERY operation fails for  $n=2$  (Fig. 8) which is quite low from the stability point of view.

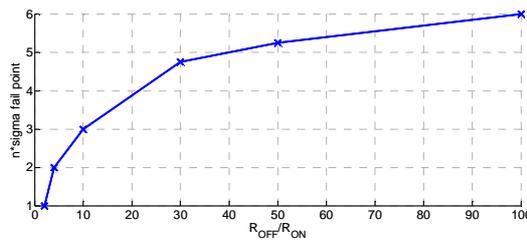


Fig.8 Variation of  $n\sigma_{VT}$  fail point versus the  $R_{OFF}/R_{ON}$  ratio in the worst case variation analysis

### 5.3 Towards a 6 $\sigma$ NV-SRAM cell

In order to correlate the worst-case analysis result with a typical yield evaluation, a Monte Carlo (MC) simulation with random Gaussian variation applied to all transistors of the SRAM cell was performed. This MC simulation was performed for a  $R_{OFF}/R_{ON}=4$  corresponding to  $n=2$ , as this is the maximum resistance ratio obtainable in our 8T2R NV-SRAM. In this analysis, 41 fails in 10000 samples were observed, corresponding approximately to a 3 $\sigma$  yield. Since in the typical SRAM design, a yield of 5 to 6 $\sigma$  is targeted, it can be expected that in the worst case analysis (performed in section 5.2 for RECOVERY operation) the value of  $n$  should be equal to at least 3 or 4. However, as depicted in Fig.8, the value of  $n$  equal to 3 and 4 occurs only for a  $R_{OFF}/R_{ON}$  of 10 and 20, respectively.

Yet another constraint for a reliable OxRRAM- based SRAM operation becomes evident in the MC analysis of the STORE mode. Fig.9 depicts the spread of the resistance vs. time curves obtained from a MC simulation ( $W_{LP}=100nm$ ) showing a roughly  $\pm 4k\Omega$  variation for a fixed STORE time. As it was previously mentioned, in order to obtain a sufficient and fixed stability in RECOVERY mode, a specific and low value of  $R_{ON}$  should be targeted to ensure high  $R_{OFF}/R_{ON}$  ratio. Fig. 10 depicts a set of histograms from a 10000 sample MC analysis for a  $W_{LP}=100nm$  demonstrating the spread of STORE time required to obtain a  $R_{DROP}$  between 10k $\Omega$  and 50k $\Omega$ . Clearly, if low  $R_{ON}$  is targeted (high  $R_{DROP}$ ) to satisfy RECOVERY conditions, the spread of the required STORE time increases significantly, especially as the saturation part (above 20ns in Fig.9) of the resistance curve is reached.

Figure 11 depicts the mean and worst case far tail STORE time required to obtain a range of  $R_{DROP}$  for the  $W_{LP}$  of 100nm and 200nm extracted from the similar MC simulations as used to obtain results depicted in Fig. 10. The stability of the RECOVERY operation, as demonstrated before, strongly depends on the minimization of the  $R_{ON}$ . In order to ensure that the expected, low  $R_{ON}$  is obtained, the length of the CTRL1 signal should be extended accordingly up to the worst case STORE time in the far tail of statistical distribution (see Fig. 10 for 50k $\Omega$   $R_{DROP}$ ). The minimization of the difference between the mean and the worst case far tail STORE times is therefore important to reduce the power overhead coming from the operation time extension required for reliable RECOVERY. As depicted in Fig.11, increasing  $W_{LP}$  is an efficient solution to minimize this problem. This is due to the fact, that the PMOS has a very high influence on the resistance curve during store operation (Fig.6) and hence, increasing its width reduces the spread of the resistance plot (Fig. 9) due to inverse root square dependence of transistor sizes on the  $\sigma_{VT}$ , leading to the lower variation of the PMOS  $V_T$ . Moreover, in order to limit the influence of variability on the worst case delay,  $R_{ON}$  extraction has to be limited exclusively to the region where the  $\frac{\delta R}{\delta t}$  is high (Fig 9), which creates a strong limitation on the lowest achievable  $R_{ON}$  and does not allow to increase it further by extending the STORE operation time. As a result, the only efficient method to obtain a high  $R_{OFF}/R_{ON}$  ratio and hence a high RECOVERY stability, is either by increasing the  $W_{LP}$  or improving the OxRRAM itself. Since the former is strongly limited by the low cell area and SRAM write stability, it can be concluded, that the OxRRAM development has to strongly focus on the increase of  $R_{OFF}/R_{ON}$  ratio to allow obtaining a sufficient  $R_{DROP}$  within the high  $\frac{\delta R}{\delta t}$  region, corresponding to the  $R_{OFF}/R_{ON}$  of 10-20 for low STORE time periods. Such a high resistance ratio raises a potential challenge for the design of NV-SRAM cell, but most importantly on the OxRRAM device itself. A complete strategy that could be used for the improvement of the OxRRAM devices is composed by the following steps: use FORMING operation to obtain high  $R_{OFF}$  values [22, 23] and use  $W_{LP}$  and the STORE timing to obtain the desired low  $R_{ON}$  that satisfies the high  $R_{OFF}/R_{ON}$  condition required to obtain a 5-6 $\sigma$  yield.

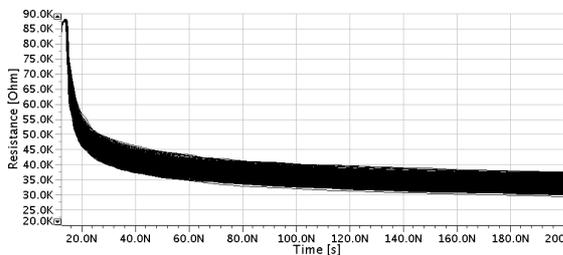


Fig.9 OxRRAM resistance vs. time during STORE operation. Data obtained from the MC simulation random Gaussian  $V_T$  variation applied to all SRAM cell transistors, for  $W_{LP}=100nm$ .

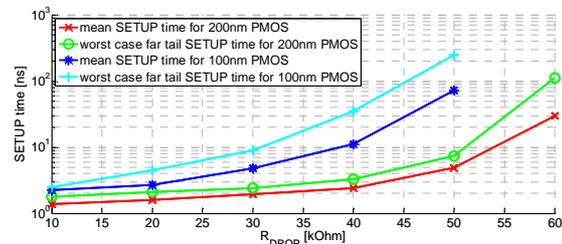


Fig.11 Mean and worst case STORE time vs.  $R_{DROP}$ . Data obtained from 10k MC simulations for  $W_{LP}$  of 100nm and 200nm.

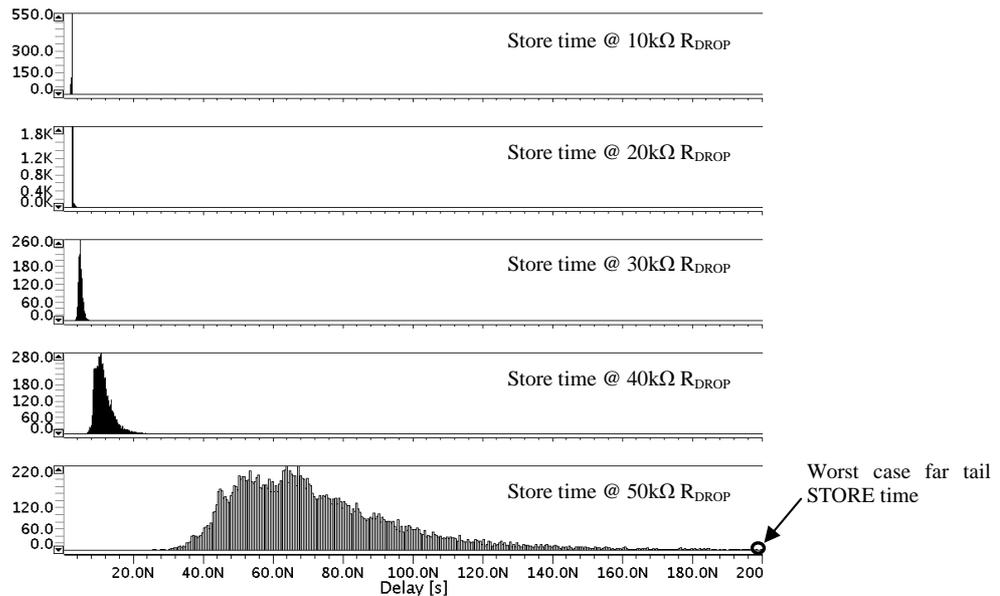


Fig.10 Distributions of STORE time required to obtain various  $R_{\text{DROP}}$  in STORE operation obtained from a 10k samples MC simulation for  $W_{\text{LP}}=100\text{nm}$ .

## 6. Conclusion

A 8T2R Non-Volatile SRAM cell having capability of fast storing and restoring information was presented in this work. This cell is designed with a 22nm FDSOI PDK for the CMOS transistors and an OxRRAM model based on  $\text{HfO}_2$  devices. The cell is operational for “normal SRAM-RESET-STORE-POWER DOWN-RESTORE” cycle. The cell operates at high speed (20ns pulses) and low voltage having 1.1V as maximum voltage drop on the transistors. For the first time the analysis of  $V_T$  variability on the stability of 8T2R NV-SRAM cell was performed. It was revealed that  $R_{\text{OFF}}/R_{\text{ON}}$  of at least 10 (20) is necessary in order to ensure sufficient reliability of the RECOVERY operation at a typical SRAM yield of  $5(6)\sigma$ . In order to meet this yield value, due to the constraints coming from the cell area, power consumption and write stability the OxRRAM device development has to focus on the maximization of the  $R_{\text{DROP}}$  in the high  $\frac{\delta R}{\delta t}$  region.

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