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Contribution to Silicon-Carbide-MESFET ESD robustness analysis

T. Phulpin, K. Isoird, D. Trémouilles, P. Austin, X. Perpinyà, J. León, M. Vellvehi

Abstract—In this work, ElectroStatic Discharge (ESD) tests are performed on SiC MESFETs in order to understand their physical behavior and failure mechanisms during such stresses. The purpose is to point out advantages and drawbacks of this technology, paying special attention to aspects related to its possible commercialization and reliability. Three MESFETs designed to be integrated as a driver in monolithic SiC systems, featuring some ESD internal protection are investigated. Different configurations on ohmic and Schottky contacts are analyzed. Lock-in thermography is carried out for the physical failure location. With TCAD Sentaurus simulation, it allows to determine the nature of the defects on the damaged areas. Hypothesis on the failure mechanism as SiO₂ breakdown or SiC sublimation are presented. Solutions to increase the ESD robustness such as a Zener diode integration or the use of Al₂O₃ dielectric for passivation are therefore proposed in this article.

Index Terms— ESD, MESFET, Passivation, Protection, Reliability, Integration, SiC, Schottky contact, Schottky diode, TLP, Zener diode

I. INTRODUCTION

RELIABILITY and robustness of power semiconductor devices are primordial in any final application. In this regard, ElectroStatic Discharge (ESD) robustness is one of the critical aspects. ESD induce destructive failures or aging in such devices, reducing their life time [1]. Thus, understanding the failure mechanisms during ESD events is crucial to improve robustness, especially in new emerging materials such as Silicon Carbide (SiC) [2]. SiC is a promising wide band gap material for manufacturing power semiconductor devices. It allows converters miniaturization and power losses reduction thanks to, among other physical properties, its high voltage breakdown and high operation temperature capability [3]. However, although SiC is pointed out as a good candidate for integrated systems working for example near motors, its behavior during ESD stresses is scarcely reported, analyzed, and explained in the literature. Only one work dealing in this subject was found [4]. The main difficulties to investigate in this field are due to high stresses produced by ESD tests, which suddenly breaks down the device.

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This work intends to study under ESD tests, several SiC MESFETs specifically designed for integrated power systems working under harsh environment conditions.

This paper is organized as follows. First, the devices (based on ohmic and Schottky gates) and their ESD workbench are presented. Next, in Section III, the ESD results are discussed. In Section IV, a failure analysis using lock-in thermography, jointly with Technology Computer Aided-Design (TCAD) simulation, is carried out to determine their failure mechanism. Finally, in Section V, more rugged structures against ESD events are proposed.

II. PRESENTATION OF THE STUDIED DEVICES

The following parts of the paper will present these devices and the test setup used for the evaluation of their ESD robustness.

A. Three different topologies

Because of the difficulty to obtain homogenous doping along SiC material [5], mesa configuration is often used to optimize the dopant repartition and the termination junction of SiC power devices. Mesa isolation also brings an efficient electrical isolation but planar device makes this integration easier. Circle isolation with a high P doping layer is then preferred.

The studied devices measure 80 μm large and 160 μm long and are made of 0.5μm N-channel doped at 10¹⁷cm⁻³ with phosphorus over a 5μm P-layer doped at 5.10¹⁵ cm⁻³ with Boron. The N channel is circled with a P⁺ layer at 10¹⁹ cm⁻³ for the lateral isolation, which provides with the P-layer a RESURF (REDuced SURface Field effect [6]) for the electric field repartition. Phosphorus at 10¹⁷ cm⁻³ (N⁺) is added for increasing the source and drain contact. A second gate called body is in contact with the P-layer and can be used to increase transconductance of the device.

The three MESFETs are essentially identical but internal protection was added (Fig.1.). One MESFET is used as reference one (MR). The second has a Zener diode on the drain electrode (MZD) in order to derive an overcurrent through the body layer. On their layout, we can observe a body layer (in red) circling the transistor, with a 2 μm N⁺-P⁺ juxtaposition for MZD for building the Zener diode (Fig.2.). The third device has no Zener diode but is protected with a Schottky diode on the drain electrode (MSD), allowing the drain current only in one way. It requires more potential to be triggered on and avoids any problem of inversion polarization.

A layout of a planar MEFET with its respective internal protection in Fig.3.

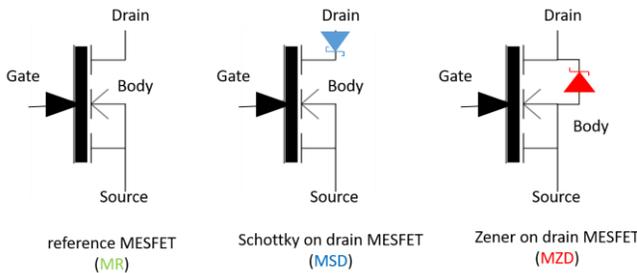


Fig.1. Planar MEFET with internal diodes protection

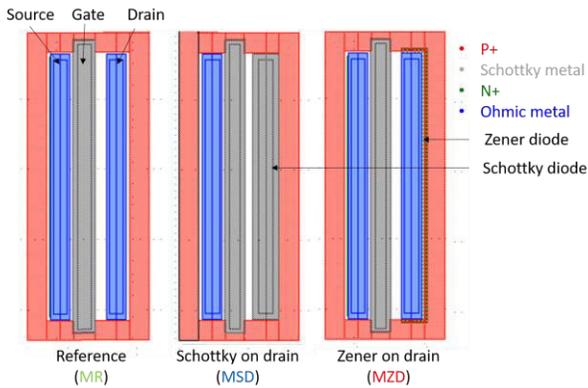


Fig.2. MR, MSD and MZD layout

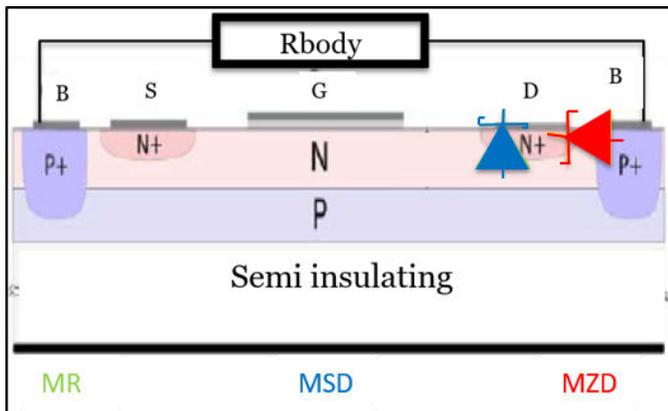


Fig.3. Schematic cross section of MR and MSD and MZD with their internal protection

Regarding device static measurement with V_{gs} floating, MSD presents a slight shift because of the diode conduction in comparison with the others devices, which have the same characteristics, depending on the different devices (Fig.4.). For the three signals, current saturation is around 16 mA for a range of 0-15 V. The threshold voltage is calculated at -15V with this equation:

$$V_{blocked} = (W^2 * q * Nd) / (2 * \epsilon) = -15V$$

With $W=0.5 \mu m$, $q=1.6*10^{-19} C$, $Nd=5.5*10^{16} cm^{-3}$ and $\epsilon=9,66$

Devices were characterized with $J_{ds_max}= 60.68 mA/mm$, $J_{ds_leak}= 116 \mu A/mm$ and $J_{gs_leak}= 2,68 \mu A/mm$ [6].

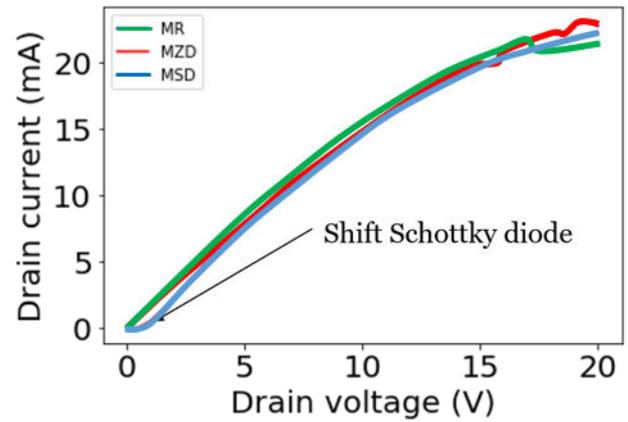


Fig.4. Ids-Vds characteristics for MR and MSD

Regarding device dynamic measurement, impedance is measured with AC signal of 0.5 V and DC signal of 0 V. A phase around 90° is observed at 10 MHz with a maximum module value at 1 MHz. This figure indicates presence of passive element corresponding to a capacity, as it was demonstrated in [7]. Model used for the impedance measurement is therefore a capacitance in parallel with a resistance (Fig.5.) [8].

Drain-gate dynamic measurements (1kHz-1MHz) for MR and MZD are almost similar for internal capacitance (Fig.6.). 2 kΩ are added by the Zener diode integration for resistance measurement. With frequency, C_p is constant whereas R_p increases due probably to the carrier saturation velocity. MSD is not plotted because its imaginary part is not comparable due the Schottky diode capacitance in serie with the drain-body measurement.

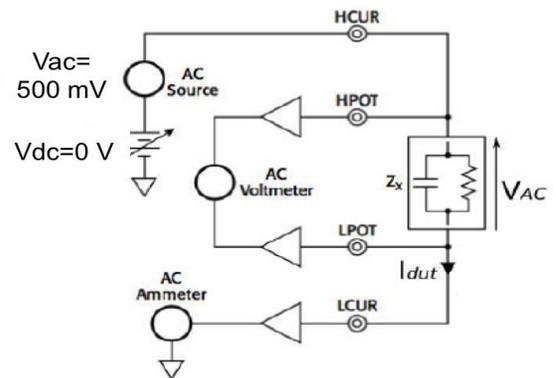


Fig.5. Schematic of the setup used for the impedance measurement [8]

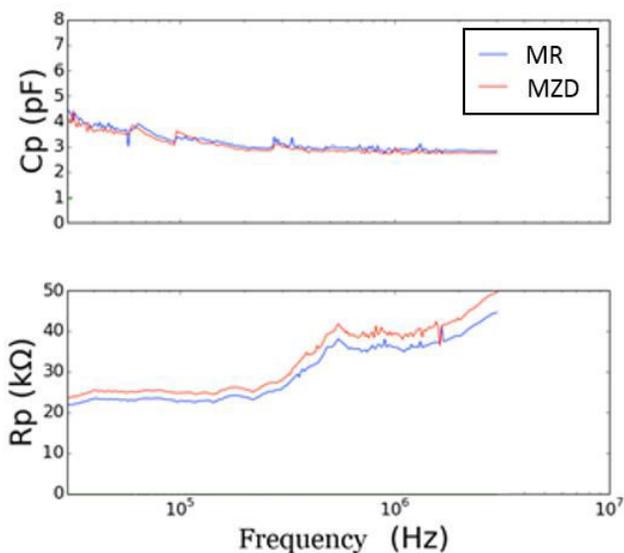


Fig.6. Impedance measurements on SiC MESFET MR, MSD, MZD

B. TLP and HBM test

Tests were realized with a Transmission Line Pulse (TLP) equipment setup to analyze the electrical behavior of the MESFET during ESD. HBM (Human Body Model) test is the standard test used for qualification in JEDEC ESD robustness. However, this test doesn't permit to study the electrical characteristics during experiments. TLP and HBM difference comes from the shape signal realized within a 100 ns step for TLP and a capacitor discharge for HBM. During experiments, stress amplitude is increased until electrical or physical failure. For TLP test, experiment is stopped as soon as failure I_{ds} - V_{ds} measurement, realized after each step, is modified by about 20% of the initial reference curve.

III. MEASUREMENT AND RESULTS

TLP stresses are realized at ambient temperature on each device and results are examined to understand the failure mechanism. First results are commented for a stress applied on the drain with the gate floating (ON state), then in OFF state condition. Eventually the stress is applied directly on the gate electrode for the Schottky contact ESD robustness comparison.

A. Stress on drain (ON state)

TLP stresses are applied on drain electrode with gate and body electrode floating. Results are displayed in the Fig.7. Each point corresponds to a stress level and stars indicate the destructive stress. In the contrary of silicon, reference measurement between each measure (here called leakage measurements) are not a failure indicator as seen in Fig.8. Indeed although devices are physically broken, only a small shift is observed. Visual indications have then to be used to stop the test as soon as a failure takes place.

TLP result shows similar behavior for MSD and MR with tens volt dispersion on voltage failure level, and with a failure at higher voltage value but very low current level. As the

maximum drain current measured is around 20mA for a voltage of 250V, the power sustain by these MESFETs is in both case around 5W.

In the contrary, MZD has still the same TLP characteristics, with a current increasing at 115V, until 1A and 130V. The power sustain is then around 130 W. In this case, the device conducts the ESD current and is not physically degraded.

Standard HBM test confirms a better MZD ESD robustness. Whereas MR and MSD have the same behavior with a failure observed visually at approximately 420 V, MZD can withstand around 1250 V and 0.9 A even if his electrical characteristics are not modified. The JEDEC classification, which is the reference in ESD, is then different with class 1C for MZD instead of class 1A for MR and MSD [9]. This better ESD classification allows the main works in laboratory without specific protection with MZD. In addition after the HBM test, failure looks different for MZD because the current increase, signature of the failure in case of MR and MSD was not detected in HBM I-V measurement. However, a failure is physically observed and looks similar from the optical point of view with the same localization.

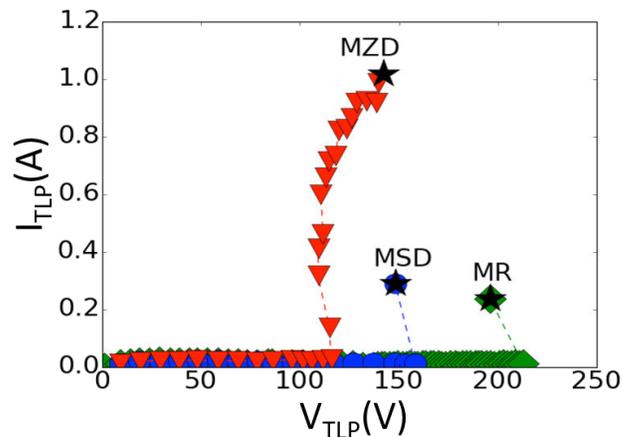


Fig.7. SiC MESFET TLP between drain and source with $V_{gs}=0V$. Stars are represented the failure point

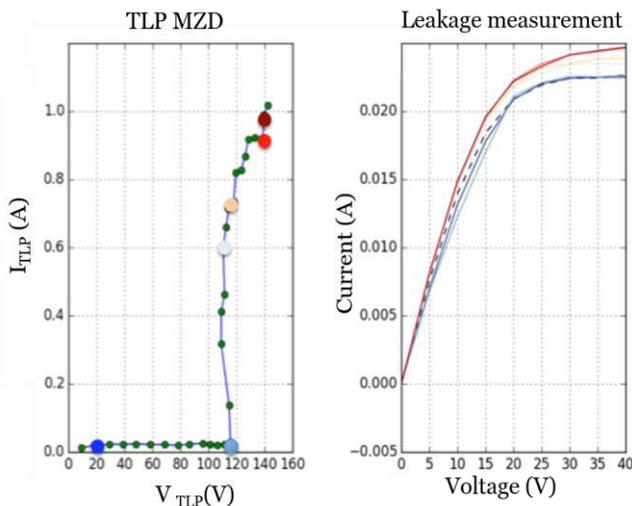


Fig.8. DC leakage curve during TLP experiment on SiC MZD

B. Stress on drain (OFF state)

An external generator supplying -15V on gate electrode is added to our TLP benchmark. The measured off-state leakage is 0.004mA in the gate biased condition of -15V, indicating the device is blocked..

Results of the TLP test on the drain are reproducible and show three different behaviors (Fig.9). MR and MSD present now a different electrical behavior with a different failure mechanism. Indeed, MR has a current increase before failure, and handles 0.4 A and 280 V before failure, which corresponds to 112 W. MZD is broken at 0.5 A and 230 V, for power almost similar than in the previous experiment and almost equal to MR failure power. However the current hasn't the same behavior in both cases with a different internal resistance evolution. Results and failure are similar than previously for MSD without any overcurrent.

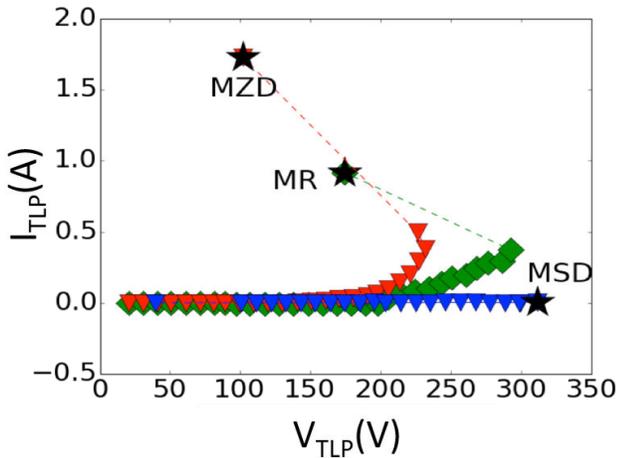


Fig.9. SiC MESFET TLP between drain and source, with $V_{gs}=-15V$ and body floating. Stars are represented the failure point

C. Stress on gate

Stress is applied on Schottky contact between gate and source electrodes with the others terminals floating. TLP result presents a failure in direct mode at 100 V with 0.2 A (20W) and only 230V with 0.02A (5W) in reverse mode (Fig.10.). The TLP failure power level is equal in reverse mode to MSD failure power level.

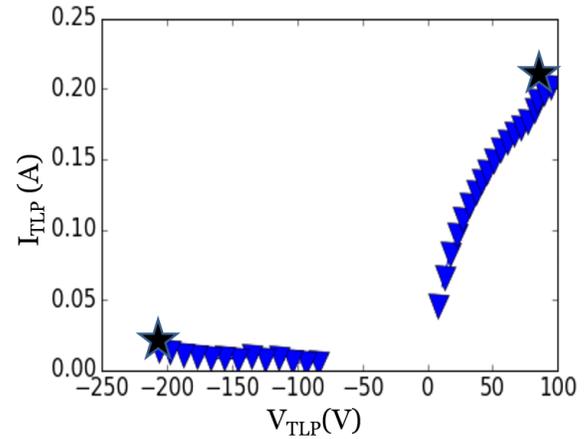


Fig.10. One negative and one positive TLP stress between gate and source electrode for SiC MESFET with drain floating. Stars are represented the failure point

D. Sum up of results

The following table (Tab.1.) sum up the different result of TLP voltage and power sustain by the stressed device.

Tab.1. Results after TLP stress experiments on SiC MESFET

Stress	MR	MSD	MZD
Drain with $V_{gs}=0V$	$V_{br}=200V$ $P_{br}=5W$	150V 5W	115V 115W
Drain with $V_{gs}=-15V$	280V 112W	310V 5W	230V 115W
Gate with Drain floating	100V 20W	-	-

IV. FAILURE ANALYSIS

In a first part, Lock-in thermography is used as failure detector. It allows in our case to separate in two groups origin of the failures and it brings correlation between electrical and physical failure. Then for the failure analysis, microscopic observations are used and are compared to TCAD Sentaurus simulations. This analysis contributes to the failure mechanism understanding.

A. Lock-in thermography

Lock-in thermography (LIT) is a general approach capable of locating the physical failure after an ESD event, based on the frequency modulation of heat sources or hot spots, which correspond to faulty locations on the device surface. After an acquisition of the thermal field and following a data lock-in postprocessing strategies, thermal amplitude and phase lag at one frequency are measured [10] and such heat sources are detected. Concretely, lock-in thermography can be implemented with an Infrared (IR) camera, recording IR photon emission of the studied device with a high spatial resolution (5 μm).

This work has been done at CNM laboratory. Samples have been biased with a sine-like signal at a given frequency to carry out the lock-in detection. After data collection and mathematical convolution [9], amplitude and phases are analyzed at the biasing frequency. Only amplitude results are

presented here, as they are of significance for the intended study: locate hot spots as indicators of physical failure positions. Scale of infrared emission is the same for all graphs, without legends because the value measured are related to the average of each measure

TLP stress creates a failure on MR (Fig.11.) but failures are not revealed by the LIT (Fig.12.): no modifications are observed before and after stress whereas a failure is visually observed with a microscope. We can observe on the figure that most of current is going uniformly through the gate electrode, which is lighter between the drain-source electrode. MSD has a similar behavior. However, for MZD, results are different as shown in Fig.13. and Fig.14. With the emission scale, we can just deduce that a failure occurs in SiC and where it is localized. The failure nature can not be easily interpreted but confirms the difference of mechanism with MR or MSD.

The colored LIT signal for MZD is concentrated at the failure localization. A hypothesis of the different LIT signal of MZD before and after the failure is that electric field is concentrated all around the defect as shown in Fig.15. In this simulation, we can observe an example in 2D, with two lateral NPN $10\mu\text{m}$ -device polarized at 50V: one with a hole, corresponding to the observed defect in SiC [12] and one without. Result of this simulation is that electric field, related to current distribution, is more concentrated around the hole and presents stronger values for the “hole” device than for the “normal” device. Hence it justifies the current increase in the DC leakage current measurement during the TLP test (Fig.7.).

The LIT analysis indicates probably the internal defect in case of MZD, and external defect in case of MR and MSD. This analyze justifies the LIT representation and the slight DC current leakage increased noticed after ESD stress for MZD. In any cases, the LIT allows detecting the defect creation on SiC and permits the localization of the failure even if the accuracy is limited by the camera’s resolution ($5\mu\text{m}$).

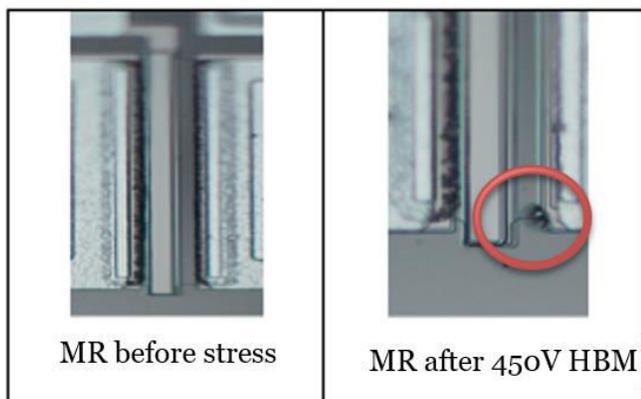


Fig.11. MR photography before and after destructive HBM stress on the drain with gate floating

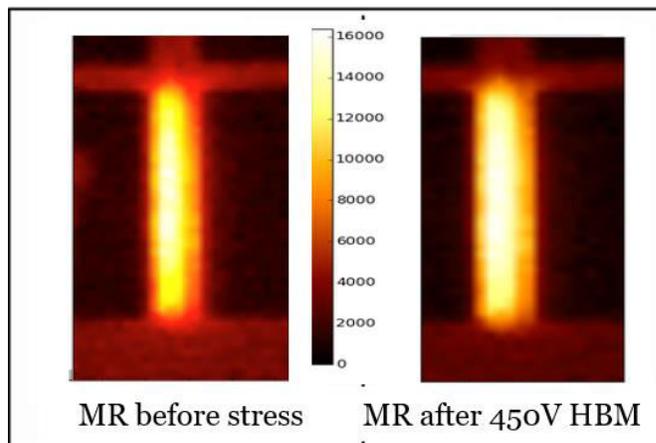


Fig.12. MR lock-in thermography before and after destructive HBM stress on the drain with gate floating

B. Visual observation

1) Stress on drain

As described in previous works [12] [13], MR and MSD failure, in ON state condition, are related to the intermetallic dielectric breakdown, which is the weakest part of SiC technology [5] [14]. By contrast, when the N-channel is blocked, MR presents a different failure mechanism. Concerning MZD, failure looks to have the same origin even if the failure voltage level is different. Due to the Zener diode conduction, a parasitic transistor conducts current until failure. This transistor takes still place at the drain corner, at the body junction, where electric field is the highest. The Zener diode conduction in OFF state condition requires more voltage in comparison with ON state condition: this shift is induced by leakage current through the surficial layers, increasing the body potential as in Fig.16. In this figure, we can observe that electron current looks to find its origin with hole current coming from the gate. This current conduction may delay the parasitic transistor triggering (Fig.17.).

Furthermore, between MR and MZD, failure looks similar as shown in Fig.18. Even if electrical characteristics are different, TLP power failure is equivalent for MR and MZD and equivalent to MZD in ON state. Only current increase slope is different, meaning the internal resistance of the $I_{\text{TLP}}-V_{\text{TLP}}$ characteristic, measured here at around $R_{\text{MZD}}=75\Omega$ and $R_{\text{MR}}=250\Omega$.

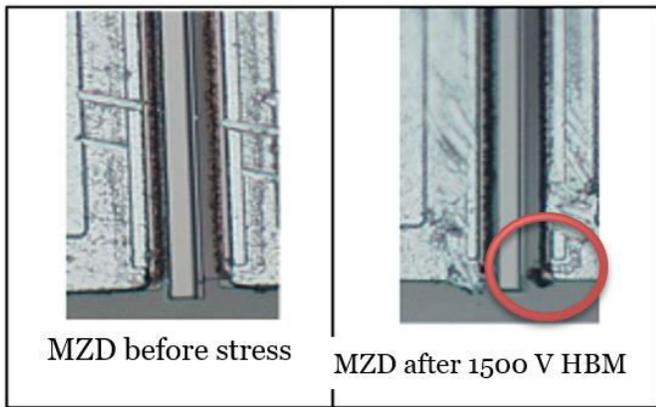


Fig.13. MZD photography before and after destructive HBM stress on the drain with gate floating

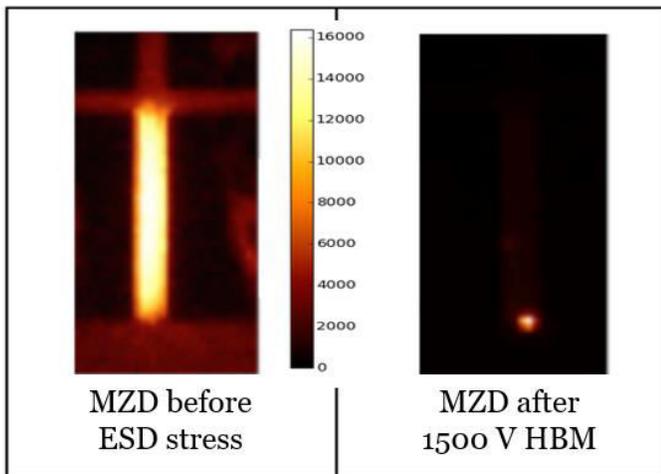


Fig.14. MZD lock-in thermography before and after destructive HBM stress on the drain with gate floating

2) Stress on gate

Corresponding to MESFET's gate stress, results are similar for the three devices with positive stress, and with similar visual consequences (Fig.19.). The unmetallized part of the gate burnt.

In reverse biasing, failures are also reproducible and identical, with in addition the creation of a short between source and gate electrodes (Fig.20.). This short is localized now at the extremity of the gate metal.

In both cases, failures seem to correspond to the oxide breakdown. A short between gate and source is created and at around 200V, voltage is too high for the passivation layer composed of SiO₂. Failure occurs for the same TLP power failure than MSD in Ohmic stress condition.

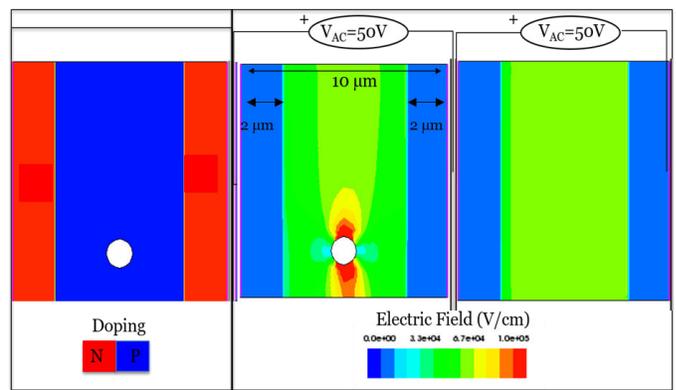


Fig.15. Example of TCAD simulation result with electric field repartition in two SiC lateral NPN, biased at 50V. One is presenting a defect, considered as a hole.

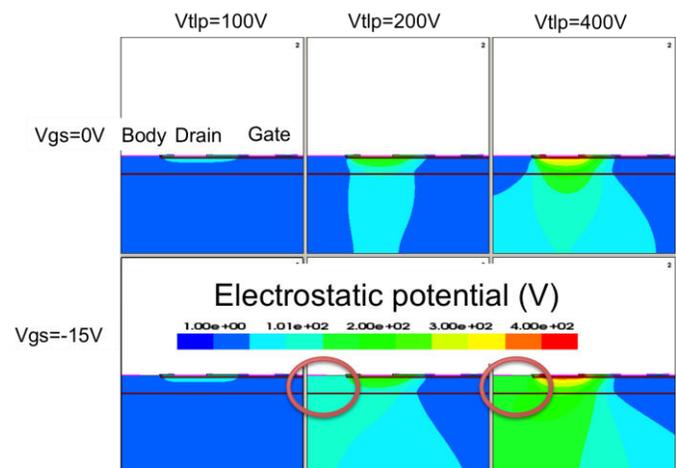


Fig.16. Simulation of the electric field repartition in blocked and unblocked MESFET

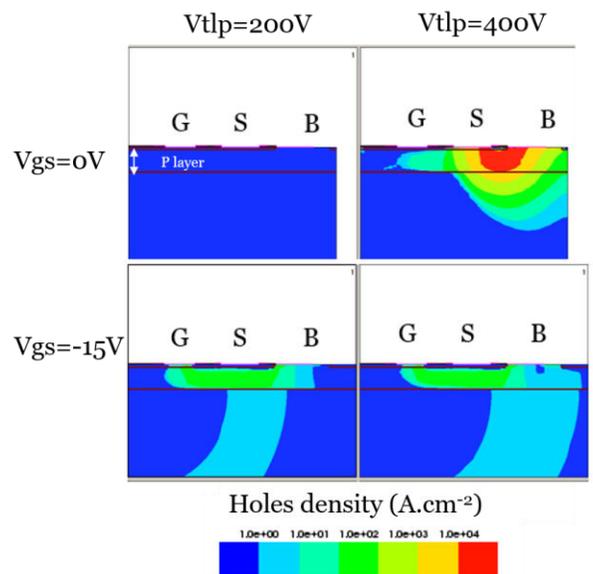


Fig.17. Simulation of holes density in ON and OFF state condition

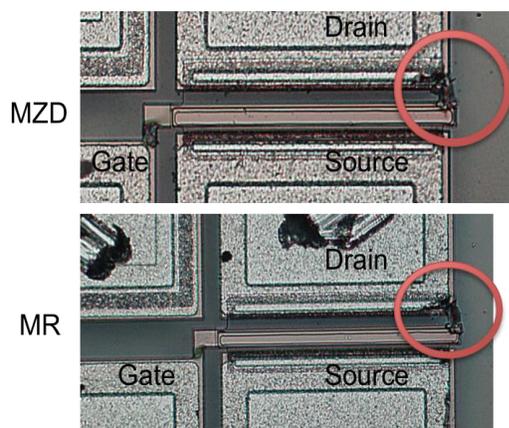


Fig.18. Failures on MR and MZD after TLP drain-source stress in Off state condition ($V_{gs}=-15V$)

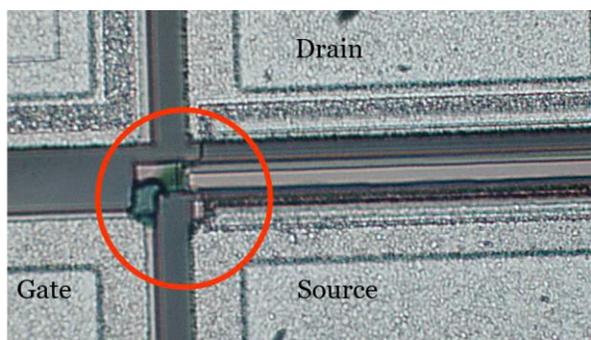


Fig.19. Failure on MZD after a positive TLP stress on the gate with drain electrode floating

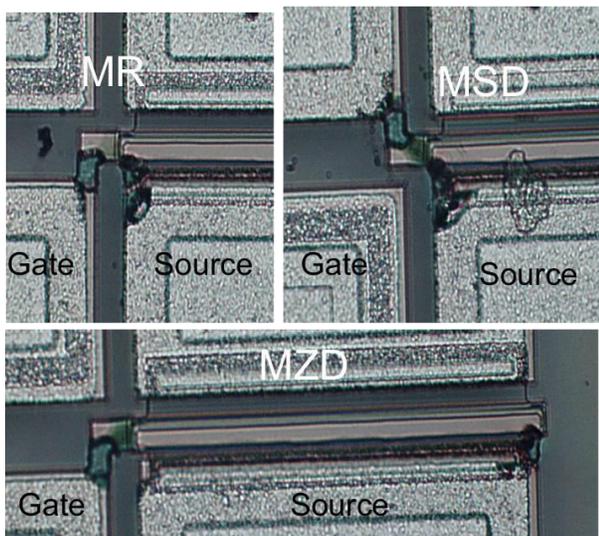


Fig.20. Failures on SiC MESFET provoked by negative TLP stress on the gate with drain electrode floating

V. DISCUSSIONS

We try to understand the physical behavior during failure mechanism and what are the differences between each devices. Failures in ON state condition were already explained with a parasitic transistor triggering and with oxide breakdown [12] [13]. For the OFF state condition, hypothesis of the failure mechanism is here advanced. Finally the impedance

measurement between broken and unbroken device will complete the study.

A. Correlation with diode triggering

As it was demonstrated, during TLP stress, internal diodes affect the device electrical behavior and trig on the failure mechanism. On our MESFETs, the only difference between MSD and MR, and MSD is the kind of diode or its localization.

For instance, MSD requires more voltage to inject carriers in the N channel than the other devices. MSD has indeed no N^+ area below the electrode privileging the drain-body diode conduction during high ESD stress. However failure occurs for high TLP voltage because oxide breakdown happens before current triggering,

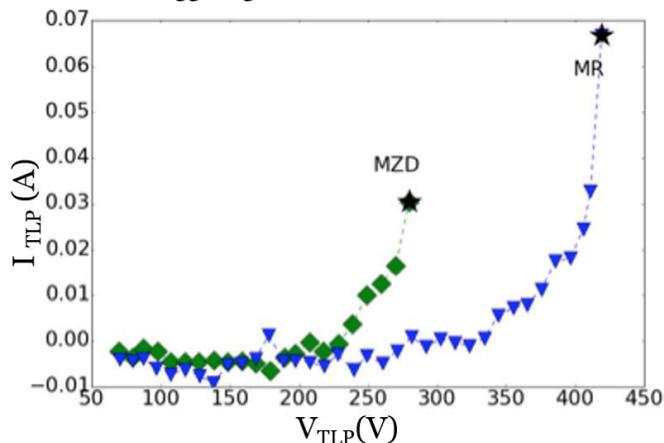


Fig.21. TLP between drain and body in MZD and MR: the diode triggering is different

For MR and MZD, the drain-body diode stressed in reverse mode indicates different TLP voltage value after current increase with different slope. Furthermore these values look higher than those of the entire MESFET failure ones (Fig.21.).

In this study, internal diode impact is, underline with MZD failure mechanism [13]. However, failure couldn't be due only to the Zener diode voltage triggering because the Zener diode is triggered at 30 V in static measurement. In TLP measurement, current increases after 85V for MZD and after 115V for the Zener diode even if failure is coming at around 250V. In blocked condition, the Zener diode TLP measurement indicates a small-triggering-current increase at around 250 V and a failure of the junction diode for 280V is observed. As we can observe (Fig.22.), MZD failure is probably related to the Zener diode triggering but happens later in off-state configuration than in floating one.

The Zener diode triggering is responsible of the transistor triggering, which increases the drain-source current, hence the ESD robustness, until failure. The same phenomenon can also trig on the current increase with the P-N diode conduction and justifies the MR failure for the same power range.

Concerning the different slope, it corresponds to the difference of the internal resistance for each diode. With the parasitic transistor, the power become unsustainable for the device and a hole is created in the device as already demonstrated.

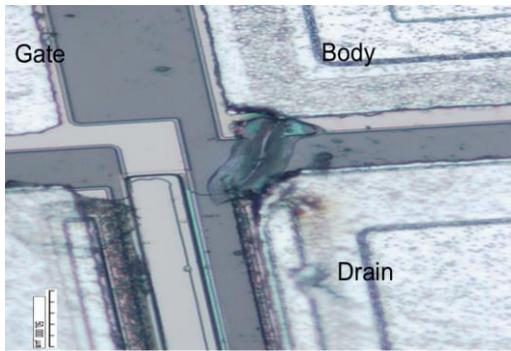


Fig.22. Visualization of the Zener diode failure

B. Consequence of failure on impedance characteristic

As we have seen, internal protections do not modify sufficiently the static and dynamic measurement even if they play a role by increasing the global ESD robustness of the MESFET.

Although passive values can be calculated, an adaptive circuit is required [15]. The purpose in this work is just to determine the internal impedance differences with broken devices for MR and MZD. The goal is to determine which part of the impedance is broken after destructive TLP stress.

Result in Fig.23. shows for broken MR a reduction and noise in the capacitance measurement and a reduced internal resistance, probably corresponding to internal capacity failure and the deterioration of the SiC surface. In the contrary for MZD, the capacity value increases with exactly the same signal form and the resistance measurement presents no modification. A buried hole is therefore created in the SiC.

Because of the parasitic NPN transistor, a local current increase produces a local heating in the SiC [12] resulting in SiC sublimation and the hole creation in the semi-conductor. This hole modifies the capacitance between drain and P⁺ body and creates interferences in the dynamic measurements.

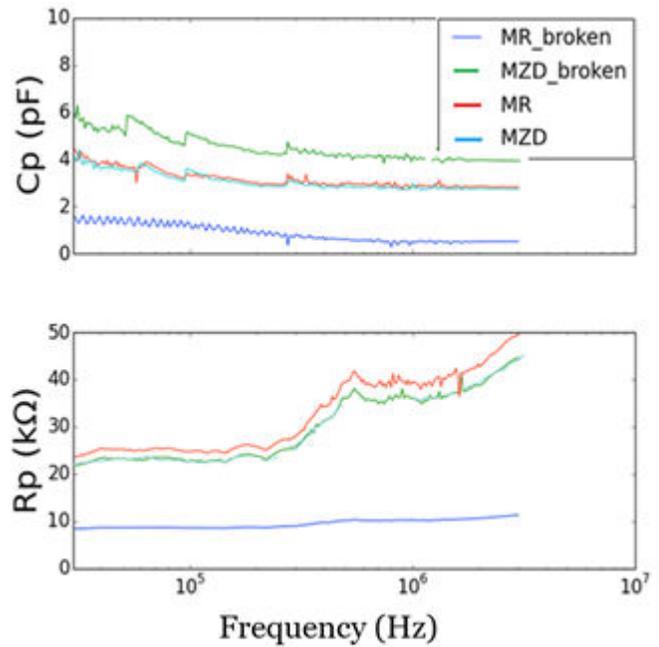


Fig.23. Dynamic measurements for MR and MZD on Drain-Body junction; Internal impedance has a failure

VI. ROBUSTNESS IMPROVEMENTS

In order to increase the ESD robustness of the MESFET, a solution for canceling or delaying the different failures mechanism in regards with the avalanche voltage or with the passivation dielectric is presented.

A. Body's metallization and Zener on drain improvement

The MESFET structure is undoubtable a suitable configuration for the development of a parasitic transistor (Fig.24). The ESD robustness of the design is limited because of this mechanism, triggered firstly by avalanche process as for MR and secondly with by the Zener triggering, hence injecting carriers below the source electrode as for MZD device.

Several possibilities for silicon devices exist for delaying this transistor, like alternative N⁺ and P⁺ area below the drain electrode [16] or like circular trench in the drain contact [17]. It globally permits to reduce the local current density below the electrode responsible of the parasitic transistor. Unfortunately, they were not tested or simulated in this work.

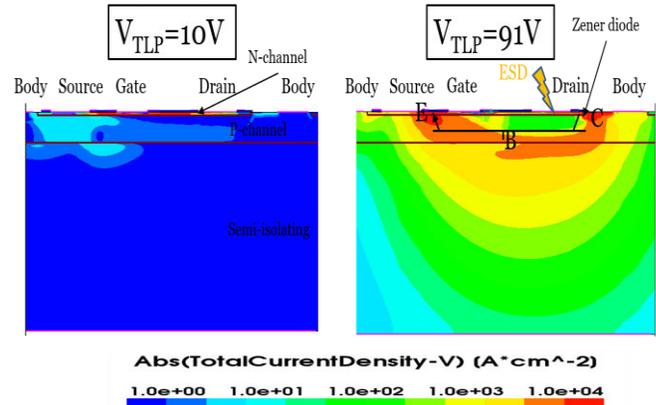


Fig.24. Current density representation on MZD layout before and after the parasitic NPN triggering

Another way to delay the transistor triggering can be to add a metallization on the body layer in order to homogenize the internal resistance and hence spread the current repartition all over the surface of the device [13]. However this solution is not easy to put into practice because of the overlaying of several metals.

Eventually a solution could be to modify the channel thickness as it was demonstrated for a mesa-MESFET with a similar structure composition but it brings a tradeoff with our requirements as the voltage breakdown [12]. In Fig.25., the ESD robustness seems better with a P-channel of 1 μm than with standard 0.5 μm or 0.2 μm

In any case for delaying this premature NPN parasitic transistor triggering due to the avalanche voltage, the Zener diode linked to the body is still efficient, not disturbing the system and does not cost space, to the contrary of changing the passivation oxide.

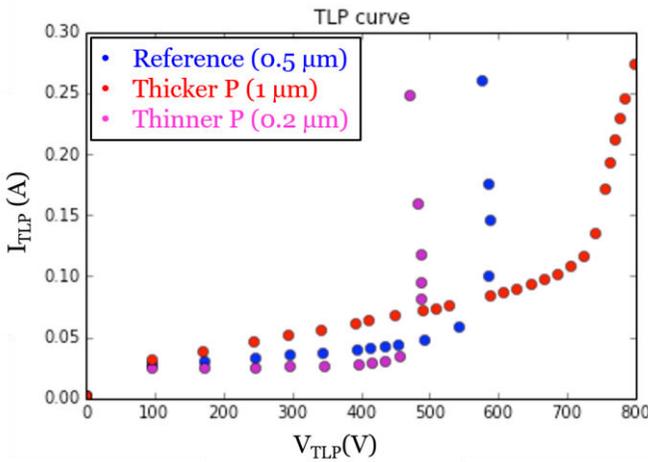


Fig.25. TCAD simulation of TLP test on mesa-MESFET with several P thickness

B. Dielectric of passivation for SiC

Thanks to TCAD Sentaurus package software, it has been possible to simulate breakdown field variation of the device with different dielectric layers (Tab.2). Simulations have been run just by changing the SiO_2 by HfO_2 or by Al_2O_3 which are dielectric, with a high dielectric constant, interesting for SiC [5] [13]. In this simulation, the dielectric thickness was also modified to match with the Atomic Layer Deposition (ALD) of these oxides, corresponding to the deposition method of these dielectric. A maximum thickness of 100nm instead of 500nm was selected. A breakdown criterion on the maximum electric field in the dielectric is added in the simulation.

Results for the aluminum oxide are interesting, with no oxide breakdown until 900V whereas HfO_2 and SiO_2 simulation stop at their maximum electrical field criteria around 400V (Fig.26).

We can also notice that the dielectric constant impact the current level (Fig.27.). Indeed the electric field in the passivation layer seems to saturate the N-channel. That's why high dielectric constant materials of passivation allow a higher current level.

Oxide breakdown is an important parameter to take into account for ESD robustness. Realization with HfO_2 or Al_2O_3 is however limited by the time of deposition, which impact the

deposition thickness limited to 100 nm due to the need of using ALD technique. It's hence not suitable for power devices which need thicker passivation layer. Other high-k materials have to be tested in order to find one suitable for SiC material.

Materials	ϵ_r	Breakdown Field (MV/cm)
SiO_2	10	3
HfO_2	20	5.4
Al_2O_3	9	12

Tab.2. Table of simulated materials properties for SiC MESFET oxide passivation

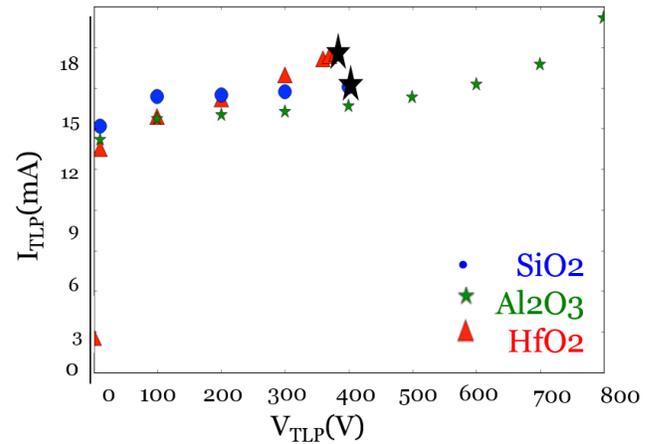


Fig.26. TLP test simulation on several passivation dielectrics MESFET. Al_2O_3 looks to be the most reliable because there is no oxide breakdown symbolize in black

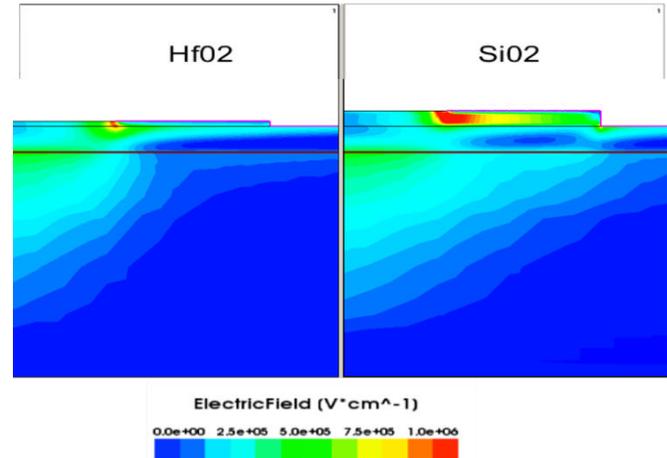


Fig.27. Electric field repartition in HfO_2 or SiO_2

VII. CONCLUSION

TLP stress results on Schottky gate contact and Ohmic contact are investigated in this work. Three different SiC MESFETs are tested against ESD and HBM to test point out for Ohmic contact and the benefits of Zener diode integration to the contrary of Schottky diode. Robustness is improved from 1A to 1C according to JEDEC Classification.

Two failure mechanisms are identified after stress: only the Zener on drain MESFET is not limited by the first mechanism, corresponding to the intermetallic dielectric (SiO_2) failure. Its ESD robustness is increased without modifying the electrical dynamic and static characteristics, with no extra cost and is insured by the triggering of a parasitic transistor. However, current filamentation occurs and ultimately limit the device robustness.

Moreover TLP stress results on Schottky gate contact and Ohmic drain contact present a different ESD robustness even if the failure mechanism looks similar.

In contrast with silicon devices case, electrical measurement cannot clearly indicate the device failure because the created hole in the SiC material only marginally impact the device electrical characteristics. Visual analyses are hence presently used when stopping the test just after a failure is observed. Consequently, SiC requires new methods for failure detection that are different of the one used for silicon devices due to its sublimation property.

Lock-in thermography analysis is used in this work and reveals different emission response depending of the failure created and the MESFET studied.

Furthermore, integration of the Zener on Drain MESFET in electronic circuit has also to be experimented and tested in order to validate the ESD robustness improvements.

Finally, TCAD Sentaurus simulation results show that in replacement of SiO_2 , Al_2O_3 with his high dielectric constant can be a candidate for application requiring high ESD robustness. However a tradeoff has to be found because the realization would be more expensive.

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