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Printed Complementary Organic Thin Film Transistors based decoder for ferroelectric memory

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Abstract— This paper presents a decoder circuit manufactured in a printed complementary organic TFT technology on flexible substrate. Decoder architecture, simulation and experimental results are detailed. In order to comply with current printed electronic capability, a tree based decoding architecture is specifically implemented in order to provide robust functionality with a limited number of transistors. Two different output stages are implemented in order to drive active and passive ferroelectric memory. To drive active matrix, a buffer output stage is proposed, whereas a pass-gate based output stage, with customizable voltage, is used for passive matrix. Characterization results show that the decoder for both output stage options is functional for a wide range of voltage from 40V down to 5V, and for timing between 5ms and 100ms.

Keywords— Decoder, Printed electronic, organic thin film transistor (OTFT), FeRAM, Memory design.

I. INTRODUCTION

In the last ten years, the interest in organic semiconductor technology on flexible substrate has strongly grown, especially for the applications requiring low cost, flexibility, low complexity and capability to cover large area [1][2]. Indeed, organic thin film field-effect transistors (OTFTs) are particularly interesting as their fabrication processes are much less complex than conventional Silicon technology and their mechanical properties are intrinsically compatible with cheap flexible substrate. Consequently such technology could enable the integration of electronic at low-cost in different consumer's goods. In this context, OTFTs has already been demonstrated as enabler for several key applications such as electronic paper (e-paper) [3], smart sensors [4][5] and information storage devices [6][7]. The research in the field of organic memory has mainly focused on the development and optimization of innovative organic memories devices, and especially Ferroelectric random access memory [8]. However with the recent improvement of OTFT performance and emergence of complex OTFT circuits, peripheral circuitry for memory have been also recently reported with organic decoder fabricated with inkjet printing on flexible plastics [10]. The figure 1 illustrates a full FeRAM memory circuit. Surrounding a passive or active bit cell array, peripheral circuits allow controlling all programming and reading operations. The peripheral circuits are given as follow: a word line or row decoder to select the active word, a multiplexer to select the active bit cell, a plate line driver to perform programming operation on selected bit (pulse on FeRAM cell bottom

electrode), a R/W selector to connect active bit line to the sense amplifier for read operation or to the write driver (pulse on FeRAM cell top electrode) for program operation. It is important to note that in passive matrix row decoder is used to apply positive pulse or blocking voltages on FeRAM cell top electrode during programming operation.

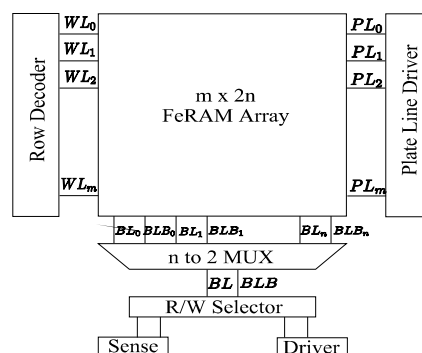


Fig. 1. Full architecture block diagram for ferroelectric memory.

Regarding decoder architecture, the first and largely utilized decoder, is the Logic Gate Decoder. It makes use of logic gates to drive each decoder output, the active output being at a logic value 'X' while all the others are set to 'X̄'. This architecture has a fast stabilization time, a high power, and is composed by of a large number of transistors (54 in a 3 to 8 decoder and 136 in a 4 to 16 decoder). Some modifications may improve certain properties like for example a selective decoder with pre-charge as detailed in [9] to reduce the power consumption and alternative architecture based on tree to reduce the transistors number.

In this context, the aim of this work is to propose a printed C-OTFT row decoder suitable for active or passive ferroelectric memory with a minimal number of C-OTFT. The paper is organized as follows. Section II gives an insight on the adopted C-OTFT technology. Section III describes the architecture of the decoder, and section IV presents characterization results and performances analysis. Finally main conclusions are drawn in section V.

II. COMPLEMENTARY ORGANIC TFT TECHNOLOGY

The technology employed in this papers is a printed complementary Organic TFT technology manufactured on $11 \times 11 \text{ cm}^2$ flexible foil by CEA-Liten [11][12]. A simplified cross-section of TFTs is shown in Figure 2 [13].

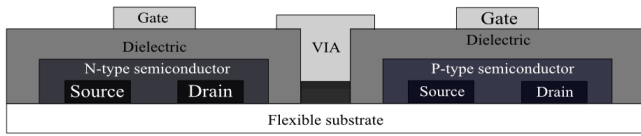


Fig. 2. C-OTFT cross-section of the adopted technology.

Both N and P-type Transistors are implemented with a top-gate bottom-contact multi-finger architecture. Source and drain electrodes are first patterned either by photolithography or by laser ablation on a 125- μm thick Polyethylene-naphthalate (PEN) foil with 20 μm as typical channel length. Then after surface treatment and injection engineering by the mean of a Self-Assembled Monolayer (SAM) [12], the small molecule based organic semiconductors are patterned through screen printing with a final thickness in the range of 50-150nm. Typical carrier mobility of 1.5 $\text{cm}^2/\text{V}\cdot\text{s}$ and 0.55 $\text{cm}^2/\text{V}\cdot\text{s}$ are respectively obtained for p-type and n-type. A common fluoro-polymer dielectric (CYTOP®) is then screen-printed and annealed on top of both semiconductors with a thickness of 750nm, leaving open areas for via holes. Finally a silver-ink conductor is screen-printed on the top of the dielectric and annealed at 100°C, forming in the same step the gate electrodes for devices and the 2nd level for interconnection. The CEA printed technology also enable monolithic integration of multiple device including with N and P transistors, metal-insulator-metal (MIM) capacitors with 24 pF/mm^2 and optional screen-printed carbon-ink resistors [14].

III. ARCHITECTURE DESCRIPTION

A. Decoding stage

The seed of a tree-based decoder is a base-decoder unit, shown in figure 3, which is a 1 to 2 decoder with an enable pin A_i . The base-decoder unit is composed with a pair of transmission gates, one driven by A_i and the other by $\overline{A_i}$. Unselected output is biased to V_{DD} thanks to a pull-up transistor. For 2^n outputs, which corresponds to 'n' address, 'n-1' stages are necessary. The number of base-decoder unit for a stage 'n' is 2^n . Doing so the most significant address bit A_n and $\overline{A_n}$ are routed to the selected output given by the less significant address bits (A_{n-1} to A_0), activating only one output depending on A_n value. The decoder developed in this work, as presented in figure 3, is designed with three addresses and eight outputs; it requires two stages. The final decoding architecture, shown in figure 3, requires 36 transistors plus 6 for the three inputs inverters; making 42 transistors in total, whereas the same capacity decoder proposed in [10] requires 52 transistors.

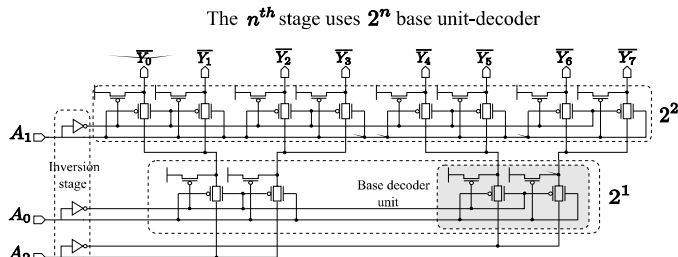


Fig. 3. 3 to 8 decoder schematic.

Moreover, when dealing with larger number of address bits, the tree-based architecture allows even a more significant

reduction of transistors number compared to NAND gate architecture (cf Fig. 4). For example, for a matrix of 32 words by 32 bits, which provides a 1kb capacity, the tree-based architecture requires only 190 transistors, while the NAND gate architecture reaches 330 transistors.

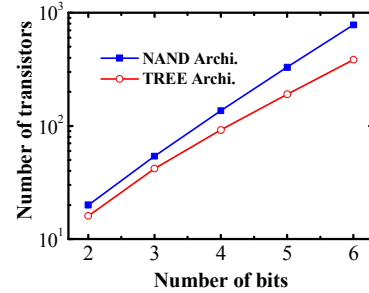


Fig. 4. Number of transistors versus number of address bits for a NAND gate architecture and a tree-based architecture.

B. Driving stage

The proposed architecture cannot directly address a matrix with large dimensions due to its low output current. In order to do so, an output stage must be added. Here, two solutions are proposed: a *buffer* output stage for active matrix and a *pass-gate* output stage for both passive and active matrix.

The buffer stage shown in figure 5.a can be used to drive the word line (WL) of an active matrix, where each word line is connected to a p-type transistor's gate to select the bit-cell. The buffer output allows driving more current to switch the p-type transistor when the output is at "0". Another approach is to connect the word line decoder to a passive matrix. In this case, decoder output stage is directly connected to the top electrode of the FeRAM cell of a given word. This output stage, or pass-gate output stage, is able to connect inputs D_0 or D_1 with different voltage level to Z .

The schematic of this output stage for a single bit is shown in figure 5.b, as proposed in [10]. To drive active matrix with large capacitance load due to P-OTFT gate, buffer transistor requires large dimension ($W=2000\mu\text{m}$), whereas pass-gate address directly the FeRAM cell and requires less current ($W=500\mu\text{m}$).

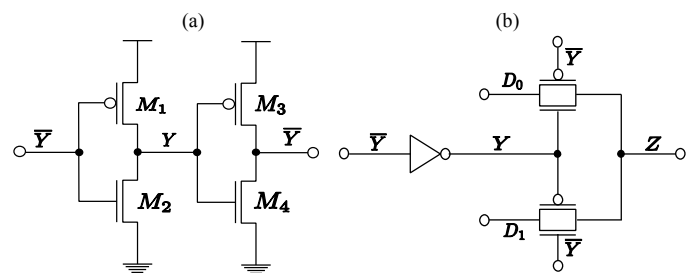


Fig. 5. (a) Double-inversion output schematic for 1 bit ($W/L=2000\mu\text{m}/20\mu\text{m}$) (b) Pass-gate stage schematic for 1 bit ($W/L=500\mu\text{m}/20\mu\text{m}$).

Fig. 6 shows the layout of both decoders, and figure 7 includes a photograph of our printed C-OTFT decoder with buffer output stage on flexible foils. Figure 8 presents the simulations results of both decoders. Simulations are carried out to validate the functionality of the circuits using compact model of the C-OTFT [15][16][17], during design phase.

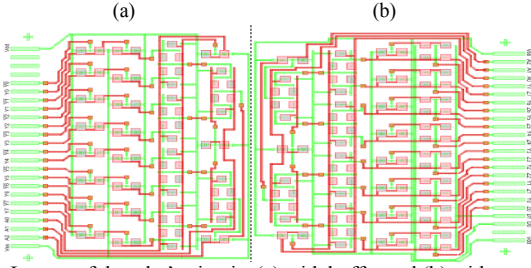


Fig. 6. Layout of decoder's circuits (a) with buffer and (b) with pass gates.

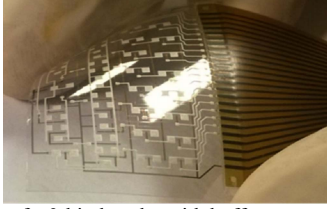


Fig. 7. Photograph of a 3-bit decoder with buffers.

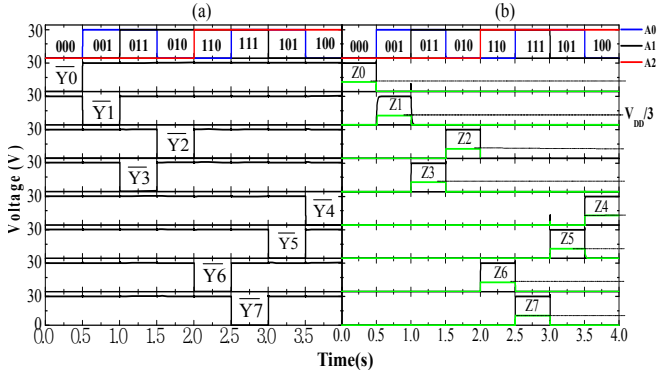


Fig. 8. Simulations results for outputs after (a) the buffer stage (b) pass-gate stage $V_{DD}=30V$ & $T_{word}=500ms$ (with black: $D_0/D_1=V_{DD}/GND$ & green: $D_0/D_1=V_{DD}/3/GND$).

Simulation results show that each output is successively selected following the address bits evolution (Gray code). When an address is activated, the selected output is set to '0' for the decoder with buffer output stage, and respectively Z is set to a given positive voltage (V_{DD} or a third of V_{DD}) for the decoder with pass-gate, depending on voltages on D_0 and D_1 .

IV. EXPERIMENTAL RESULTS AND PERFORMANCES

A. Validation of circuit functionality

All electrical measurements have been performed in air at room temperature. Custom external circuitry and software provides decoder address inputs A_0 , A_1 and A_2 and measure the output wave-forms after the *buffer* stage ($\bar{Y}_0, \bar{Y}_1, \dots, \bar{Y}_7$) and after the *pass-gate* stage ($Z_0, Z_1 \dots Z_7$). The corresponding measurements, are respectively reported in figure 9.a and 9.b, in the case of 30V as supply voltage for both decoders with double inversion and pass-gate and duration of 500ms and 100ms for the address. We can observe here that experimental waveforms of both decoders are in agreement with expected functionality and simulations results presented on figure 8. Moreover the green waveform reported on figure 9.b with input signals set up as $D_0/D_1=(V_{DD}/3)/GND$ shows that the pass-gate output can successfully provide customizable voltage level to Z depending on D_0 and D_1 values.

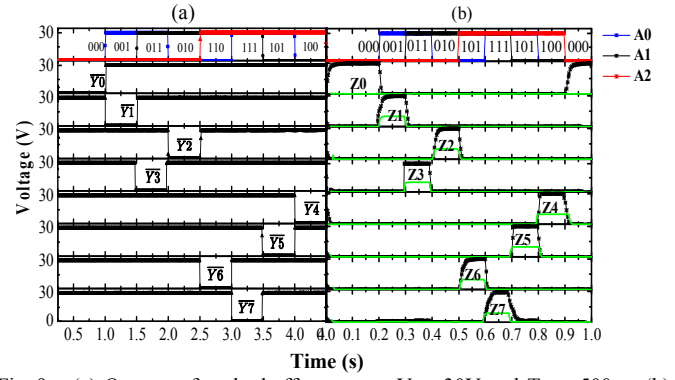


Fig. 9. (a) Outputs after the buffer stage at $V_{DD}=30V$ and $T_{word}=500ms$ (b) Outputs after the pass-gate stage at $V_{DD}=30V$ and $T_{word}=100ms$ (black: $D_0/D_1=V_{DD}/GND$, green: $D_0/D_1=V_{DD}/3/GND$).

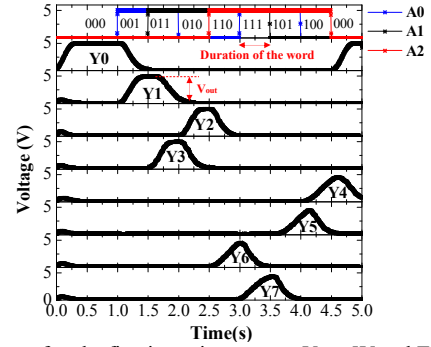


Fig. 10. Outputs after the first inversion stage at $V_{DD}=5V$ and $T_{word}=500ms$.

We have also checked through the measurements reported on Figure 10, that the tree decoding architecture with the buffer option can still operate successfully even with supply voltage as low as 5V. However we observe that output signal slope is strongly degraded and that a minimum duration of 500ms is then required for functional addressing.

B. Dynamic characterization and performances analysis

In order to determine the range of functionality for both decoders in terms of voltage and timing, multiple measurements have been carried out with different supply voltages V_{DD} ranging from 5V to 40V and address code duration from 5ms to 95ms. The propagation delay is measured during the activation and the deactivation of the selected output following an address code change, as illustrated in figure 11. Measured activation and deactivation delay are reported as function of supply voltage on figure 12.a and figure 13.a respectively for decoders with buffer and pass-gates output stage.

We can observe on figure 12.a and figure 13.a, that deactivation transition is always faster than activation transition. This result is linked to the tree-based architecture. Indeed activation signal is provided by A_2 through the entire tree architecture, whereas deactivation signal is provided on the decoder output with pull-up transistor. The tree-based decoder has been simulated to validate this hypothesis. The results obtained, reported on figure 14, shows clearly the same delay trend on the decoder simulation when compared to the measurements on the full structure. The V_{out}/V_{DD} ratio, with V_{out} being the amplitude of the output voltage, is also crucial

and determines the signal degradation through the structure. Measured degradation ratios are presented in figure 12.b and figure 13.b for decoders with buffer and pass-gates output stage respectively.

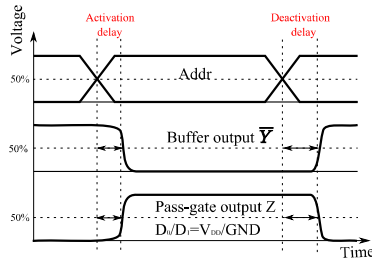


Fig. 11. Measurement of activation and deactivation delays.

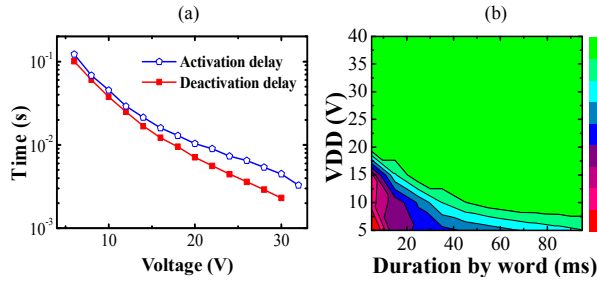


Fig. 12. (a) Activation and deactivation delays (b) V_{out}/V_{DD} ratio for the decoder with *buffer*.

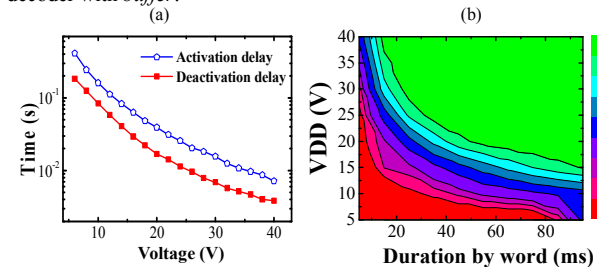


Fig. 13. (a) Activation and deactivation delays (b) V_{out}/V_{DD} ratio for the decoder with *pass-gates* (with $D_0/D_1=V_{DD}/GND$).

From these experimental results, we can see that both decoders are functional with acceptable degradation ratio over a wide range of voltage from 5V to 40V depending of the code address duration required. In addition, one can notice that activation and deactivation delays are inversely proportional to the supply voltage, thus defining the functional window in term of supply voltage and speed available for a given application.

V. CONCLUSIONS

A tree-based word-line decoding scheme, for ferroelectric passive or active memory is proposed. To address both type of memory, two different output stages are proposed, based on buffer or pass-gate insertion. Both circuits have been successfully manufactured using printed C-OTFT technology on flexible foils. Measured V_{out}/V_{DD} ratio and activation/deactivation delays on the decoder outputs show functionality for a supply range of 5V to 40V and address code duration from 5ms to 95ms. Proper operating point at high speed is linked to high supply voltage. Finally, the tree-based decoder allows a design with a reduced number of transistors compared with NAND gate architecture for a limited impact on activation delay.

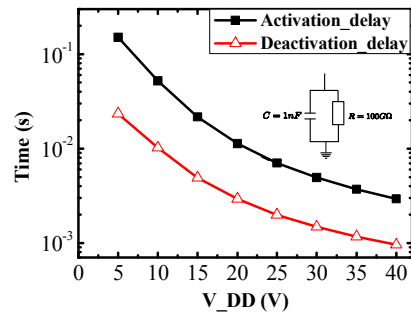


Fig. 14. Simulation results of activation and deactivation delays of the tree architecture without driving stage (with load of $C=1nF$ & $R=100G\Omega$).

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