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Temperature impact (up to 200 °C) on performance and reliability of HfO₂-based RRAMs

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Abstract— This paper provides an overview of the temperature impact (up to 200 °C) on the electrical behavior of oxide-based RRAM, during forming, low-field resistance reading, SET/RESET, disturb, data retention and endurance. HfO₂-RRAM devices (in a 1T1R configuration) integrated in an advanced 65 nm technology are studied for this aim. We show that forming operation is strongly activated in temperature (*i.e.* -0.5 V per hundred Celsius degree), being much less for SET and RESET voltages (*i.e.* < -0.05 V per hundred Celsius degree); disturb of HRS at fixed voltage showed to be independent of temperature; endurance up to 3.10⁶ cycles, with optimized set of stress parameters showed no significant variation; data retention at 150 °C up to 68 days showed stable programming window, after different initial programming algorithms.

Index Terms— Resistive-switching random access memory (RRAM), bipolar operation, endurance, data retention, disturb.

INTRODUCTION

Resistive-Switching Random Access Memories (RRAM), are considered as one of the most promising candidates for replacing or complementing current non-volatile memories, based on FLASH, in next memory generations. Both non-polar (*i.e.* switching triggered by voltage amplitude, regardless of voltage polarity) and bipolar (*i.e.* switching triggered by the voltage polarity) have been shown on several active materials [1]. In the scientific literature many papers deals with the impact of temperature on the RRAM operation [2]-[5], however no one of them provides a synoptic view of the temperature impact on all basic memory operations like forming, SET/RESET, low-field resistance reading, disturb, endurance and data retention with state-of-the-art RRAM in 1T1R configuration. Without the pretention of being exhaustive on each of these aspects, this paper draws light on the weak dependence of RRAM operation on temperature (except for forming) on a wide temperature range, up to 200 °C, well above the automotive application specifications of 140 °C.

For this aim, we use quasi-static measurements for the investigation of forming/RESET/SET voltages/currents (see

Fig. 1.), in order to acquire also a better insight in the physics of resistive switching, and pulsed-mode regime for the analysis of performances and reliability (data retention and endurance). The devices under test are HfO_x-RRAM, embedded in 1T1R configuration on 65 nm CMOS technology platform (Fig. 1.). The RRAM active layer consists of 5 nm thick HfO₂, deposited by ALD, sandwiched between bottom TiN(35 nm) and top electrodes Ti(10 nm)/TiN(50 nm) deposited by PVD. The RRAM area is 1x1 μm².

Unless otherwise mentioned all data presented in the next sections come from evaluation on 10 to 20 devices. Even if not from a large statistical ensemble of cells, this data are used to have a view on the average and standard deviation.

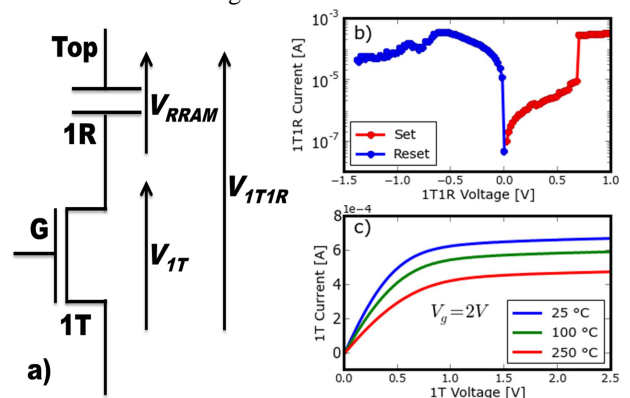


Fig. 1. a) Schematic of 1T1R HfO₂-RRAM; except otherwise mentioned, all voltages represented in the remaining figures of the paper refer to V_{RRAM} b) I(V) characteristics for SET and RESET operations c) Transistor characteristics measured at 25 °C, 100 °C and 250 °C (such characteristics are essential to extract V_{RRAM} at the different temperatures).

I. QUASI-STATIC MEASUREMENTS

First quasi-static measurements were made to assess the impact of temperature on full I(V) characteristics. The forming operation, as shown in Fig. 2. and as already shown in Refs. [4],[6], is strongly activated in temperature: -0.5 V per

hundred Celsius degree can be appreciated for our devices, so that the forming voltage is almost halved passing from room temperature (RT) to 200 °C. If we perform the forming on the devices at ambient temperature and we operate the low-field resistance reading, on the same aforementioned temperature span, as shown in Fig. 3. , we note that: the LRS conduction appears metallic being the resistance raise with temperature mainly due to the transistor itself and not to the RRAM [2][3],[7],[8]; the HRS resistance, on the contrary, is almost constant or slightly decreasing, within the considered temperature range, which is consistent with the charge transport mechanism, *i.e.* the trap-assisted tunneling among the traps located within the broken filament. In essence *both LRS and HRS resistance evolution due to temperature is below a factor of 1.3 from RT up to 200 °C.*

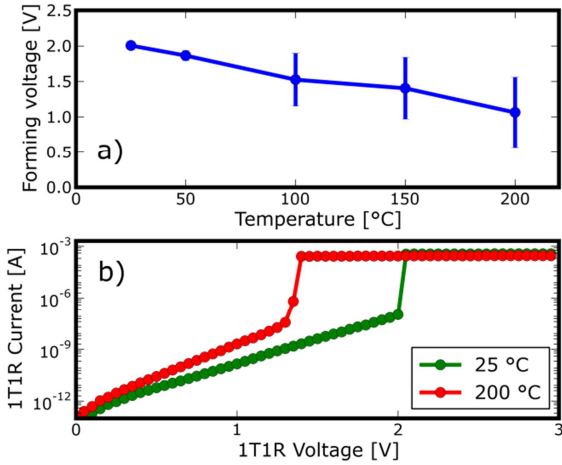


Fig. 2. a) Forming voltage dependence with respect to the temperature. b) $I(V)$ characteristics during forming (positive voltage on top electrode) at $T=25$ °C and $T=200$ °C.

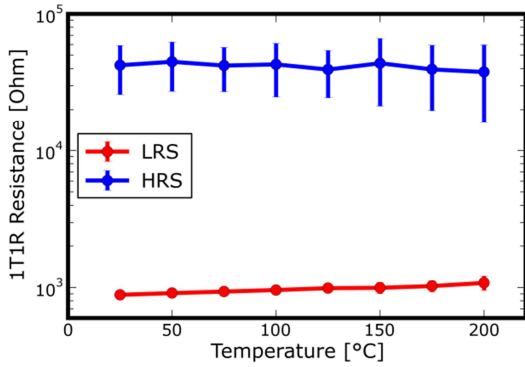


Fig. 3. Low-field resistance reading of both HRS and LRS with respect to temperature (note that forming is performed once at ambient temperature).

If RRAM switching capabilities are evaluated in temperature, we see in Fig. 4. that *both SET/RESET voltages exhibit less than 50 mV variation in the analyzed temperature range.* The corresponding LRS and HRS resistance states (this time written/erased at high temperature) do not feature any significant variation as well (*i.e.* less than a factor of 1.6).

From the set of measurement of Fig. 4. we extract also that at high temperature, the RESET current, I_R , remains similar to compliance current, I_C [9] (not shown here). The only deviation with respect to this classical behavior appears whether we operate a forming/SET at RT, being the RESET operation realized at high temperature. Indeed, as shown in Fig. 5. , the RESET $I(V)$ are monitored up to 250 °C, being the SET operation realized at ambient temperature. This electrical behavior has been interpreted with a simulation frame presented in Ref.[10], which comprises a statistical Kinetic Monte Carlo diffusion model coupled with the model describing the electron charge-transport through Trap-Assisted Tunneling (TAT), the power generation/dissipation and field- and temperature- induced oxygen vacancies and ions generation/recombination [6]. In this frame, we evaluated self-consistently the forming and RESET made at different temperature and simulations are presented in Fig. 6. The I_R/I_C trend is qualitatively explained as follows: the RESET current reduction is justified by an enhanced diffusivity of oxygen ions and so enhanced ion/vacancy recombination rate at higher temperature, thus reconstructing the dielectric barrier more easily than at lower temperature. This conductive filament partial disruption depends directly on the recombination/oxidation process, and increasing the temperature leads to smaller RESET currents and voltages, as represented in Fig. 6.

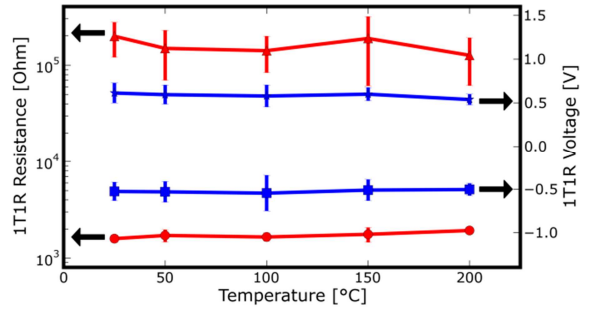


Fig. 4. SET/RESET voltage and associated resistance states evolution as a function of temperature. Note that, according to data of Fig. 3, here the LRS/HRS are written/erased and read at the corresponding temperature.

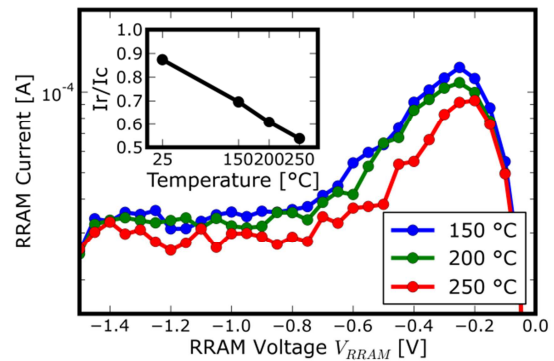


Fig. 5. Average RESET characteristics for 150 °C, 200 °C and 250 °C, when forming is performed at RT. Inset: RESET to compliance current ratio I_R/I_C as a function of the temperature: a strong deviation from the well-known empirical rule of $I_R \approx I_C$ is evident.

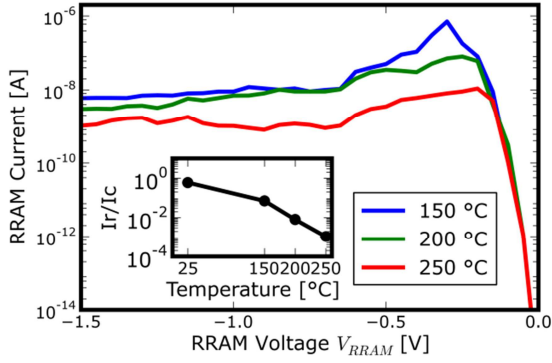


Fig. 6. (a) Simulated reset curves at 150 °C, 200 °C and 250 °C after forming at room temperature. Note that due to the TAT assumption for electron transport, the simulations are limited to 10 μ A, while data of Fig. 5 are with currents of 100 μ A. Inset: simulated RESET to compliance current ratio I_r/I_c as a function of the temperature: qualitatively, the trend of Fig. 5. Inset is reproduced.

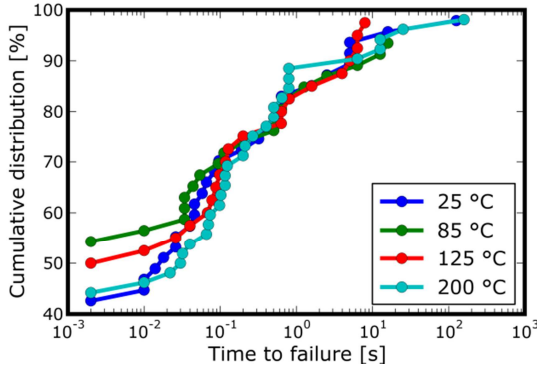


Fig. 7. Failure distributions with respect to temperature for an applied voltage of 0.6 V. Note that failures below $t=2 \cdot 10^{-3}$ s are below the sensitivity limit of our instrument.

In order to assess the disturb robustness of such devices, we programmed the HRS state at room temperature and then we subjected the devices to a constant voltage stress ($V=0.6$ V) at temperature between 25 °C and 200 °C. Currents are monitored to detect failure (*i.e.* switch of device from HRS to LRS). The cumulative distribution function of time to failure is represented in Fig. 7. *No dependence on temperature is observed [11].*

II. PULSED-MODE REGIME

Finally we assessed the impact of temperature on RRAM device endurance and data retention working with RESET and SET in pulsed regime: unless otherwise mentioned the SET/RESET pulse width is 10 μ s, and voltages suited for a compliance level of 100 μ A.

To assess the impact of temperature on endurance performances, 3 million cycles (with resistance read after each SET/RESET operation) have been made on different cells at different temperatures. Note that the same optimized pulse features are used among all temperatures and all endurance tests are operated in blind-mode (without any intelligent algorithm to pursue a specific resistance value). The result is shown in Fig. 8. *The endurance performance is fine regardless*

of the ambient temperature used for the test, with a programming window of roughly one decade kept up to the end.

To push further the endurance analysis in Fig. 9., we monitored the LRS and HRS cumulative distribution functions of a test up to 10^8 cycles, performed at ambient temperature. We note that 30x more cycles do not change the programming window (the test has been interrupted due to excessive test time), moreover the blind-mode distributions of neither LRS nor HRS notably changed during cycle number. Queues of LRS and HRS distributions overlap in less than 0.001% number of cycles. To handle this negligible number of “failing” states, an intelligent algorithm for resistance correction has been demonstrated (up to 10^4 cycles “intelligent” endurance) to fully recover them (not shown here).

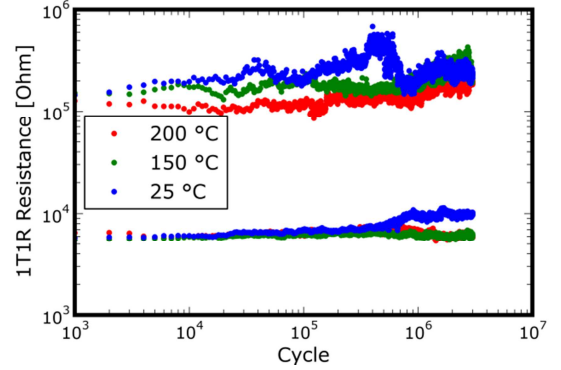


Fig. 8. 3 million cycle endurance test at 25 °C, 125 °C and 200 °C with identical voltage/timings for SET and RESET among different temperatures (one device per temperature). Note that for the sake of clarity not all resistance steps are represented but only one out of 10^3 values.

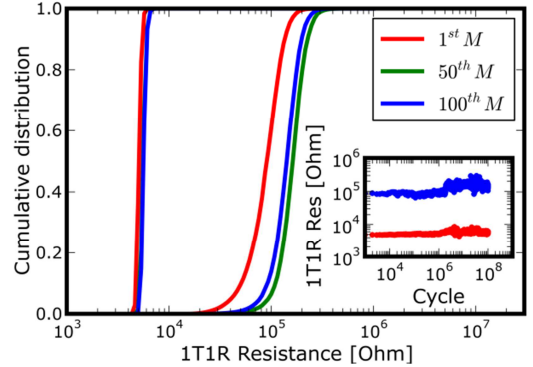


Fig. 9. Cumulative Distribution Function for both HRS and LRS state for 10^8 RESET/SET cycles (room temperature, one device), focusing on the first, 50th and 100th million of cycles. Inset: Resistance as a function of cycle number

The data retention performances have been assessed at 150 °C up to 68 days, after an initial seasoning of 10 RESET/SET pulses. In particular the standard optimized set of forming/RESET/SET pulses of 10 μ s has been compared to two other options: one condition where only the forming is operated at 10 ms, and a second condition where forming/RESET/SET are all operated at 10 ms.

In Fig. 10, we appreciate a global excellent data retention regardless of the energy used for forming/RESET/SET. Operating only a longer forming operation (“Cond. B” in Fig. 10.), is not sufficient to better stabilize the filament against the high temperature stress, if compared to the standard operation (“Cond. A” in Fig. 10.); operating forming/RESET/SET at 10 ms offers a slightly larger programming window, with probably a small improvement of data retention in time, too. As reported in the Fig. 11. , the RESET and SET resistance dispersion is only slightly aggravated during and at the end of this 150 °C test.

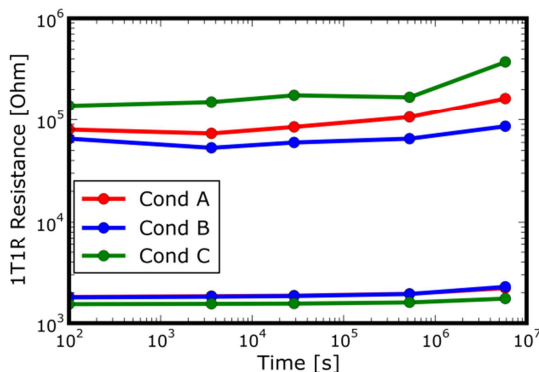


Fig. 10. 68 days data retention at 150 °C for three different RESET/SET options. “Cond. A”: standard optimized set of forming/RESET/SET pulses with 10 μ s pulse width; “Cond. B”: Same than “Cond. A” except of long forming (10 ms); Cond C: Same than “Cond. A” except of long forming/RESET/SET operations (10 ms).

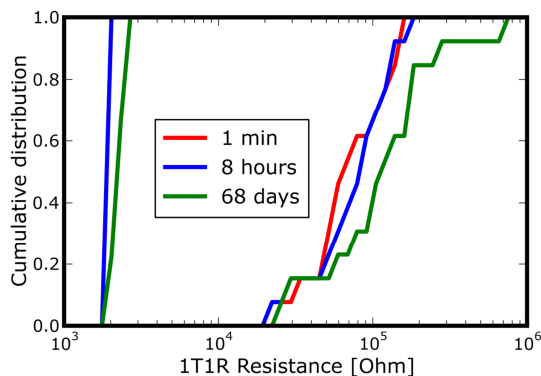


Fig. 11. Cumulative Distribution Function for both HRS and LRS states during the data retention test shown in Fig. 10 for “Cond. A”.

CONCLUSION

We have presented in this paper the impact of temperature (up to 200 °C, the first time with such high temperature boundary) on the main operations of 1T1R 5nm HfO_x-based RRAM integrated in an advanced 65 nm technology. The main conclusions are that:

- The SET/RESET voltages are lightly activated in temperature (*i.e.* < -0.05 V per hundred Celsius

degree), while this is not the case for the forming voltage (*i.e.* -0.5 V per hundred Celsius degree).

- With optimized RESET operation, the disturb at fixed voltage shows no dependence on temperature;
- Endurance (up to 3.10⁶ cycles), with optimized set of stress parameters, shows no significant variations with respect to ambient temperature;
- Data retention at 150 °C measured up to 68 days suggests a highly stable programming window and associated LRS/HRS distributions.

Finally, we believe that this technology is highly promising for embedded NVM applications, in particular taking into considerations the high temperature automotive specifications.

REFERENCES

- [1] H.S. Philip. Wong et al., “Metal – Oxide RRAM,” Proceedings of the IEEE , vol.100, no.6, pp.1951-1970, June 2012.
- [2] C. Walczyk et al., “Impact of Temperature on the Resistive Switching Behavior of Embedded HfO₂ -Based RRAM Devices,” Electron Devices, IEEE Transactions on , vol.58, no.9, pp.3124-3131, Sept. 2011
- [3] Z. Fang et al., “Temperature Instability of Resistive Switching on HfO_x -Based RRAM Devices Electron Device Letters, IEEE , vol.31, no.5, pp.476-478, May 2010
- [4] B. Butcher et al., “Hot forming to improve memory window and uniformity of low-power HfO_x -based RRAMs,” Memory Workshop (IMW), 2012 4th IEEE International , pp.1-4, 2012
- [5] B. Butcher et al., “High Endurance Performance of 1T1R HfO_x based RRAM at Low (< 20 μ A) Operative,” Integrated Reliability Workshop Final Report (IRW), 2011 IEEE International , vol., no., pp.146-150, 16-20 Oct. 2011
- [6] L. Vandelli et al., “Comprehensive physical modeling of forming and switching operations in HfO₂ RRAM devices,” *Electron Devices Meeting (IEDM), 2011 IEEE International* , vol., no., pp.17.5.1-17.5.4, 5-7 Dec. 2011
- [7] D. Ielmini et al., “Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories.,” *Nanotechnology*, vol. 22, no. 25, Jun. 2011.
- [8] B. Traore et al. “Investigation of the role of electrodes on the retention performances of HfO_x based RRAM cells by experiments, atomistic simulation and device physical modeling,” *2013 IEEE IRPS*.
- [9] D. Ielmini et al., “Universal Reset Characteristics of Unipolar and Bipolar Metal-Oxide RRAM,” *Electron Devices, IEEE Transactions on* , vol.58, no.10, pp.3246-3253, Oct. 2011
- [10] L. Larcher et al., “Microscopic understanding and modeling of HfO₂ RRAM device physics”, *IEEE IEDM Tech. Deg. p 474, 2012*
- [11] T. Diokh et al. “Investigation of the Impact of the Oxide Thickness and RESET condition son Disturb in HfO₂-RRAM integrated in a 65nm CMOS Technology” *2013 IEEE IRPS*