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# Phase-Change Memory: A Continuous Multilevel Compact Model of Subthreshold Conduction and Threshold Switching

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**A Phase-Change Memory (PCM) compact modeling of the threshold switching based on a thermal runaway in Poole-Frenkel conduction is proposed. Although this approach is often used in physical models, this is the first time it is implemented in a compact model. The model accuracy is validated through a good correlation between simulations and experimental data collected on a PCM cell embedded in a 90nm technology. A wide range of intermediate states is measured and accurately modeled with a single set of parameters, allowing multilevel programming. A good convergence is exhibited even in snapback simulation thanks to this fully continuous approach. Moreover, threshold properties extractions indicate a thermally enhanced switching, which validates the ground hypothesis of the model. Finally, it is shown that this model is compliant with a new drift-resilient cell-state metric. Once enriched with a phase transition module, this compact model is ready to be implemented in circuit simulators.**

## 1. Introduction

The rapidly growing market of the internet-of-things requires the use of embedded non-volatile memory (e-NVM) presenting ultra-small area, ultra-fast access time and ultra-low consumption. The mainstream solution, the NOR flash technology, needs high potentials hardly compatible with high-k metal gate of advanced CMOS processes (like FinFET or FD-SOI) and thus requires costly advanced process modifications. Other back-end resistive memories are then investigated, and among them, phase-change memory (PCM) is one of the most mature technologies and has reached a pre-production level.<sup>1,2)</sup>

The memory principle relies on the phase transition of an active element between two phases (amorphous or crystalline) presenting resistance levels separated by two or three orders of magnitude.<sup>3)</sup> The state of the cell is determined by reading the resistance in low field area. The PCM has unique multilevel capabilities, because the resistance can vary continuously between the full RESET and the full SET state.<sup>4)</sup> For some states including the RESET state, the I-V characteristics of the cell exhibits a threshold switching, above which the amorphous phase becomes suddenly conductive. The nature of this threshold switching has been a long-term discussion and relies classically on two main hypotheses. First of all, the mechanism has been reported to be mainly electronic,<sup>5-9)</sup> but recent studies brought evidences in favor of a thermal activation in some nanoscale cell.<sup>10,11)</sup> Although it has nothing to do with phase transition, this behavior is central in the PCM's functioning and crucial for circuit designers to determine sense margin. Indeed, the read operation has to be done under the threshold, otherwise phase transition could happen. However, fast reading means setting the reading voltage as high as possible in order to maximize the current difference between two states and to speed up the read process. Moreover, the lower the SET programming current, and the lower the SET resistance achieved, so the better the programming window,<sup>12)</sup> which is interesting in terms of multilevel programming. To fully exploit this unique feature, designers need a trustworthy model to verify by simulation the validity of their design. Mainly, designers want to validate that no switching occurs when supplying the array during the read phase and that peripherals are well designed and provide proper biasing during programming phase with the continuous simulation of the state of the cell including the threshold switching process.

In this context, a compact model requires to be fast, robust and accurate. The threshold switching is a difficult part of the PCM modeling due to its intrinsic non-linearity and abrupt

transition regarding transient simulation. Thus, it may generate convergence problems in the electrical simulators used in the CAD tools. Lots of compact models of PCM have appeared through the years using various modeling strategies. SPICE macro-models have been developed,<sup>13–15)</sup> other more physical models based on a crystalline fraction have been implemented in verilog-A,<sup>16–18)</sup> but most of them dedicate themselves to the phase transition and attach too few importance to the DC behavior. Among those, some use a negative resistance area,<sup>19)</sup> some use a Fermi-like smoothing function,<sup>20,21)</sup> others use switches.<sup>22)</sup> In this work, it has been modeled for the first time using exclusively self-heating mechanism of the cell. This original approach has been validated through I-V measurements for a large set of intermediate states. The simplicity and the continuity for all regimes (below and above the threshold voltage) of the approach is highly interesting in terms of simulation time and convergence ease required in compact modeling.

This paper expands the abstract presented on the 2017 International Conference on Solid State Devices and Materials,<sup>23)</sup> justifying deeper the validity of the proposed compact model, and exhibiting new simulation results. First, the measurement setup, followed by the modeling method are presented. The correlation between experimental and modeling results is then detailed, and the good convergence is validated with additional simulations. Finally, comments on the coherency of such modeling approach is discussed and the compliance with a new cell-metric is shown.

## 2. Experimental Setup and Modeling Method

### 2.1 Experimentation

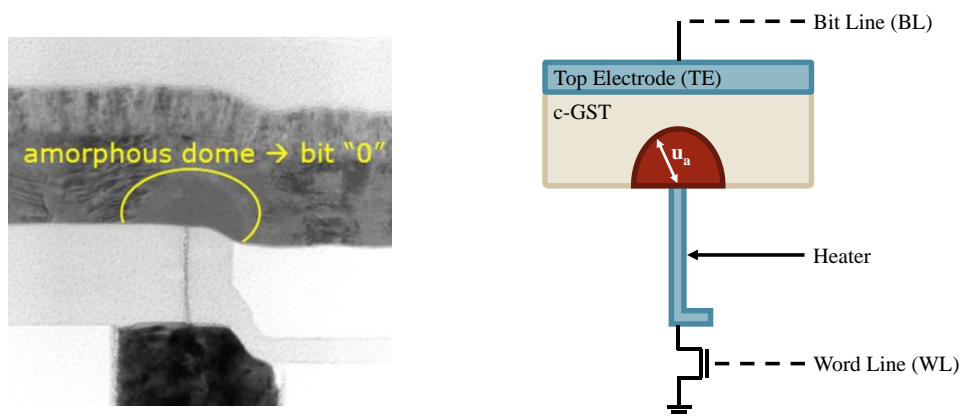


Fig. 1. TEM cross-section (a) and 2D equivalent schematic (b) of the test structure.

Measurements have been performed on a test structure manufactured on a 90nm CMOS node

with embedded PCM option. This test structure is composed of a PCM stack serially connected to a MOS transistor, the latter being used to limit the current flowing through the cell. A TEM cross-section along with a 3-D equivalent schematic of the memory cell is shown on Fig. 1. The 50nm-thick phase-change material (GST225) layer has been inserted between Top Electrode (TE) and a heater with a wall structure shape.<sup>3)</sup> The size of the amorphous dome that can be seen on Fig. 1 reflects the state of the cell, so the goal of the measurements is to let this thickness  $u_a$  vary in order to highlight threshold switching for all the states where it happens.

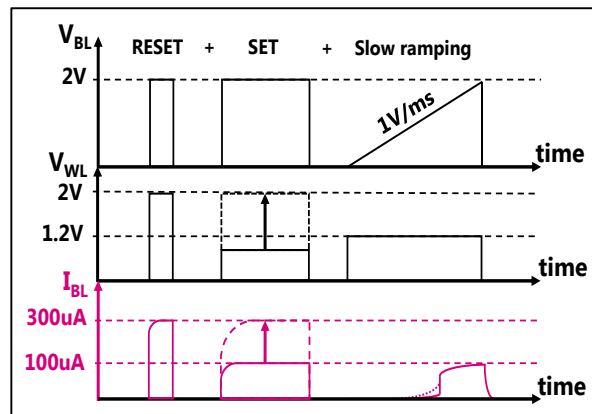


Fig. 2. Chronogram of the measurement protocol. This set of measurement has been repeated 100 times in order to achieve such wide range of intermediate states.

Fig. 2 represents the chronogram of the measurement protocol for each programmed state. A reset pulse of 2V is applied during 200ns before any programming pulse. The word line (WL) bias is then tuned in order to modulate the bit line (BL) current during an 800ns pulse of 2V on the top electrode, resulting in a wide range of intermediate states (see Fig. 3).

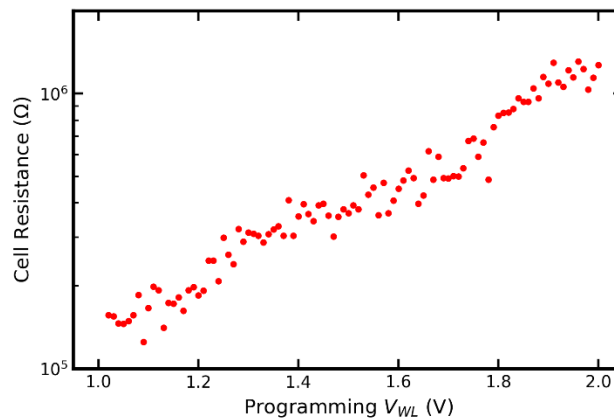


Fig. 3. Cell resistance as a function of the programming gate voltage, displaying the continuously distributed states achieved

Tuning the WL voltage from 1V to 2V, a resistance continuum between 125kΩ and 1.3MΩ can be achieved. The current-voltage characteristics is then obtained by reading the Bit Line current while applying a 1V/ms ramp (0 to 2V) on the top electrode. During this read phase, the WL voltage is set to 1.2V to limit the current and thus the PCM stress. In order to avoid any drift effect,<sup>24)</sup> and to ensure similar measurement conditions whatever the resistance level, a fixed delay has been introduced between every SET pulse and read ramping.

## 2.2 Compact Model

It is widely known that the amorphous part of the subthreshold transport is a hopping conduction of Poole-Frenkel type.<sup>25–28)</sup> In this work however, for compact model purpose, a limited density of traps is assumed and only a simplified form<sup>29)</sup> is considered, given by,

$$I_{PF} = A * F * \exp\left(-\frac{\Phi - \beta\sqrt{F}}{kT}\right) \quad \text{with} \quad F = \frac{V}{u_a} \quad \text{and} \quad \Phi = E_{a_0} - \frac{aT^2}{b+T} \quad (1)$$

where  $k$  is the Boltzmann constant,  $\beta$  a constant of the material linked to its permittivity and  $A$  is a fitting parameter.  $T$  is a global temperature inside the active area and  $F$  the electric field across the amorphous phase. It is calculated through this simplified equation under the assumption of a negligible voltage drop inside the crystalline GST, allowing the access to the amorphous thickness  $u_a$ , straightly linked to the state of the memory (Fig.1).  $V$  is the PCM's voltage, and  $\Phi$  is the activation energy of a single coulombic potential well. It follows the Varshni's empirical law for its temperature dependence,<sup>11,30)</sup> with  $E_{a_0}$  the barrier height at 0K,  $a$  and  $b$  material-related fitting parameters.

The threshold switching is modeled as a thermal runaway in the Poole-Frenkel current triggered by the self-heating of the cell. Any elevation of the temperature in the material being due to the Joule Effect, the temperature is calculated, under the assumption of a short time constant, as,

$$T = T_{amb} + R_{th} * P_J \quad \text{where} \quad P_J = V_{PCM} * I_{PCM} \quad (2)$$

with  $T_{amb}$  the ambient temperature,  $R_{th}$  an effective thermal resistance, taking amongst other the geometry of the cell into account.  $P_J$  is the electrical power dissipated inside the PCM.

As it depends on the current flowing through the cell, the calculation of the temperature implies a positive feedback responsible of the switching inside the amorphous phase. Once it has switched, a series resistance of  $6\text{k}\Omega$  corresponding to the heater resistance limits the current.

Extending the field approximation as long as some amorphous phase exists in the active area – neglecting the voltage drop outside the area – the same Poole-Frenkel current is applied to all the intermediate states as well.  $u_a$  parameter carries the state as it varies from  $0\text{nm}$  to the maximum thickness  $u_{a,max}$  extracted from the full RESET state. The crystalline resistance is said to be semiconducting-type, so it can be expressed as,<sup>31)</sup>

$$R_{cry} = R_{C_0} * e^{-E_{ac}\left(\frac{1}{kT_{amb}} - \frac{1}{kT}\right)} \quad (3)$$

where  $E_{ac}$  is an activation energy and  $R_{C_0} = R_{cry}$  when  $T = T_{amb}$ ; they are both treated as fitting parameters.

### 3. Results and Discussion

#### 3.1 Subthreshold conduction and threshold switching modeling

The comparison of the I-V characteristics between model and measurements for a full range of resistance values is presented on Fig. 4. It shows a very good agreement between data and simulations for two decades of current. The measured resistance is extracted at a constant voltage of  $0.36\text{V}$  during the slow ramping procedure. The current at high applied voltage is fitted by the modeling of the serially connected MOS transistor.

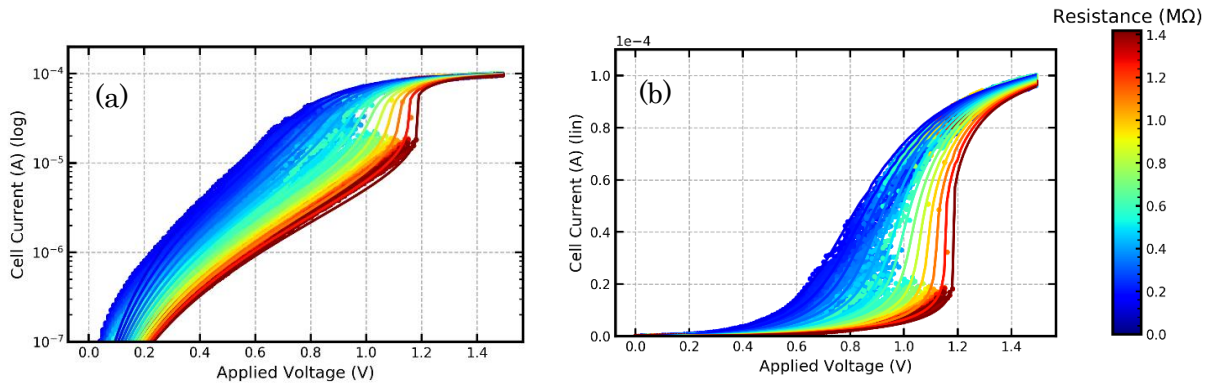


Fig. 4: Cell current versus applied voltage (a) in logarithmic scale and (b) in linear scale for several intermediate states with model (line) and measurements (symbol).

Table I. Model card parameters

Parameter	Value
$R_{th}$	$2.0\text{K}\cdot\mu\text{W}^{-1}$
$A$	$1.45\cdot 10^{-4}\Omega^{-1}$
$\beta$	$24\mu\text{eV}\cdot\text{V}^{-0.5}\cdot\text{m}^{0.5}$
$E_{a_0}$	$0.3\text{eV}$
$R_{heater}$	$6\text{k}\Omega$
$R_{C_0}$	$10\text{k}\Omega$
$E_{a_c}$	$0.1\text{eV}$
$a$	$1.2\text{meV}\cdot\text{K}^{-1}$
$b$	$800\text{K}$

The model card parameters are summarized in Table I.  $R_{th}$  is in good agreement with the commonly accepted value for a high thermal efficiency nanoscale PCM cell.<sup>20)</sup> A value of relative dielectric constant  $\epsilon_r = 10^{11}$ ) implies, accordingly to Poole-Frenkel's theory,<sup>25)</sup>  $\beta = 24\mu\text{eV}\cdot\text{V}^{-0.5}\cdot\text{m}^{0.5}$ .  $a$  and  $b$  parameters have been chosen to fit the self-heating inside the GST but they were kept close to the one found in the literature.<sup>11)</sup> Similarly, the couple of parameters ( $R_{C_0}$ ,  $E_{a_c}$ ) has been chosen to fit the self-heating of the material in crystalline phase for high current density so it is not surprising that it is found higher than previous values.<sup>32)</sup>

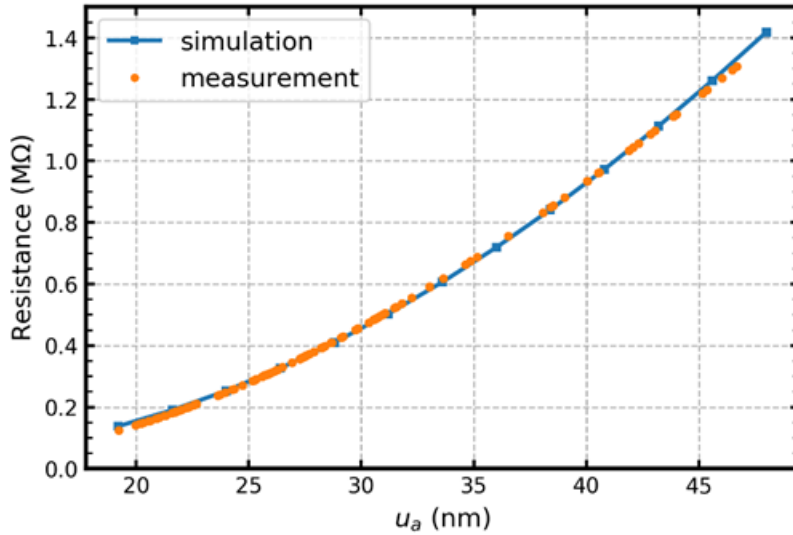


Fig. 5. Resistance of the cell as a function of the amorphous thickness



The only model parameter that varies from one state to another is the amorphous thickness  $u_a$ . Reversing Eq. (1), amorphous thicknesses have been calculated as a function of the measured resistance for each state. The resistance level as a function of the amorphous thickness is given Fig. 5 and one can verify that there is an excellent correlation between the simulated and the measured-based calculated  $u_a$ . It means that  $u_a$  can indeed be used as state parameter for further model-measurement correlation. This allows the computation of the threshold field (cf. Eq. (1)), which is plotted Fig. 6, along with the threshold power (see Eq. (2)), as a function of the resistance of the cell. The threshold is defined as the value of voltage and current where the current in one voltage step of 10mV exceeds a given value of  $1\mu\text{A}$ . Based on this definition, states that are less resistive than  $0.45\text{M}\Omega$  – that have an amorphous dome smaller than  $28.8\text{nm}$  – do not present the threshold switching.

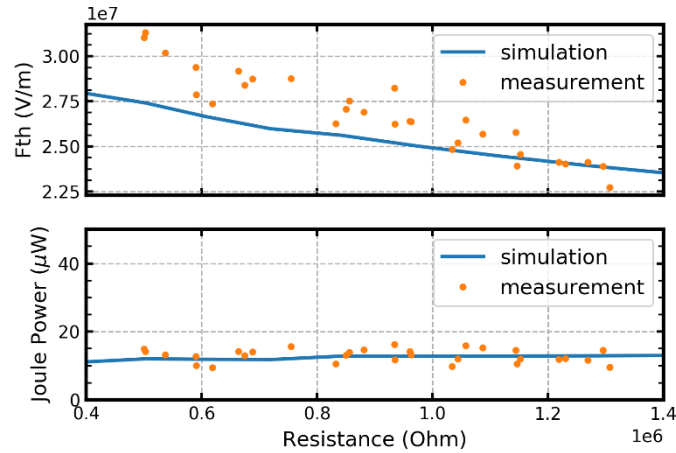


Fig. 6. Threshold field (up) and power (down) versus the resistance of the cell.

### 3.2 Robustness and coherency of the model

The method used for the measurements and simulations presented Fig. 4 was to apply voltage steps on the top electrode and read the current, it is not possible to see a snapback this way. On the contrary, the current-driven simulations for different sizes of amorphous dome shown Fig. 7, exhibit the snapback behavior without any convergence trouble, which illustrates the robustness of the model. The  $19.2\text{nm}$  and  $48\text{nm}$  simulated curves correspond respectively to the minimum and maximum size of amorphous dome measured. Those values are coherent with the height of the deposited GST layer of about  $50\text{nm}$ . The snapback appears for amorphous domes larger than  $28.8\text{nm}$ , this limit corresponding to the minimum size of dome where the threshold is observed.

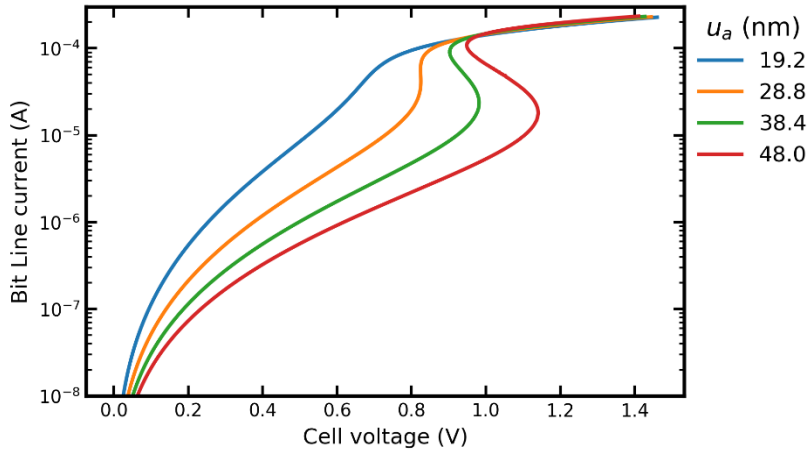


Fig. 7. Current-driven simulation for cell states corresponding to the range measured at 273K. The snapback is observable for states that have an amorphous dome larger than 28.8nm.

As the threshold switching is highly dependent on the temperature calculation, the sub-threshold conduction in full amorphous state ( $u_a = 48\text{nm}$ ) as a function of the temperature has been plotted Fig. 8. The threshold power has been extracted based on the same criteria as before, and it is plotted against the ambient temperature in the inset of the Fig. 8. The subthreshold conduction has a strong temperature dependence, but the threshold seems here again to happen at fixed power. These simulations are fully coherent with previous experiments about threshold switching<sup>11)</sup> and validate that the switching is indeed triggered by a thermal runaway in the model. I-V characteristics simulated for ambient temperature ranging from 0°C to 85°C. The inset plot the threshold power as a function of the ambient temperature, showing a constant trend.

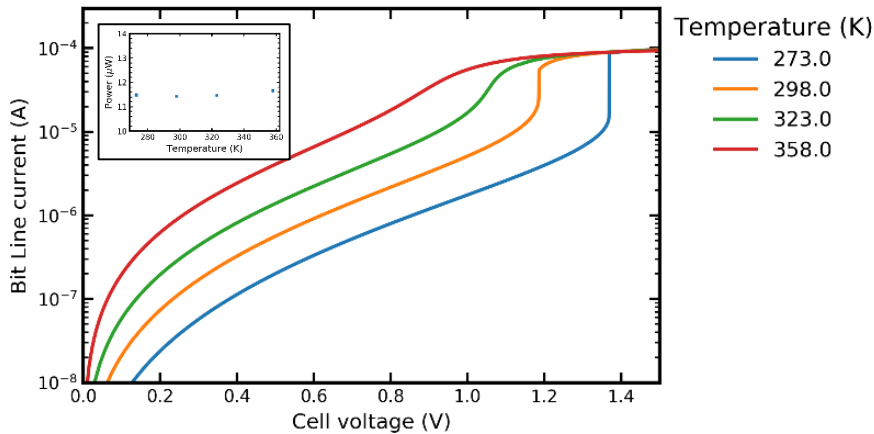


Fig. 8. I-V characteristics simulated for ambient temperature ranging from 0°C to 85°C. The inset plot the threshold power as a function of the ambient temperature, showing a constant trend.

The main roadblock preventing a good multilevel programming of the phase-change memory is for now on the resistance drift, due to relaxation inside the amorphous phase.<sup>2)</sup> The resistance of the cell tends to increase with time, preventing to correctly read the state of the cell after a while. To get rid of the inconvenience, Sebastian *et al.* purposed a new metric  $M$  that is less drift-dependent than the low-field resistance for the cell reading.<sup>33)</sup>  $M$  is defined as the voltage needed to reach a reference current under the application of a linear ramping voltage.  $M$  as a function of  $u_a$  is plotted Fig. 9 for a detection current of  $1\mu\text{A}$ . The simulation presents an excellent correlation with the measurement and both exhibits a linear relationship between  $M$  and  $u_a$ . This proportionality is in agreement with Sebastian's *et al.*, even though the amorphous thickness is not extracted the same way as in article because of the different expression of the subthreshold current used. It confirms the relevance of the choice of  $u_a$  as a state parameter of the model and validates that the model is suitable for multilevel programming.

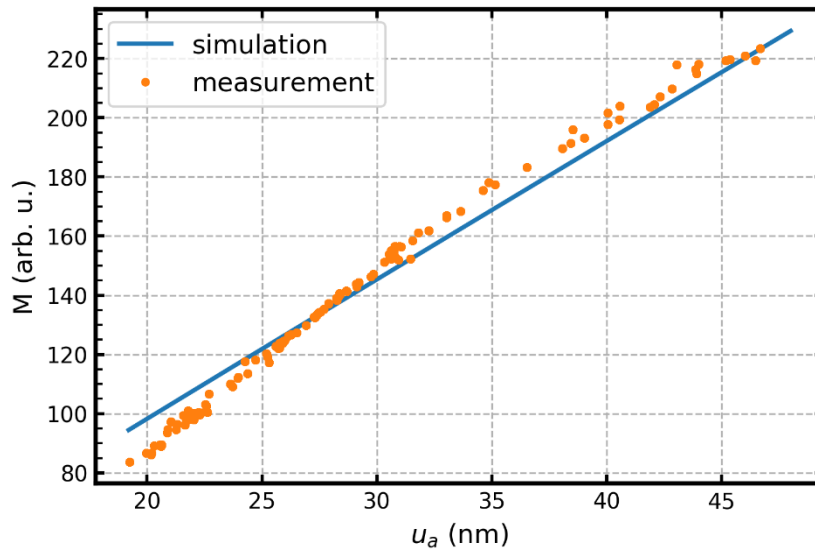


Fig. 9. New metric  $M$  as a function of the amorphous thickness of the state

## 4. Conclusion

This work presents a compact modeling of the threshold switching in phase-change memory based solely on self-heating in the Poole-Frenkel's conduction. This new approach presents the advantage of modeling the current characteristic in a fully continuous way, even the non-linearity of the threshold switching, which eases the convergence and speed-up the simulation time. It has been shown that the model presents a good correlation with measurements

for a wide range of intermediate states and the snapback is natively computed by the model, when driven in current. Besides, the extraction of the threshold properties shows a constant switching power, and so a constant switching temperature, validating the working hypothesis of a thermally activated mechanism. It has also been shown that this new model is compliant with the drift-resilient metric, opening the door of the multilevel programming. This robust and fast-converging subthreshold conduction and threshold switching compact model, once completed by a continuous compact model for phase transition, will be ready for the integration in circuit design tools.

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