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Continuous Multilevel Compact Model of Subthreshold Conduction and Threshold Switching in Phase-Change Memory

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Abstract

A Phase-Change Memory (PCM) physical-based compact modeling of the subthreshold conduction together with the threshold switching is proposed and the results are compared to experimental data collected on a PCM cell embedded in a 90nm technology. The good correlation between simulations and measurements for all intermediate states with a single set of parameters proves the accuracy of the model. Moreover, the constant threshold power measured brings evidence in favor of a thermally activated threshold in nanoscale PCM devices.

1. Introduction

Phase-Change Memory (PCM) has known a growing interest in the previous decade thanks to its unique features of fast switching, low voltages, and high scalability. Now to push this emerging non-volatile solution to an industrial level, designers need a robust compact model to assess for instance the efficiency of full memory array. A difficult part of the PCM modeling is the switching of the amorphous phase to low resistance regime, due to its intrinsic non-linearity. Although it has been considered for a long time as a pure electronic mechanism [1], recent studies have shown a thermal activation in nanoscale memories [2]. Previous works of physical-based compact modeling [3, 4] use a fermi-like smoothing function to simulate the threshold switching whereas it is modeled in this work through the self-heating of the cell. The basic approach is validated through I-V measurements for a large set of intermediate states. The simplicity of the approach is highly interesting in terms of simulation time and convergence ease required in compact model.

2. Experimental Setup and Modeling Method

Test Structure

Measurements are performed on a test structure, manufactured on a 90nm CMOS node with embedded PCM option. This test structure is composed of a PCM stack serially connected to a MOS transistor used as selector. A simplified 2-D schematic of the memory cell is shown Fig. 1. The phase-change material of about 50nm thick is inserted between Top Electrode (TE) and a heater with a wall structure shape [5].

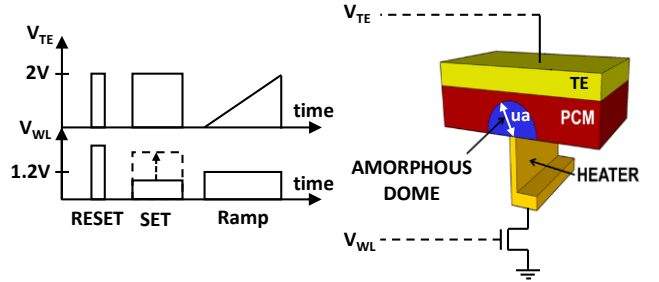


Fig. 1 Schematic of the test structure: a wall-type PCM serially connected to a MOS transistor.

Measurement set-up

A reset pulse of 2V is applied during 200ns before any programming pulse. Intermediates states are then achieved applying a 800ns pulse of 2V on the Top Electrode (TE) and modulating the Word Line (WL) bias between 1V and 2V. A continuum of resistance between 200kΩ and 2MΩ can be achieved this way. Threshold switching is then measured with a 1V/ms ramp (0 to 2V) applied on TE and a WL voltage of 1.2V to control the compliance.

Compact Model

The subthreshold transport has been modeled by a Poole-Frenkel (P-F) current I_{PF} [6,7] given by,

$$I_{PF} = A * F * \exp\left(-\frac{\Phi - \beta\sqrt{F}}{kT}\right) \quad \text{with } F = \frac{V}{u_a} \quad (1)$$

where k is the Boltzmann constant, T the temperature and F the electric field across the amorphous phase. The way it is computed, under the assumption that the voltage drop inside the crystalline GST is negligible, allow the access to the amorphous thickness u_a , straightly linked to the state of the memory. V is the PCM's voltage, β a constant of the material linked to its permittivity, and A is a fitting parameter. Φ is the activation energy and follows the Varshni's empirical law [8] given equation (2),

$$\Phi = E_{a_0} - \frac{aT^2}{b+T} \quad (2)$$

with $a = 1200\mu\text{eV}\cdot\text{T}^{-1}$, $b = 800\text{K}$ and E_{a_0} a fitting parameter.

The threshold switching is modeled as a thermal runaway in the P-F current triggered by the self-heating of the cell. Any elevation of the temperature in the material is assumed to be due to the Joule Effect, so the temperature is calculated, under the assumption of a short time constant [2], as,

$$T = T_{amb} + R_{th} * P_j \quad (3)$$

with T_{amb} the ambient temperature, R_{th} an effective thermal resistance, taking the geometry of the cell into account. P_j is the electrical power dissipated inside the PCM. As P_j depends on the current flowing through the cell, the calculation of the temperature implies a positive feedback responsible of the switching inside the amorphous phase.

Considering that the crystalline semiconducting resistance is negligible as long as the amorphous phase exists in the material, the same P-F current is applied to all the intermediate states as well. The parameter u_a carries the state as it varies from 0nm to the maximum thickness $u_{a,max}$ extracted from the full RESET state.

3. Results and Discussion

The comparison of the I-V characteristics between model and measurements for a full range of resistance values is presented Fig.2. The measured resistance is extracted at a constant voltage of 0.36V. The compliance current is fitted thanks to the serially connected MOS transistor.

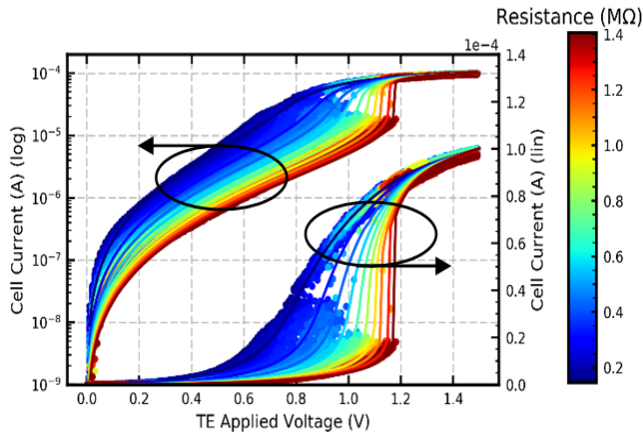


Fig. 2 Cell current versus TE applied voltage for several intermediate states with model (line) and measurements (symbol).

The model card parameters are presented Table I. R_{th} is in good agreement with the commonly accepted value for a high thermal efficiency nanoscale PCM cell, using the wall structure [2]. A value of relative dielectric constant $\epsilon_r = 10$ [2] implies, accordingly to Poole-Frenkel's theory, $\beta = 24\mu\text{eV}\cdot\text{V}^{-0.5}\cdot\text{m}^{0.5}$. The subthreshold slope of the RESET state then gives a coherent value of $u_{a,max} = 48\text{nm}$, compliant with a total GST thickness of about 50nm. The least resistive state achieved here corresponds to 10% of the maximum thickness, i.e. 5nm.

For amorphous caps thicker than approximately $u_a=25\text{nm}$ (resistance above 500kΩ), the I-V curve presents a drop in resistance, called the threshold switching, well captured by

the model. It can be defined as the value of voltage and current where the current in one voltage step of 10mV exceeds a given value of 1μA. Both voltage and power are shown Fig. 3, presenting a good agreement between data and simulations.

Table I Fitting parameters

Parameter	Value
R_{th}	$2.0\text{K}\cdot\mu\text{W}^{-1}$
A	$1.5\cdot 10^{-09}\Omega^{-1}$
E_{a0}	0.3eV

Despite a dispersive extraction, the threshold power can be seen constant, meaning according to equation (3) that the switching happens at a constant temperature of approximately 338K. This is a strong argument in favor of a thermally activated threshold, in line with the work of Le Gallo *et al.* [2].

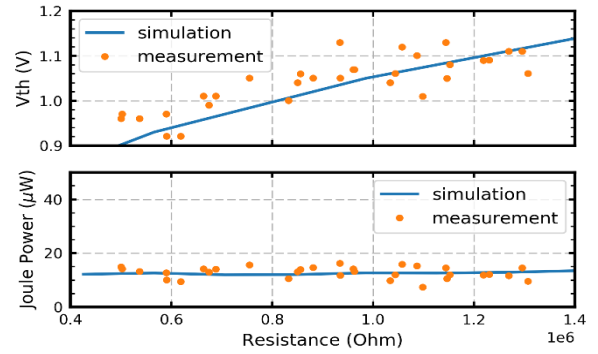


Fig. 3 Threshold voltage (up) and power (down) versus the resistance of the cell.

4. Conclusions

In this work has been shown a physical-based compact modeling of the subthreshold conduction and the electronic switching of a Phase-Change Memory using Poole-Frenkel's conduction associated with self-heating. With a single model card has been fitted I-V measurement of a wide range of intermediate states. Besides, measurements show a constant threshold power well captured by the model, standing in favor of the thermally-assisted switching. Finally, this amorphous conduction and switching modeling enables a complete compact model for phase-change memory.

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