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Impact of a HTO/Al₂O₃ Bi-Layer Blocking Oxide in Nitride-Trap Non-Volatile Memories

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Abstract

In this work, we present an experimental and theoretical study of nitride trap devices with a HTO/Al₂O₃ bi-layer blocking oxide. Such SAONOS (Silicon/Alumina/ HTO/Nitride/Oxide/Silicon) devices are compared with standard SONOS (Silicon/HTO/Nitride/Oxide/Silicon) and SANOS (Silicon/Alumina/Nitride/Oxide/Silicon) memories. The role of the different layers (blocking oxide and control gate) is deeply analyzed, focusing on their impact on memory performance and reliability. Then, a semi-analytical model is developed, which provides a good understanding of the physical mechanisms at the origin of program/erase characteristics.

Keywords

SAONOS; SONOS; SANOS; blocking oxide; charge trapping memories.

1. Introduction

In order to satisfy the continuously increasing demand of non-volatile memories with large capacities, the aggressive scaling of NAND Flash is currently pursued by the main IC companies. In this context, memories based on charge trapping layers, combined with high-k blocking oxides (as SANOS [1] and TANOS (TaN/Al₂O₃/SiN/SiO₂/Si) [2] structures) are widely investigated for sub-32nm node generations. Several studies of TANOS-like structures have been presented, analyzing the retention mechanisms [3-4], proposing the optimization of the

gate stack to improve the performances [5-6], **or simulating the programming-erasing-retention mechanisms [7]**. Replacing SiO_2 with a high-k material, as Al_2O_3 , as top blocking layer of the conventional SONOS device increases the electric field across the tunnel oxide, while reducing the electric field across the blocking layer, during write and erase operations. Therefore, these devices can achieve lower programming voltages and faster programming speed than conventional SONOS. Nevertheless, it has been underlined that when a pure Al_2O_3 layer is used as blocking dielectric, some critical issues appear, especially in terms of data-retention at high temperature and electron back tunnelling during erasing. To solve these issues, the employment of a HTO/ Al_2O_3 bi-layer blocking dielectric has been invoked [6;8-9]. Nevertheless, the identification of the precise role of each layer in nitride-trap memories, and the understanding of the complex physical mechanisms which govern the device performance and reliability, still need further investigations. In this paper, we present an experimental and theoretical study of the role of blocking oxide and control gate in SAONOS (Silicon/Alumina/HTO/Nitride/Oxide/Silicon) devices. Comparison with standard SONOS and SANOS are shown. An efficient semi-analytical model, that allows for the understanding of the critical roles of substrate hole tunnelling current and control gate electron back tunnelling current in nitride-trap memories (during program/erase operations) is finally proposed.

2. Technological Details

Figure 1 illustrates the nitride-trap memory devices studied in this work. Large NMOS transistors ($W=L$ varying between $1\mu\text{m}$ to $5\mu\text{m}$) were fabricated, with different gate stacks. A SiO_2 tunnelling oxide was thermally grown, with thicknesses of 2.5nm and 3.5nm. The charge trapping layer (a 6nm-thick nitride) was deposited by LPCVD. Various blocking oxides were integrated on different devices: a 12.5nm High Temperature Oxide (HTO), or a 16nm-thick Al_2O_3 layer deposited by Atomic Layer Deposition (ALD), or a bi-layer stack composed of 5nm-thick HTO covered by a 8nm-thick Al_2O_3 layer. N+ or P+ poly-Si control gates were finally integrated.

3. Program/Erase dynamics

In this section, we investigate the influence of the blocking oxide on the memory program/erase dynamics. Devices were written and erased by Fowler-Nordheim.

The influence of the blocking oxide on program characteristics is shown in Figure 2. We can observe that the programming speed increases with the high-k blocking oxide compared to the SONOS devices. In fact, the lower EOT of the blocking dielectric boosts the electric field in tunnel oxide during the programming operation, and increases the charge injected in the trapping layer. So the threshold voltage shift increases as the blocking oxide EOT decreases.

The bi-layer blocking oxide gives an acceptable reduction of the threshold voltage shift compared to SANOS devices, due to a small degradation of the gate coupling.

Figure 3 shows the erasing characteristics. Devices with a HTO blocking oxide (i.e. SONOS) cannot be erased, due to the low coupling ratio. An Al_2O_3 blocking oxide gives rise to a faster erasing speed compared to a HTO/ Al_2O_3 bi-layer blocking oxide, due to the improved coupling ratio (i.e. reduced EOT) between the nitride and the control gate. Nevertheless, we can observe that in this case the threshold voltage (V_T) saturation happens earlier because the parasitic electron injection from the gate through Electron Back Tunnelling is limited in the case of the bi-layer blocking oxide.

Figure 4 shows the erase characteristics of devices with HTO (i.e. SONOS) or HTO/ Al_2O_3 (i.e. SAONOS) blocking oxides, with either a N^+ poly-Si or a P^+ poly-Si control gate. As previously said, devices with a HTO blocking oxide and a N^+ poly-Si control gate cannot be erased.

In fact, during erasing, the parasitic electron injection from the control gate (i.e. Electron Back Tunnelling effect, EBT) is larger than the hole injection from the substrate. On the contrary, the use of a P^+ poly-Si control gate reduces the EBT and allows an efficient erasing.

Devices with a HTO/ Al_2O_3 bi-layer blocking oxide do not suffer from this parasitic electron injection. Equivalent erase speeds are obtained regardless of the device gate doping. Nevertheless, in samples with N^+ poly Si control gates, a V_t saturation at high voltages appears.

4. Data Retention

Figure 5 plots the retention characteristics of SONOS devices for different tunnel oxide thicknesses at room temperature and 125°C. It appears that a 3.5nm thick tunnel oxide offers much improved retention performances with respect to a 2.5nm tunnel oxide. Moreover, we can note that no improvement is obtained with a 5nm tunnel oxide. In conclusion, in this configuration ($\Delta V_T=3V$), the charge loss is related to the blocking

oxide leakage current above 3.5nm of tunnel oxide, while for a SONOS device with a 2.5nm tunnel oxide, the leakage current through the tunnel oxide controls the memory retention.

Figure 6(a-b) shows the retention characteristics of devices with different blocking oxides, at room temperature and at 125°C. The best results are obtained with a HTO BO (Blocking Oxide), the main charge loss occurring through the tunnel oxide (0.09V/dec). The 2-layer presents an augmentation of the charge decay (0.11V/dec ~ 25%). In the case of Alumina (0.17V/dec), the charge decay is twice that of HTO, indicating a mitigated leakage current through the tunnel and blocking oxides.

Figure 6(c) shows that data-retention of SAONOS is weakly activated up to 200°C. Moreover we do not observe a degraded behaviour of the high temperature retention after cycling (see Figure 6(d)). Figure 7 shows the Arrhenius plots for Al₂O₃ and a bi-layer BO. Bi-layer BO combines a higher life time (corresponding to a given ΔV_T loss) and a lower temperature activation (or activation energy) compared with Al₂O₃ BO. The different slopes observed on the Arrhenius plots are explained by the different involved charge loss mechanisms depending on the temperature. At moderate temperatures, the charge loss is determined by mechanisms which are not temperature dependent (as direct tunnelling or trap to trap tunnelling). Hence the memory lifetime lowly depends on temperature. On the other hand, at higher temperatures, temperature activated mechanisms become predominant (such as the Poole-Frenkel emission). In this case the life time is degraded as the temperature is increased and a slope is observed on the Arrhenius plots.

Now in order to identify more clearly the role of the HTO layer in the blocking dielectric stack, we studied three samples with either HTO/Al₂O₃ bi-layer or Al₂O₃ as blocking dielectrics, and with a ~3.5nm tunnel oxide. EOT in the same range (Figure 8) were targeted for the blocking dielectrics: 7.3nm for the 2-layer, and 6.6nm or 8.2nm for Al₂O₃ single layer control dielectrics. It appears that the Bi-layer BO presents the best retention characteristics. In particular it exhibits a slower charge loss rate compared to the 8.2nm Al₂O₃ layer, despite a smaller EOT of 7.3nm. This puts in evidence the strong role of the HTO layer which reduces the leakage current during retention due to its larger barrier height compared to Al₂O₃. Hence, these

results prove the high advantage of integrating a HTO/Al₂O₃ bi-layer control oxide for retention improvement, with no degradation of the coupling ratio.

5. Endurance

Figure 9(a) compares the cycling characteristics of nitride-trap devices with a pure Al₂O₃ blocking oxide (i.e. SANOS) and a HTO/Al₂O₃ bi-layer one (i.e. SAONOS). A more pronounced memory window closure appears when pure Al₂O₃ is employed as blocking oxide. As shown in Figure 9(b), the increasing of the **threshold voltage for the erased state for SANOS devices** is due to a degradation of the slope of the erased I_D-V_G characteristics during cycling. The degradation of the slope of the erased I_D-V_G may be explained by **the degradation of the tunnel oxide (confirmed by the presence of DITs) due to the higher tunnel oxide electric field during cycling; or by a parasitic trapping in the Al₂O₃ layer during erasing.**

Very good endurance characteristics, up to 10⁵ cycles, have been obtained on device with the HTO/Al₂O₃ bi-layer blocking oxide by using a smart cycling technique, where the stress time is adjusted at each cycle to keep the programming window opened (Figure 10). **We can note that the programming time has to be increased up to 2ms during cycling in order to keep a constant memory window.**

6. Model

We present here a model which allows a good understanding of the physical mechanisms governing the program/erase operations in nitride-trap memories with high-k blocking oxides.

Band diagrams of the simulated structures and basic equations describing the model are reported in Figure 11. The model considers the charge exchange between the substrate/control gate and the charge-trapping layer (i.e. nitride). The filling current of the charge trapping layer is named mechanism ① while the emptying current is mechanism ②. The electron charges (Q_n) injected in the conduction bands of the nitride layer are linked to the filling electron currents (J_{in,n}/J_{out,n}, respectively) from the substrate and control gate. Currents expressions include different tunnelling mechanisms (direct tunnelling, Fowler Nordheim (FN), or modified FN [11-12]), depending on the device configuration. **The band bending induced by the charges trapped in the nitride layer is taken into account. In our model we neglect the trap to trap tunnelling (taken into account in [7]). In fact this mechanism should be considered only**

in retention mode, at low voltages. Moreover we do not consider any drift or diffusion mechanisms in the nitride layer [13] in order to reduce the computing time. The channel energy levels and the substrate potential are calculated using a Poisson-Schrödinger simulator. We assume that the control gate is metallic, with no poly-depletion and zero hole currents.

Mechanism ② is the output current from the charge trapping layer to the substrate (during erasing) or to the gate (during programming). This current is simulated as direct and Fowler-Nordheim tunnelling [13]. If we apply the Boltzmann statistics to the electrons in the nitride layer, the output current can be calculated by equation (1).

$$J_{out_e} = \sqrt{\frac{2kT}{\pi \cdot m_{HK,e}}} \rho_e \cdot Tn \quad (1)$$

ρ_e is the free charge density in the conduction band of the nitride and Tn is the transparency of top and bottom oxides for electrons located in the nitride conduction band.

The injected charges (Q_n) can either be captured in the traps of the nitride layer (mechanism ③) or reside in the nitride conduction/valence bands as a reservoir of free charges and then be re-emitted through tunnel or control oxides (mechanism ②). The charge trapping phenomenon in the nitride obeys a classical Shockley-Read-Hall (SRH) theory (equation (2)) [14-15], where c_n/c_p are the electron/hole capture coefficients and e_n/e_p are the electron/hole emission coefficients. f_T is the trap filling probability [14] and $N_T=1.8 \times 10^{13} \text{ cm}^{-2}$ the nitride trap density.

$$J_r = [\rho_e \cdot c_n \cdot (1 - f_T) - e_n \cdot f_T] \cdot N_T \cdot q \quad (2)$$

In our model, the emission coefficients take into account the Poole-Frenkel effect.

The traps are considered Amphoteric: both electrons and holes can be trapped. We only consider one common energy level for electrons and holes. This can be justified by the fast recombination rate between two hypothetical energy levels [10]. Moreover, note that the trap energy for holes is particularly critical for the retention of over erase states, which is not studied in this work. Thus, in the same way hole mechanisms are considered:

Mechanisms ④ and ⑤ concern the charge exchange between the substrate/ control gate and the charge-trapping layer.

Mechanism ⑥ describes the capture/emission of holes in the traps of the nitride layer (equation (3)).

$$Jr_h = [\rho_p \cdot cp \cdot f_T - ep \cdot (1 - f_T)] \cdot N_T \cdot q \quad (3)$$

Based on these assumptions, the electron and hole trap rates (Jr_n and Jr_p , respectively) can be computed and we obtain a differential equation system (equation (4)).

$$\left\{ \begin{array}{l} \frac{dQn}{dt} = Jin_e - \sum Jr_{e,i} - Jout_e \\ \frac{dQp}{dt} = Jin_h - \sum Jr_{h,i} - Jout_h \\ \frac{df_{T,i}}{dt} = \frac{Jr_{e,i} - Jr_{h,i} + J_{BT,e,i} - J_{BT,h,i}}{q \cdot N_T} \end{array} \right. \quad (4)$$

Where Qn (resp. Qp) is the charge density on the conduction (resp. valance) band of the nitride.

We assume that the active traps are uniformly distributed in the nitride layer (according to experimental analyses on nitride charge centroid previously reported in the literature [16]), with distributed energies following a Gaussian law ($\sigma=0.2\text{eV}$, $\Delta E_T=1.8\text{eV}$ [17]).

The model allows us to simulate the general trend of write/erase characteristics of nitride-trap devices (as shown in Figures 2 to 4). In particular, the model allows us to provide some insights on the electron and hole currents involved during the erase operation, focusing in particular on the role of the electron back tunnelling effect from the control gate. In Figure 12 we plotted the electron and hole currents which fill/empty the nitride trapping layer, coming from control gate and substrate, for devices with different blocking oxides (the device test configuration corresponds to Figure 3). We can observe that in the case of standard SONOS devices, the electron and hole currents are negligible, explaining the inefficiency of the erase operation. Moreover, the faster erase in the case of a pure Al_2O_3 compared to a $\text{HTO}/\text{Al}_2\text{O}_3$ blocking oxide (see Figure 3) can be explained by the larger Jin_p substrate hole injection (as shown in Figure 12) in SANOS than in SAONOS devices. However the Electron Back Tunnelling (EBT) through Al_2O_3 is higher, thus provoking an earlier erase saturation in SANOS characteristics compared to SAONOS structures (see Figure 3).

Figure 13 represents the tunnelling currents simulations involved during the erasing of nitride-trap memories with different control gates. The values of the substrate injected hole currents (Jin_p) in SAONOS devices with N+ and P+ poly-Si gates are equal up to $t=10^{-3}$ s (see

Figure 4(b)-(d)), which indeed explains that such devices show the same initial erasing speed. However the EBT is higher for devices with a N⁺-poly Si gate: the EBT current equals J_{in_p} at $t \sim 10^{-2}$ s. In other words, our model qualitatively explains that devices with P⁺-poly Si control gates are less sensitive to erase saturation than devices with N⁺-poly Si control gates.

7. Conclusion

In this paper we experimentally studied the influence of the blocking oxide and control gate of SAONOS devices on memory performance and reliability.

SAONOS present a slight loss of program erase speeds with respect to SANOS devices when a higher blocking oxide EOT is used. Nevertheless, the additional HTO layer allows to reduce the Electron Back Tunnelling effect during erasing and the erase saturation issue. The integration of a p+ type control gate also reduces the erase saturation observed at elevated voltages and long erasing times. We also demonstrated that SAONOS devices present the strong advantage of improved retention characteristics (with a lower temperature activation) compared to SANOS memories even for the same gate stack EOT.

Finally, all these effects have been accurately modelled through a semi-analytical model based on the Shockley-Read-Hall theory.

Acknowledgments

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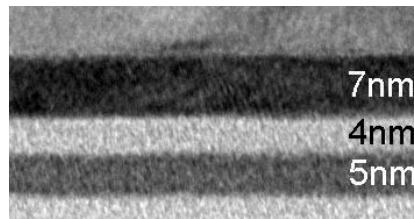
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Figure captions

- Figure 1.** TEM and schematics of the nitride-trap devices studied in this work.
- Figure 2.** Program characteristics of nitride-trap memories with different blocking oxides for 2.5 nm of tunnel oxide (N⁺-poly Si control gate). Symbols: data. Lines: simulations based on our model (see Section VI)
- Figure 3.** Erase characteristics of nitride-trap memories with different blocking oxides (N⁺-poly Si control gate, tunnel oxide is 2.5nm-thick). (symbol: data; lines: simulations).
- Figure 4.** Erase characteristics of nitride-trap memories with different blocking oxides and control gates doping for 2.5 nm of tunnel oxide (symbol: data; lines: simulations).
- Figure 5.** Normalized retention ($\Delta V_T(t=0)=3V$) of SONOS memories for different thicknesses of tunnel oxide at 25°C and 125°C.
- Figure 6.** Data retention of nitride-trap devices with different blocking oxides at (a) 25°C and (b) 125°C. Initial $\Delta V_{T0}=3V$. Data retention of SAONOS memories at different temperatures (25°C to 200°C), (c) before and (d) after 10^4 W/E cycles (control gate is N⁺ poly-Si, tunnel oxide is 2.5nm-thick).
- Figure 7.** Arrhenius plots for Al₂O₃ and bi-layer blocking oxides from 25°C to 200°C. The tunnel oxide is 2.5nm-thick.
- Figure 8.** Data retention of nitride-trap devices with different blocking oxides at 25°C for 3.5 nm of tunnel oxide. Initial $\Delta V_{T0}=6V$.
- Figure 9.** (a) Cycling characteristics of nitride-trap devices with different blocking oxides (N⁺ poly-Si control gate). For SANOS devices : $V_{GW}=14V$, $t_w=5ms$; $V_{GE}=-15V$, $t_w=0.1s$; SAONOS: $V_{GW}=14V$, $t_w=2ms$; $V_{GE}=-15V$, $t_w=0.5ms$. (b) Corresponding Id-Vg characteristics. The tunnel oxide is 2.5nm-thick.
- Figure 10.** Cycling characteristics for SAONOS devices (N⁺ poly-Si control gate) obtained with smart programming techniques (Inset: adjusted **programming and erasing times** as a function of the W/E cycles employed to keep the window opened).
- Figure 11.** Band diagram of the simulated Nitride-trap memories: (a) SANOS during erasing; (b) SAONOS during writing. Mechanisms involved in the device program/erase are illustrated.
- Table 1** Parameters used in the model to fit the experimental data.
- Figure 12.** Simulated electron and hole currents which fill/empty the nitride trapping layer of memory devices with different blocking oxides, during an erase operation at $V_G=-15V$.
- Figure 13.** Simulated electron and hole currents which fill/empty the nitride trapping layer of devices with a HTO/Al₂O₃ blocking oxide and different control gate types, during an erase operation at $V_G=-18V$.

Figure 1

TEM image of SAONOS memory



Schematics of the nitride-trap devices

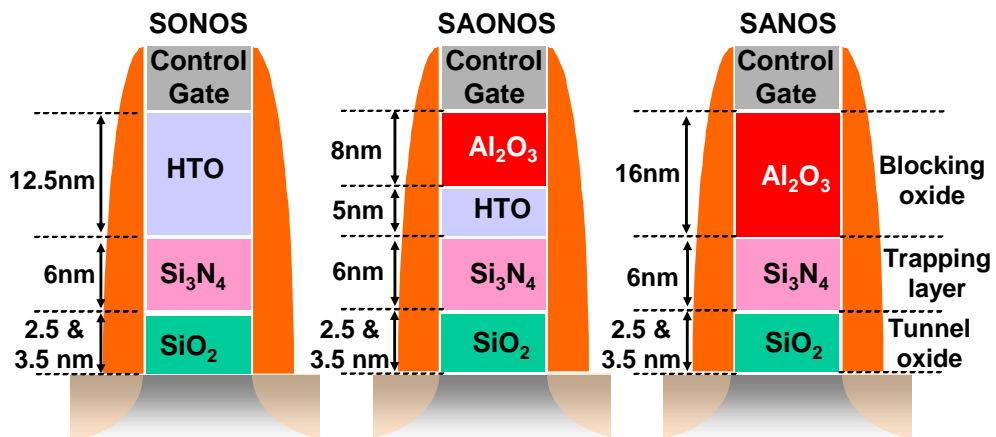


Figure 2

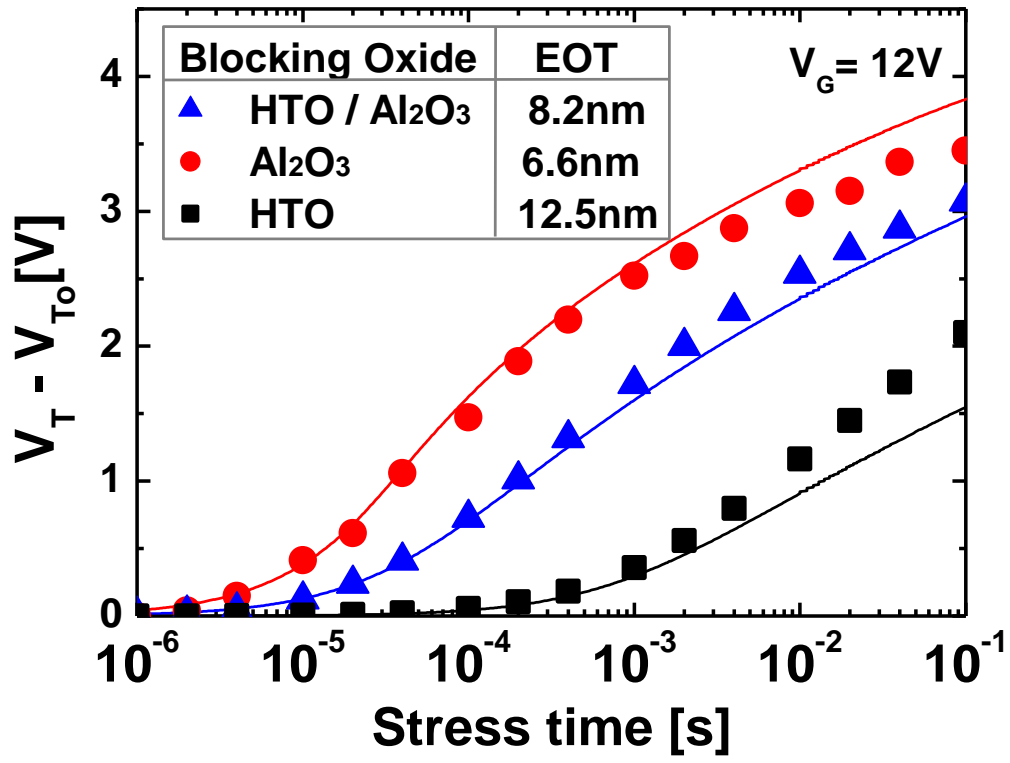


Figure 3

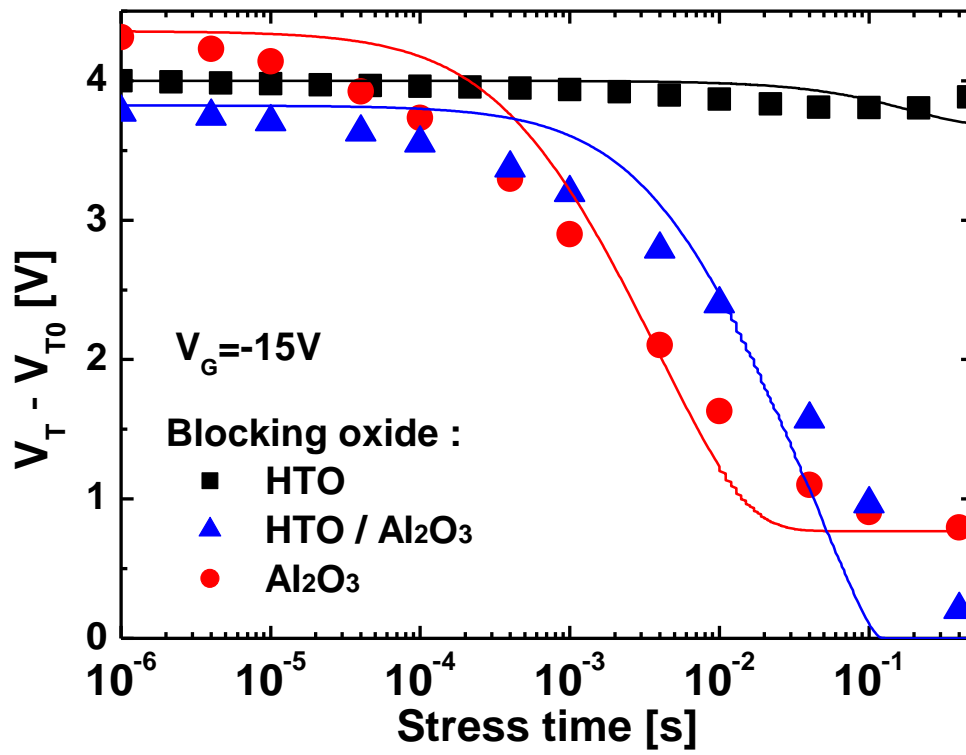


Figure 4

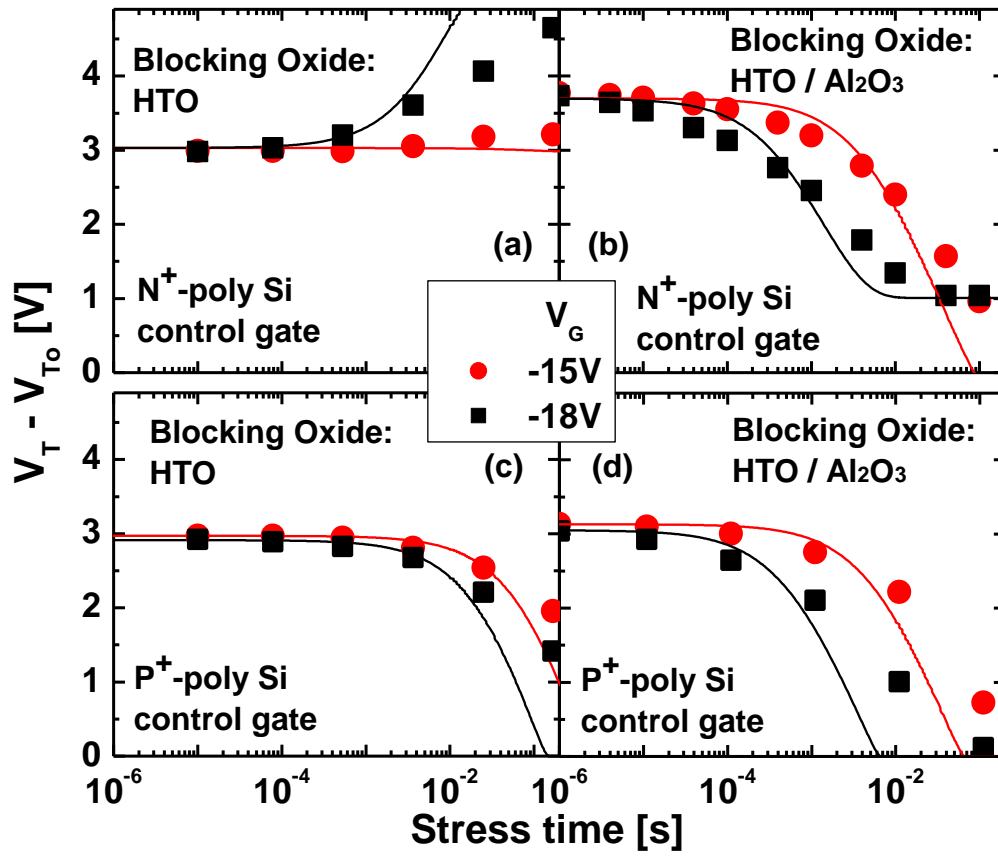


Figure 5

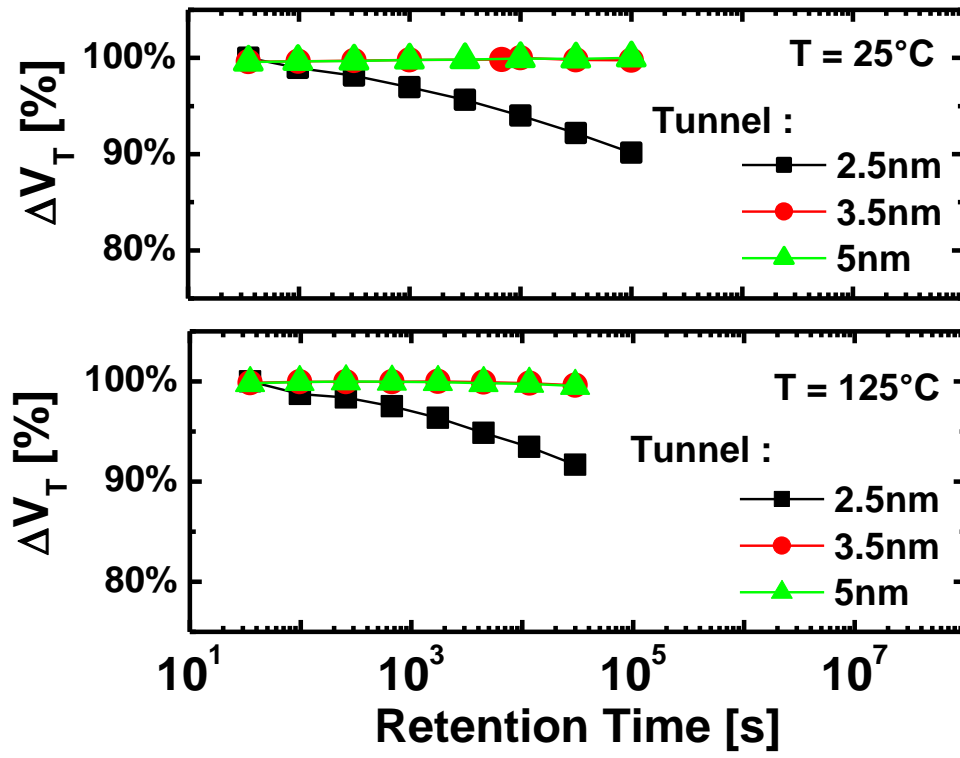


Figure 6

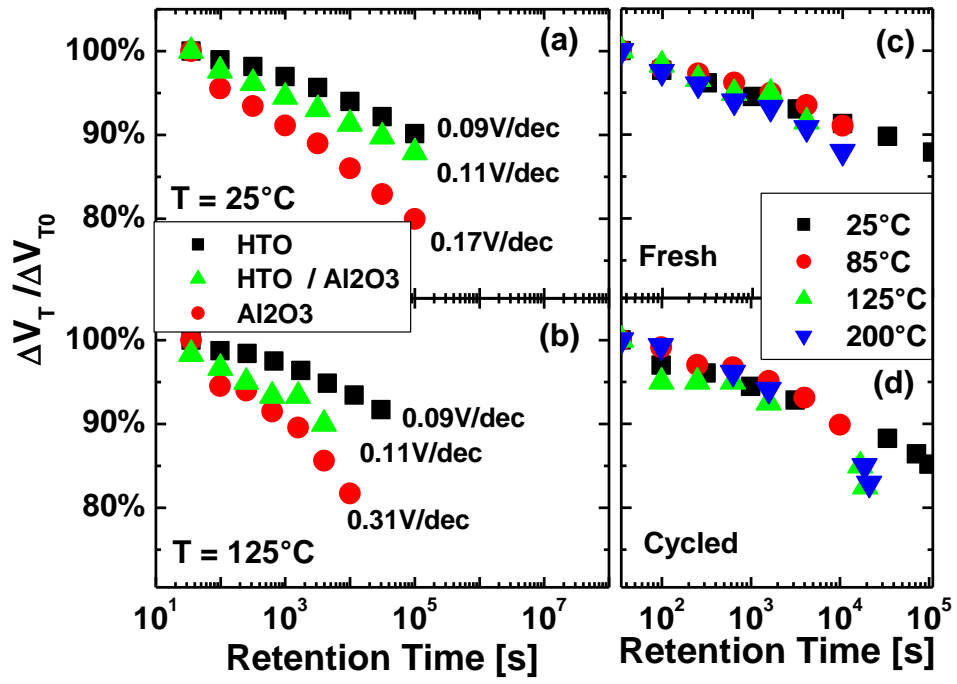


Figure 7

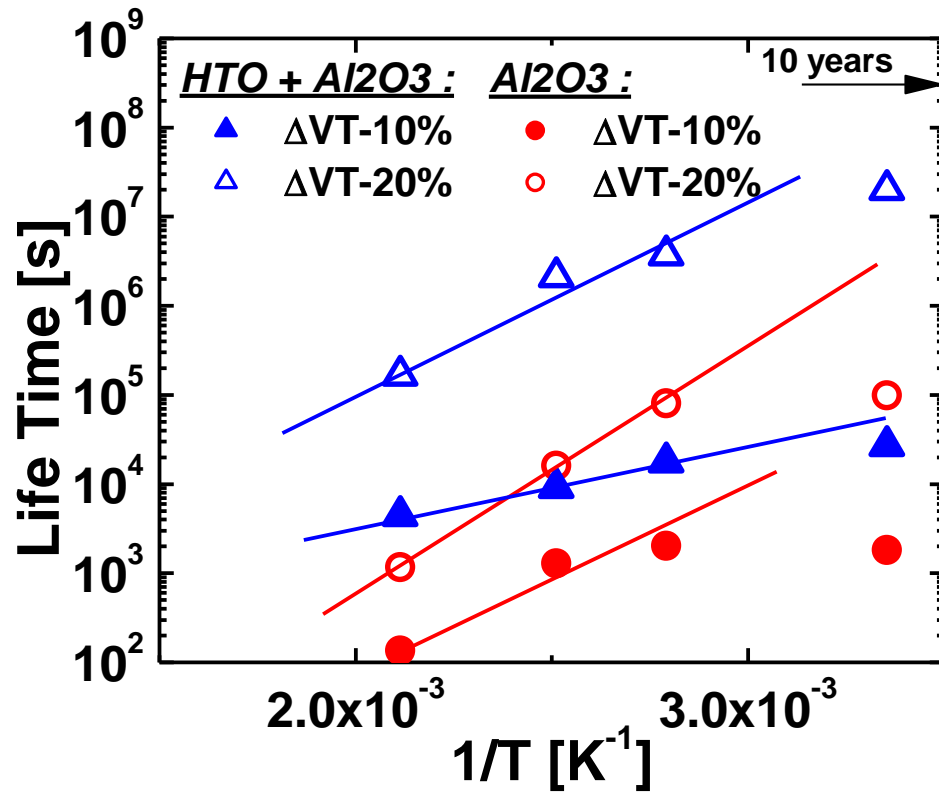


Figure 8

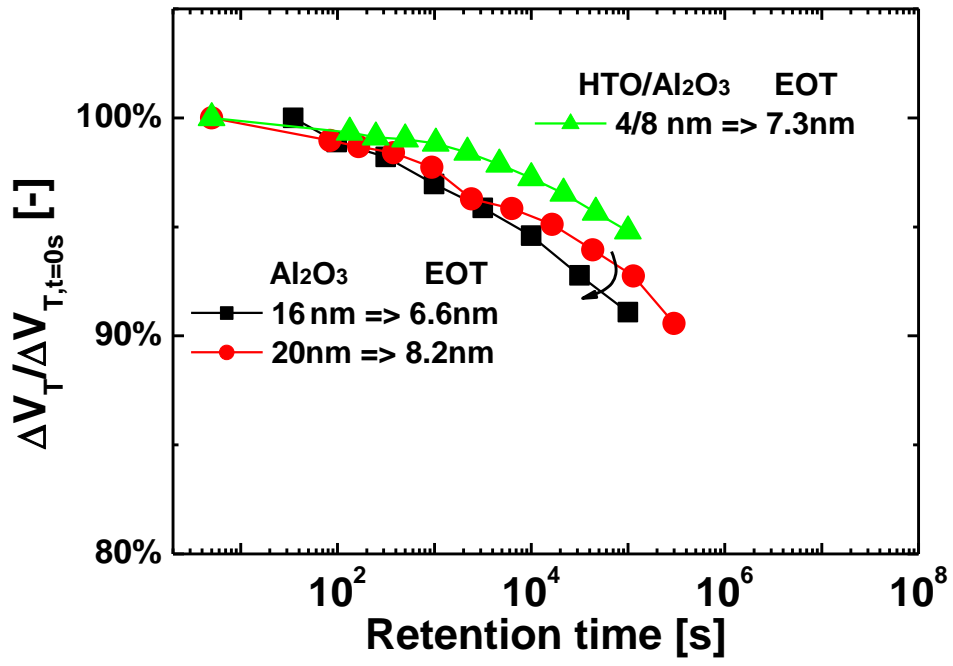


Figure 9

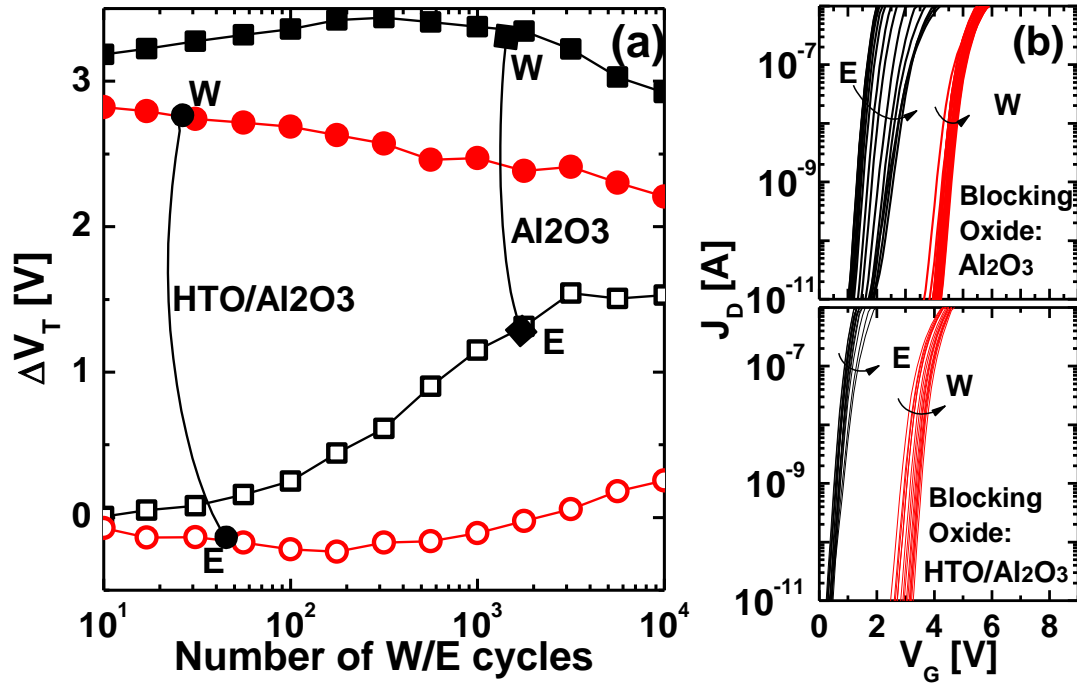


Figure 10

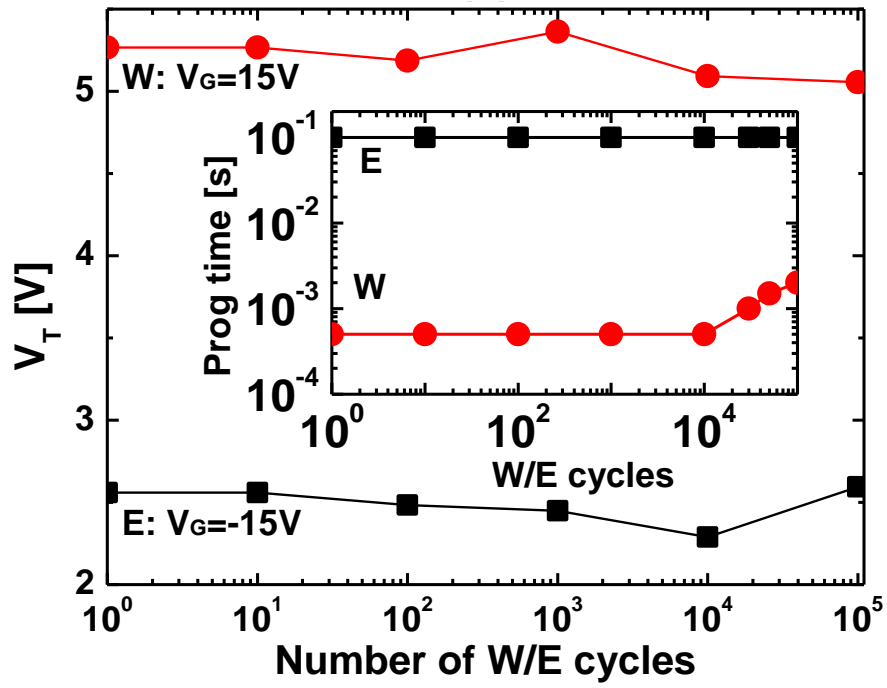


Figure 11

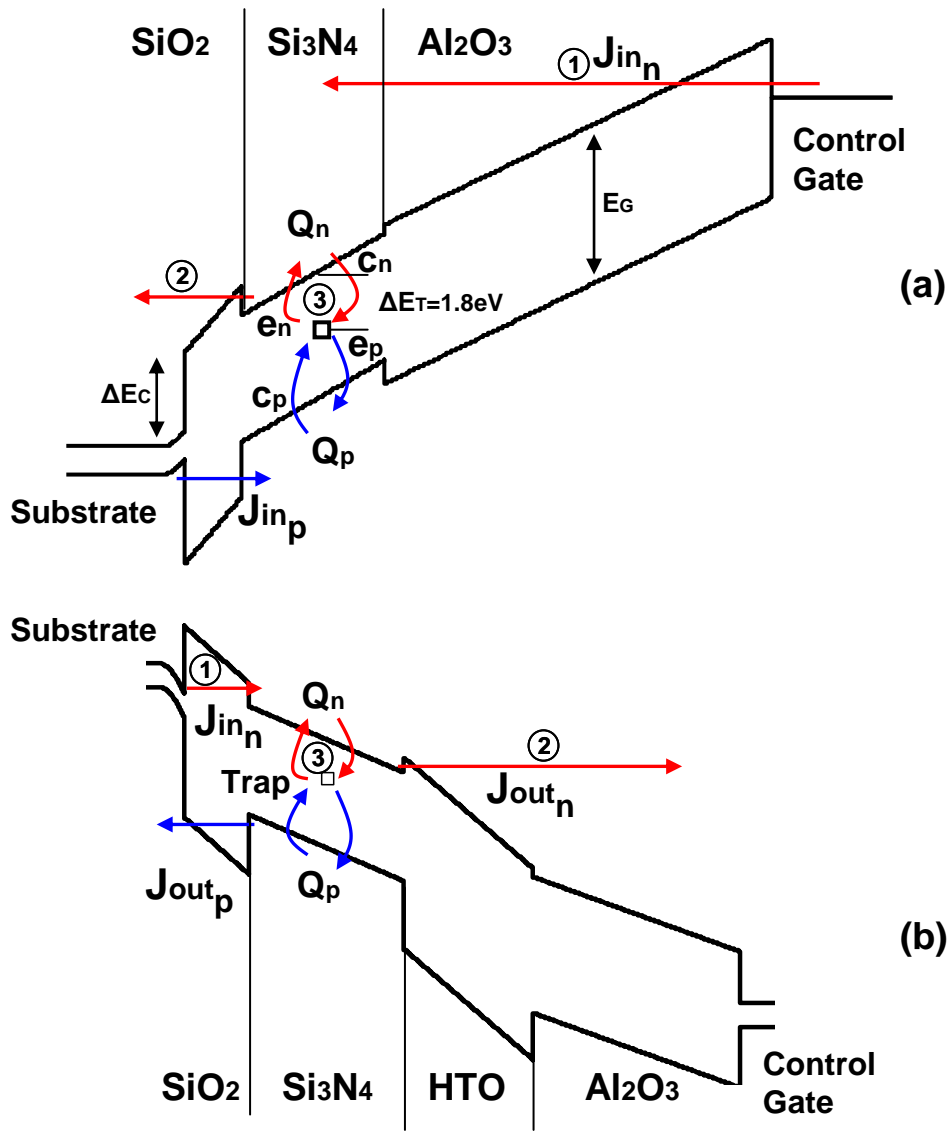


Table 1

	k	E_G	ΔE_c	m_e	m_h
SiO ₂	3.9	8.5 eV	3.15 eV	0.5 m ₀	0.7 m ₀
Si ₃ N ₄	8	5.1 eV	2 eV	0.5 m ₀	0.5 m ₀
Al ₂ O ₃	9	6.4 eV	2.3 eV	0.4 m ₀	-
HTO	4	8.15 eV	2.8 eV	0.4 m ₀	-

Figure 12

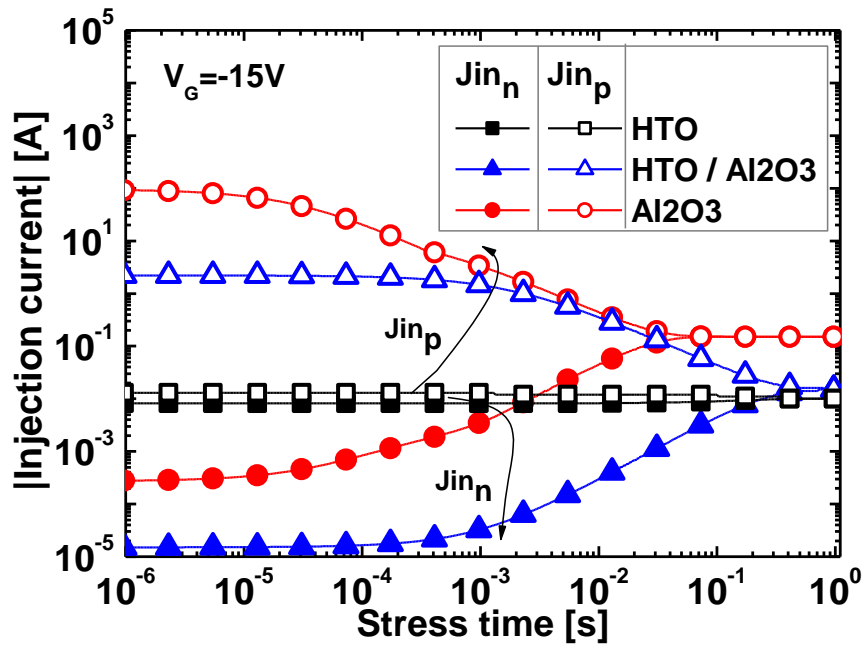


Figure 13

