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A Built-In Self-Test Structure (BIST) for Resistive RAMs Characterization: Application to Bipolar OxRRAM

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Abstract — Resistive Random Access Memory (RRAM) is a form of nonvolatile storage that operates by changing the resistance of a specially formulated solid dielectric material [1]. Among RRAMs, Oxide-based Resistive RAMs (so-called OxRRAMs) are promising candidates due their compatibility with CMOS processes and high ON/OFF resistance ratio. Common problems with OxRRAM are related to high variability in operating conditions and low yield. OxRRAM variability mainly impact ON/OFF resistance ratio. This ratio is a key parameter to determine the overall performance of an OxRRAM memory. In this context, the presented built-in structure allows collecting statistical data related to the OxRRAM memory array (ON/OFF resistance distributions) for reliability assessment of the technology.

Keywords — Resistive RAM, OxRRAM, Reliability, Test, Built-In Self-Test Structure (BIST).

1 INTRODUCTION

In RRAM, the data is stored as two or multiple resistance states of the resistive switching device. Resistive switching in transition metal oxides was discovered in thin NiO films decades ago [1]. Since then, a large number of materials showing a resistive switching have been reported in the literature [2-4]. Among them, metal oxides as HfO_2 , NiO, TiO_2 or Cu_2O are promising candidates due their compatibility with CMOS processes. In its simplest form, resistive memory element relies on a Metal/Insulator/Metal (MIM) stack that can be easily integrated into the Back-End Of Line (BEOL), paving the way for 3D technology. In the same time, new architectures are investigated to provide higher performances [5] [6].

OxRRAM presents a lot of interesting features like high integration density, high-speed operations (write/erase/read) and satisfactory reliability performances in terms of retention and cycling. Hence, OxRRAM memory has been a leading candidate among emerging technologies. However, this technology is still in its “infancy” since the physics of resistance switching is not yet fully understood. So far, it is broadly accepted that the electro migration of oxygen vacancies plays a critical role in the resistance switching. Although OxRRAM-based devices have shown encouraging properties, challenges remain, among which the device variability (or reproducibility) is the main [7]. The variance from switching cycle to cycle and from device to device can be very large. For example, it has been seen experimentally that variability can vary in the range 2x-10x for the ON resistance and 5x-100x for the OFF resistance in Cu_2O -based devices [8].

In OxRRAM memories, MIM structures are used as a single-bit memory cell, while the semiconductor transistor subsystem enables performing all the peripheral operations (input/output, coding/decoding, line driving, and sense amplification) [9]. During the early phase of development it is often difficult to obtain sufficiently reliable data on OxRRAM

memories. Indeed, the process itself is not stabilized and fully functional devices are not yet available. Moreover, a suitable OxRRAM chip currently does not exist and the technology, although rapidly evolving, is currently not sufficiently mature.

In this context, the presented study proposes a Built-In Self-Test Structure (BIST) to evaluate OxRRAM variability at a circuit level. The presented built-in structure allows collecting statistical data related to the OxRRAM memory array. Basically, ON/OFF resistance distributions are extracted at a circuit level, during a READ operation, in a specific test mode without impacting the circuit normal working operation.

Section II introduces OxRRAM technology. Section III presents in detail the BIST circuit. In section IV, simulation results are provided and section V concludes the paper.

2 OxRRAM TECHNOLOGY

In memory devices relying on a resistance change, complex physical mechanisms are responsible for reversible switching of the electrical conductivity between high and low resistance states. The resistivity change is generally attributed to the formation/dissolution of conductive paths between metallic electrodes. Various mechanisms may explain the resistance change (oxygen vacancy migration [4], oxidation-reduction processes, thermal diffusion...).

In working conditions, after an initial electroforming process, the OxRRAM element may be reversibly switched between reset (high resistance) and set states (low resistance). Electroforming stage corresponds to a voltage-induced resistance switching from an initial very high resistance state (virgin state) to a conductive state. In the literature, unipolar, bipolar and non-polar electrical behaviors are reported. In the case of bipolar switching, addressed in this paper, bipolar voltage sweeps are required to switch

the memory element (Fig. 1). Resistive switching in an OxRRAM element corresponds to an abrupt change between a High Resistance State (HRS or OFF state) and a Low Resistance State (LRS or ON state). This resistance change is achieved by applying specific voltage to the structure (i.e. V_{SET} and V_{RES}). Based on the memory cell hysteresis presented in Fig. 1, in a first approximation, four OxRRAM critical reliability parameters can be considered: V_{SET} , V_{RES} , R_{HRS} and R_{LRS} .

3 SIMULATION CIRCUIT

3.1 Circuit architecture

Fig. 2 presents the elementary array used for simulation which is constituted of a 3x3 1T/1R cell matrix, a row decoder, a column decoder and a sense amplifier for the READ operation. The resistor is actually an OxRRAM model presented in the next section. The 1T/1R memory cell (one MOS transistor in series with one resistor) is seen as an effective alternative to replace embedded DRAM-based memory modules by substituting the capacitor by an OxRRAM resistor.

Fig. 3 presents the single-ended sense amplifier (solid line). The circuit working principle is quite simple. During a READ operation, the OxRRAM cell is biased through the row decoder (with $V_{read} > 0$ and WL high). The current cell value (I_{cell}) is generated according to the memory state ($R_{ON} \sim 7k\Omega$ after a SET operation and $R_{OFF} \sim 25 k\Omega$ after a RESET operation). Notice that M_{cell} sizing is critical in terms of current consumption during the programming phase. Indeed, the clamping effect of the select transistor reduces drastically the cell current.

The comparator input V_{IN} is directly proportional to the cell current I_{cell} and therefore to the OxRRAM resistance (two distinct values are available for V_{IN} : $V_{IN SET}$ for R_{ON} and V_{IN}

RESET for ROFF). So that the sense amplifier operates properly, on the one hand the difference between $V_{IN\ SET}$ and $V_{IN\ RESET}$ must be the highest and on the other hand V_{REF} has to be set exactly between $V_{IN\ SET}$ and $V_{IN\ RESET}$ values. In these conditions, the logical value of the cell is correctly sensed and available at the sense amplifier output (OUT).

3.2 BIST implementation

At a circuit level, V_{IN} is the parameter to consider in terms of memory functionality. To extract V_{IN} value, the classical single-ended sense amplifier architecture is modified. A programmable voltage source and a multiplexer are incorporated in the sensing circuit design (Fig. 3, dotted lines) and the READ operation is modified as follow:

- V_{REF} is first set to ground,
- V_{REF} increases step by step from 0 to V_{dd} (V_{REF} increase is controlled by a shift register),
- V_{IN} value is detected when V_{REF} reaches V_{IN} (i.e. $V_{REF} > V_{IN}$ is detected when the sense amplifier output switches),
- V_{IN} is available at the circuit output in a numerical value if BIST_EN signal is set high.

The programmable voltage source is presented in Fig. 4a. Each step of V_{REF} is performed by switching on successively programmable switches. The transmission gates of the voltage source are controlled by the shift register presented in Fig. 4b, which shifts a "1" and has all its other bits set to "0". The shifting process stops when the sense amplifier output switches. At this point, the content of the register is shifted out via the sense amplifier output.

The same structure is used for extraction of both $V_{IN\ SET}$ and $V_{IN\ RESET}$. Besides, the

BIST structure is common to the entire memory array, which reduces the area overhead. The test time overhead is related to the number of programming voltage source steps. In the example presented Fig. 4b, the shift register is designed to perform 20 cycles of consecutive readings, which represents a good tradeoff between $V_{IN\ SET}$ and $V_{IN\ RESET}$ distribution accuracy and test time overhead.

3.3 OxRRAM cell Model

The elementary array used for simulation embeds an OxRRAM model. The proposed OxRRAM modeling approach relies on electric field-induced creation/destruction of oxygen vacancies within the switching layer. The model enables continuously accounting for both SET and RESET operations into a single master equation in which the resistance is controlled by the radius of the conduction pathways (r_{CF}) [10].

$$\frac{dr_{CF}}{dt} = (r_{CF\ max} - r_{CF}) \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea - q \cdot \alpha_{red} \cdot V_{cell}}{k_b \cdot T}} - r_{CF} \cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea + q \cdot \alpha_{ox} \cdot V_{cell}}{k_b \cdot T}} \quad (1)$$

where β_{RedOx} is the nominal oxide reduction rate, E_a is the activation energy, α_{red} and α_{ox} are the transfer coefficients (ranging between 0 and 1), k_b is the Boltzmann constant, T is the temperature and V_{cell} the voltage across the cell.

Moreover, the model makes assumptions of a uniform radius of the conduction pathways, a uniform electric field in the cell and temperature triggered acceleration of the oxide reduction reactions (“redox”). Finally, the total current in the OxRRAM includes two components, i.e. one is related to the conductive species (I_{FC}) and the other to the conduction through the oxide (I_{OX}).

$$I_{CF} = \frac{V_{Cell}}{L_x} \cdot \left(\pi \cdot r_{CF}^2 \cdot (\sigma_{CF} - \sigma_{OX}) + \pi \cdot r_{CF\max}^2 \cdot \sigma_{OX} \right) \quad (2)$$

$$I_{OX} = A_{HRS} \cdot S_{Cell} \left(\frac{V_{Cell}}{L_x} \right)^{\beta_{HRS}} \quad (3)$$

where L_x is the oxide thickness, S_{Cell} is the total area of the device, σ_{OX} the oxidation rate and σ_{CF} the reduction rate. To take into account I_{OX} trap assisted current (Poole-Frenkel, Schottky emission, Space Charge Limited Current (SCLC)), a power law between the cell current and the applied bias is considered with two parameters A_{HRS} and β_{HRS} . Finally, the total current flowing through the cell is:

$$I_{Cell} = I_{CF} + I_{OX} \quad (4)$$

I_{CF} is the main contributor to LRS current (I_{LRS}) and I_{OX} is the main contributor to HRS current (I_{HRS}).

The memory cell compact model is calibrated on silicon. The model was confronted to quasi-static and dynamic experimental data before its implementation in electrical circuit simulators. As presented in Fig. 5a, after calibration, the model satisfactorily matches quasi-static and dynamic experimental data measured on actual HfO_2 -based memory elements (TiN/Ti/ HfO_x /TiN stack reported in [11]). To program a bipolar OxRRAM cell, a voltage ramp is needed. In Fig. 5b, the evolution of SET voltages as a function of the ramp speed is presented. The model implementation focused on this dependence, crucial for the model to be confidently implemented in circuit simulators.

Due to the stochastic nature of the switching process in OxRRAMs, leading to large variability, the OxRRAM model features a variability dependency. The cell variability

modeling is based on OxRRAM card model parameter variations. The variation is chosen to fit circuit experimental data as presented in Fig. 6. A good agreement with experimental data is obtained for $[\beta_{\text{RedOx}} \pm 5\% \text{ and } \beta_{\text{HRS}} \pm 1.5\%]$ (i.e. β_{RedOx} and β_{HRS} are included in the range $\pm 5\%$ and $\pm 1.5\%$ respectively, of a distribution following a Gaussian law). At an electrical level, these variations directly impact ON/OFF resistances.

4 SIMULATION RESULTS

The elementary matrix presented in Fig. 2, embedding the BIST structure presented in Fig. 3, is considered for simulations. Since cell variability is generated based on a targeted technology and memory array architecture, only the realistically possible variations are reported [12] [13].

To validate the BIST structure, a straight correlation between memory cell variability and the sense amplifier output is first established. Then, an application example dealing with the sense amplifier characterization versus variability is presented.

4.1 BIST structure validation

In this study, a large number of Monte Carlo simulations are performed to provide the statistic needed to characterize variability and its impact on the circuit. Cell variation is introduced and simulated sequentially using an electrical simulator. The goal is to track an important shift of the OxRRAM reliability parameters (RON and ROFF). The memory array programming is done in 2 cycles. First, all memory cells are SET (logical “1”), then the memory array is RESET (logical “0”). Logical failures can be detected at the output of the sense amplifier during a read operation after SET/RESET cycles. Variability is introduced through the two model card parameters β_{RedOx} and β_{HRS} .

In Fig. 7a, RON and ROFF distributions are plotted for cell variability included in the range $[\beta_{\text{RedOx}} \pm 5\% \text{ and } \beta_{\text{HRS}} \pm 1.5\%]$. In Fig. 7b, cell variability is increased and included in the range $[\beta_{\text{RedOx}} \pm 10\% \text{ and } \beta_{\text{HRS}} \pm 3\%]$. An important spreading of RON and ROFF parameters is observed in Fig. 7b. Indeed, the initial spreading of RON and ROFF distributions increases according to the variability increase.

In Fig.7c and Fig.7d, $V_{\text{IN SET}}$ and $V_{\text{IN RESET}}$ distributions obtained using the BIST structure are plotted. These distributions are similar to RON and ROFF distributions obtained in Fig.7a and Fig.7b respectively. Indeed, V_{IN} represents the image of the current flowing through the OxRRAM cell. This trend is confirmed by the correlation curve presented in Fig. 8. Therefore, the modified sense amplifier structure can be used as a powerful tool to track any resistance variations but also to characterize the memory array variability.

4.2 Sense amplifier characterization

Fig. 9 presents an analysis of $V_{\text{IN SET}}$ and $V_{\text{IN RESET}}$ distributions versus the reading voltage V_{READ} . For each V_{READ} value, 100 Monte Carlo simulations are performed after a SET and a RESET operation to extract the sense amplifier V_{IN} distributions. Fig. 9 proposes also an evaluation of the cell consumption distributions during a read operation (reported on the left side of the graph, in Femto Joule, which corresponds to the product of the voltage by the current during the READ time). This information is important and underlines the need of a tradeoff between robustness and consumption. For instance, for mobile applications containing OxRRAMs, the trend would be to reduce the cell consumption without compromising reliability.

For instance, to have the highest difference between $V_{\text{IN SET}}$ and $V_{\text{IN RESET}}$ while considering the consumption parameter, V_{READ} can be set to 0.7V with V_{REF} equals to

350mV (dotted lines in Fig. 9). As OxRRAM technology suffers from cell to cell variability, the use of reference cells to obtain a reference voltage to read memory elements is prohibited. Thus, a BIST structure capable to determine on the fly, at a circuit level, the suitable reading voltage reference is a powerful tool for designers to provide robust bipolar OxRRAM memory circuits.

5 CONCLUSION

A Built In Self-Test (BIST) structure is presented for Resistive RAM memories characterization and variability evaluation. The area overhead introduced by structure is relatively low as the structure is integrated in the sense amplifiers. The normal operation mode of the memory circuit is preserved. Besides, extracted values are given in a digital data format, so the extraction process does not required any analog pin on the tester, making it fully digital tester compliant or easily observable via the random logic. As variability in OxRRAMs presents a major challenge for fabrication process and design engineers, the BIST structure can be used to quickly evaluate cell variability impact on the ON/OFF resistance ratio of a whole memory array. From a design point of view, BIST data can provide interesting guidelines at a circuit level to design robust bipolar OxRRAM memories.

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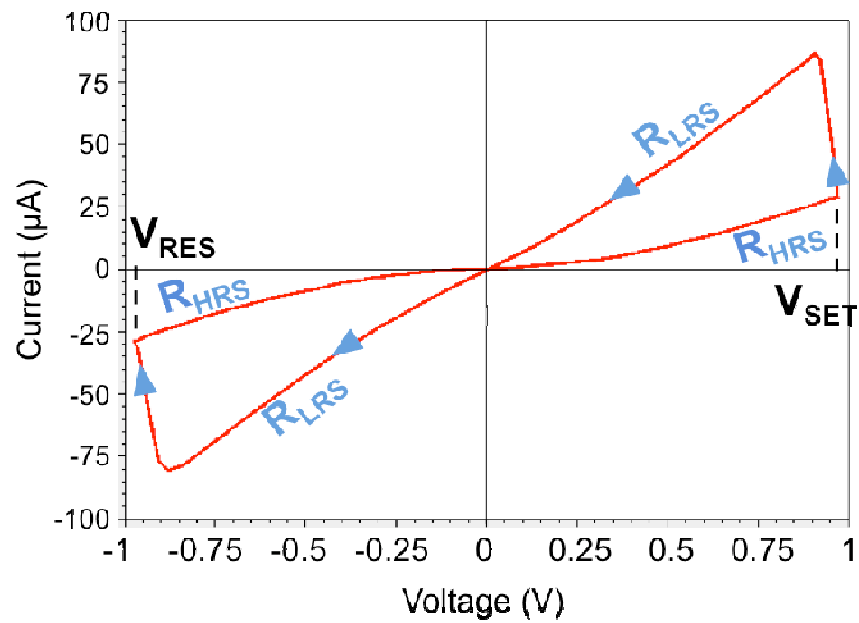


Figure 1. Typical I-V characteristic of a bipolar OxRRAM cell

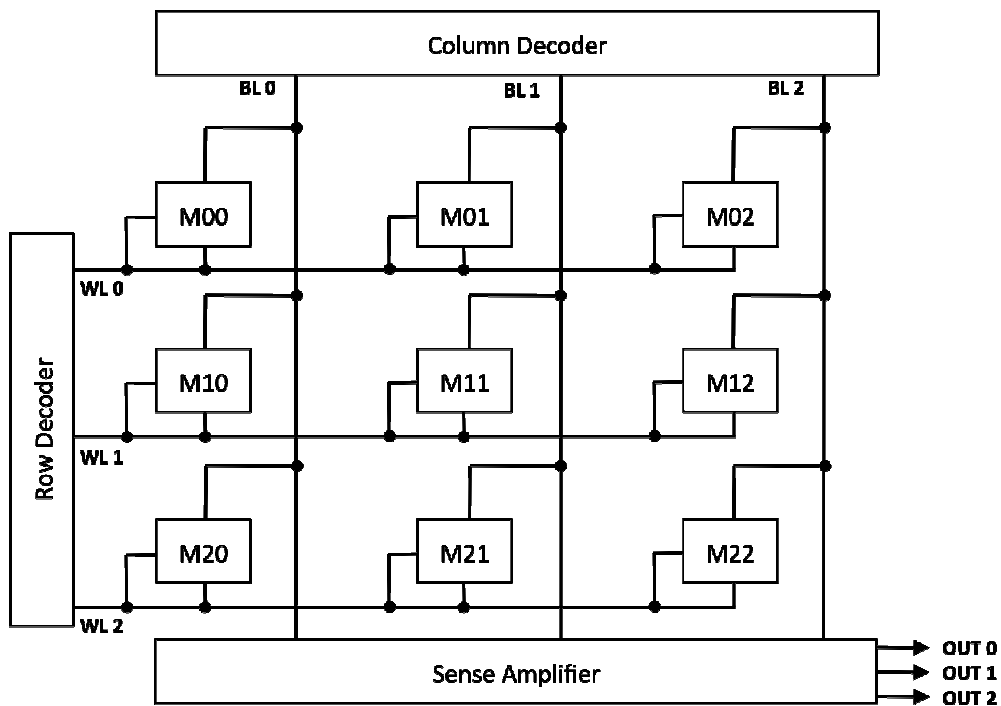


Figure 2. 3x3 OxRRAM memory array

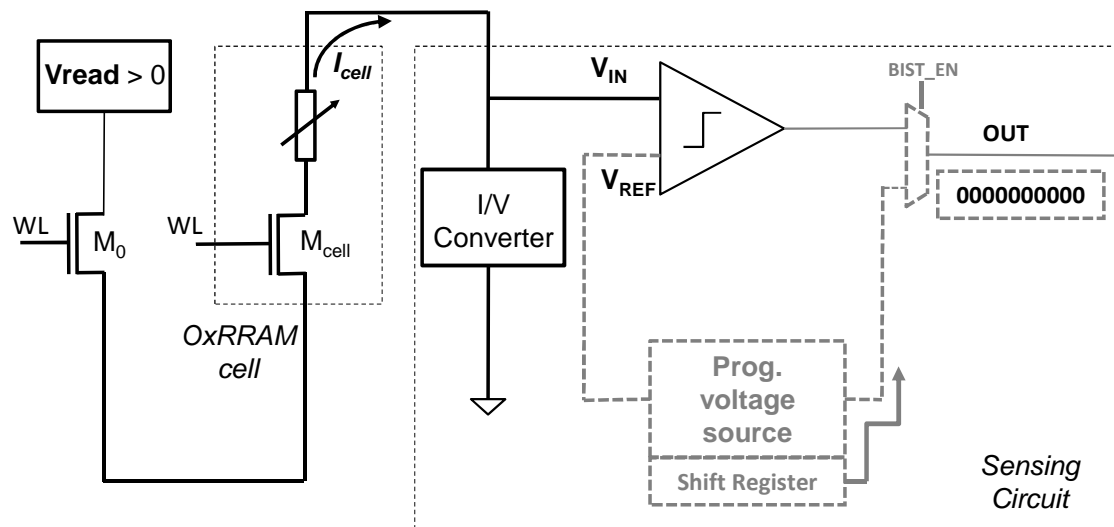


Figure 3. OxRRAM sensing circuit

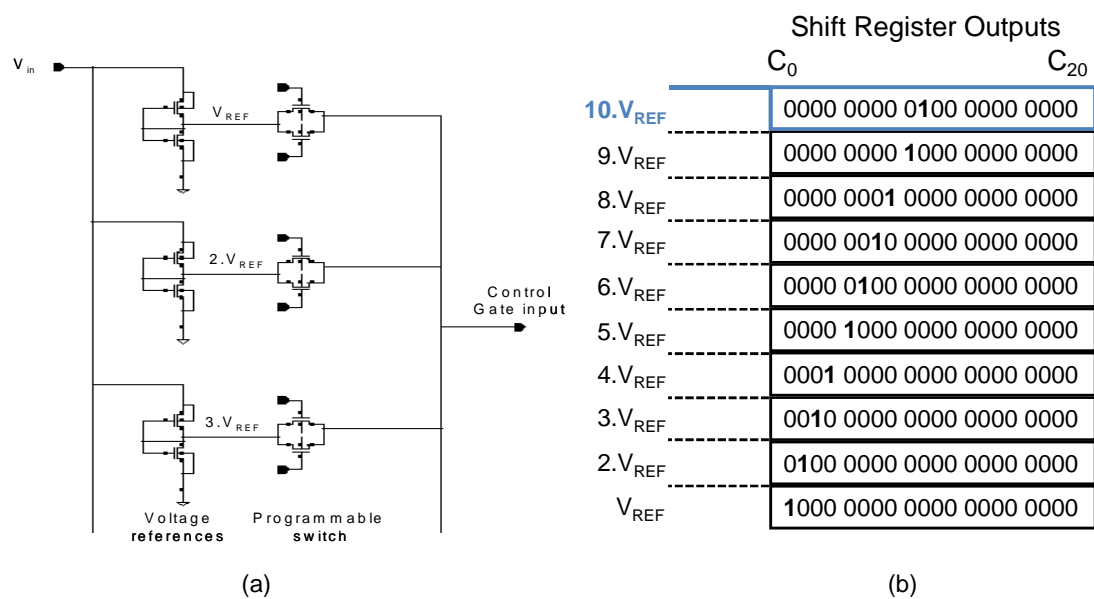


Figure 4. Programmable voltage source (a) and shift register (b)

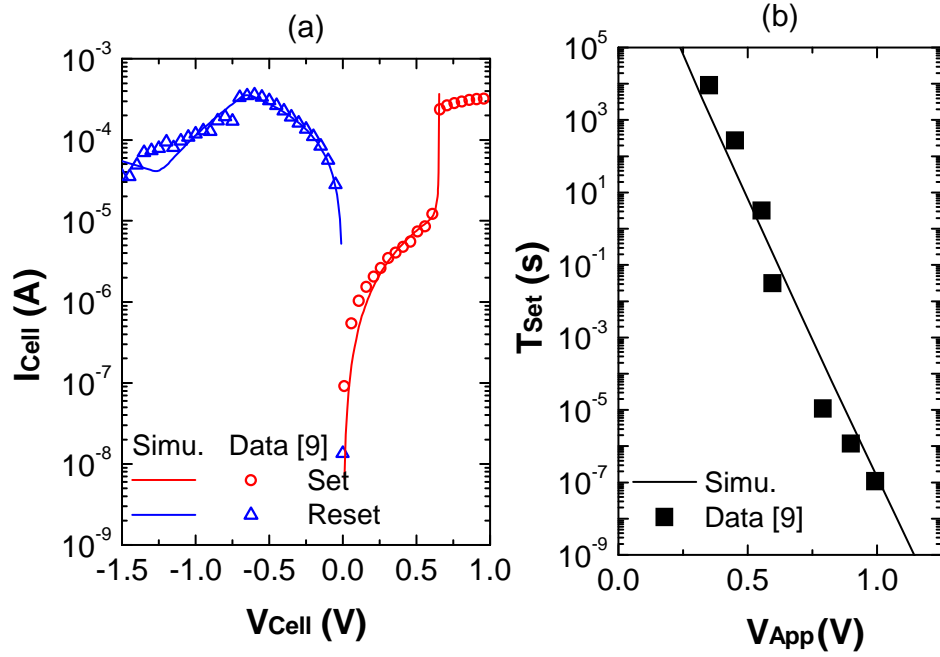


Figure 5. I-V characteristic measured on HfO₂-based devices (a) [11] and corresponding simulation using a bipolar OxRRAM physical model. Set voltage as a function of the programming ramp (b)

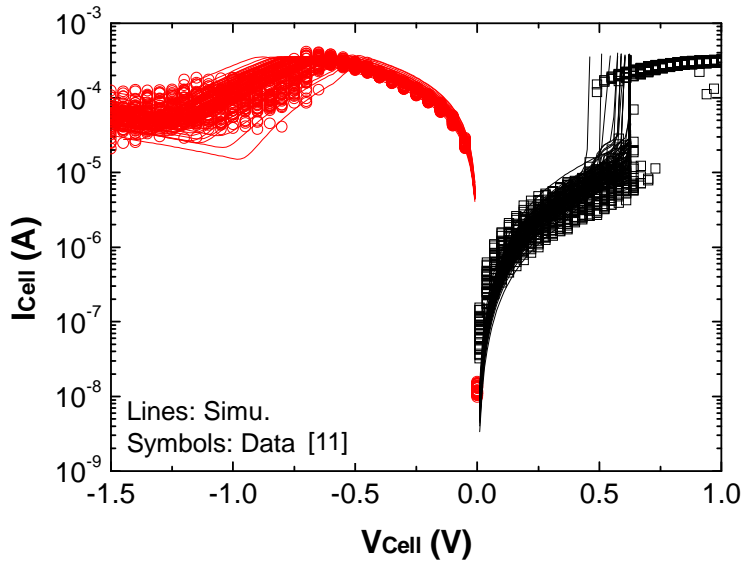


Figure 6. RON and ROFF distributions versus cell variability. Model calibrated on experimental data for specific card model parameter variation [$\beta_{RedOx} \pm 5\%$ and $\beta_{HRS} \pm 1,5\%$]

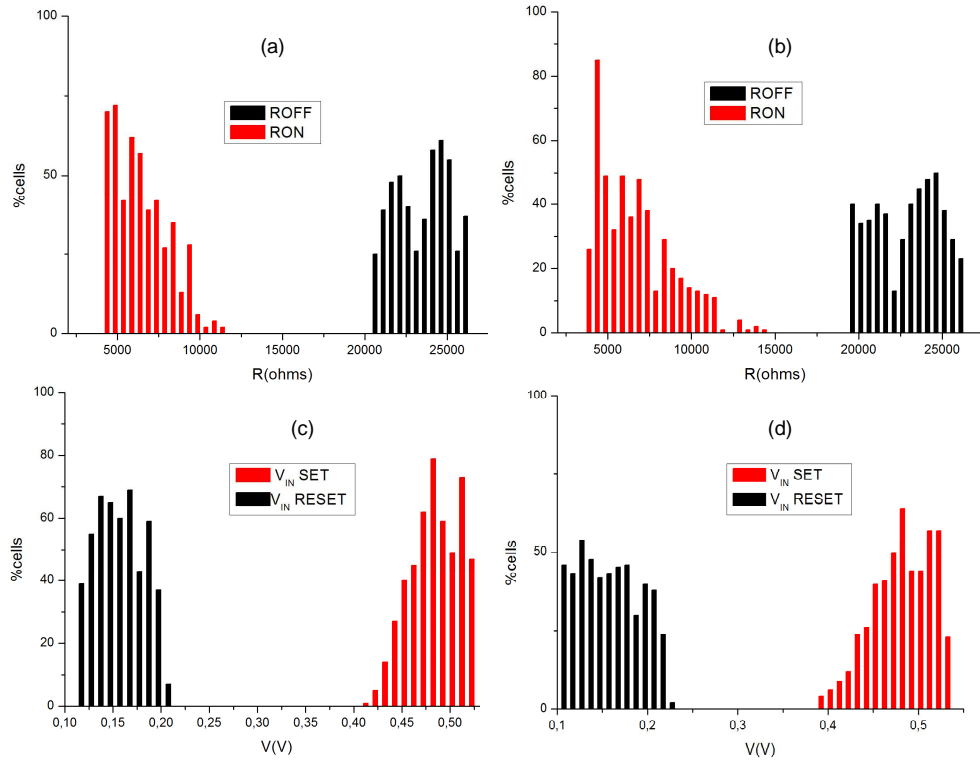


Figure 7. RON and ROFF distributions versus cell variability after 500 Monte Carlo runs. Cell variability included in the range $[\beta_{RedOx} \pm 5\%$ and $\beta_{HRS} \pm 1.5\%]$ (a) and in the range $[\beta_{RedOx} \pm 10\%$ and $\beta_{HRS} \pm 3\%]$ (b). Corresponding SET/RESET V_{IN} voltage distributions (d), (e).

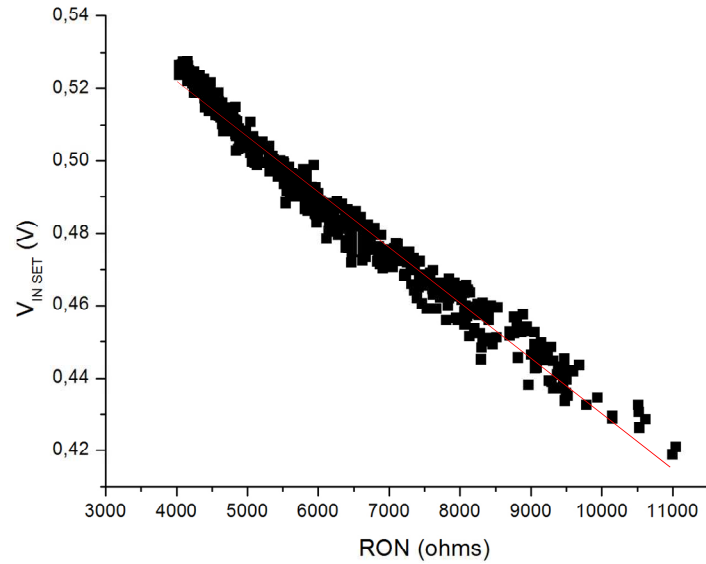


Figure 8. RON versus $V_{IN\ SET}$ correlation graph

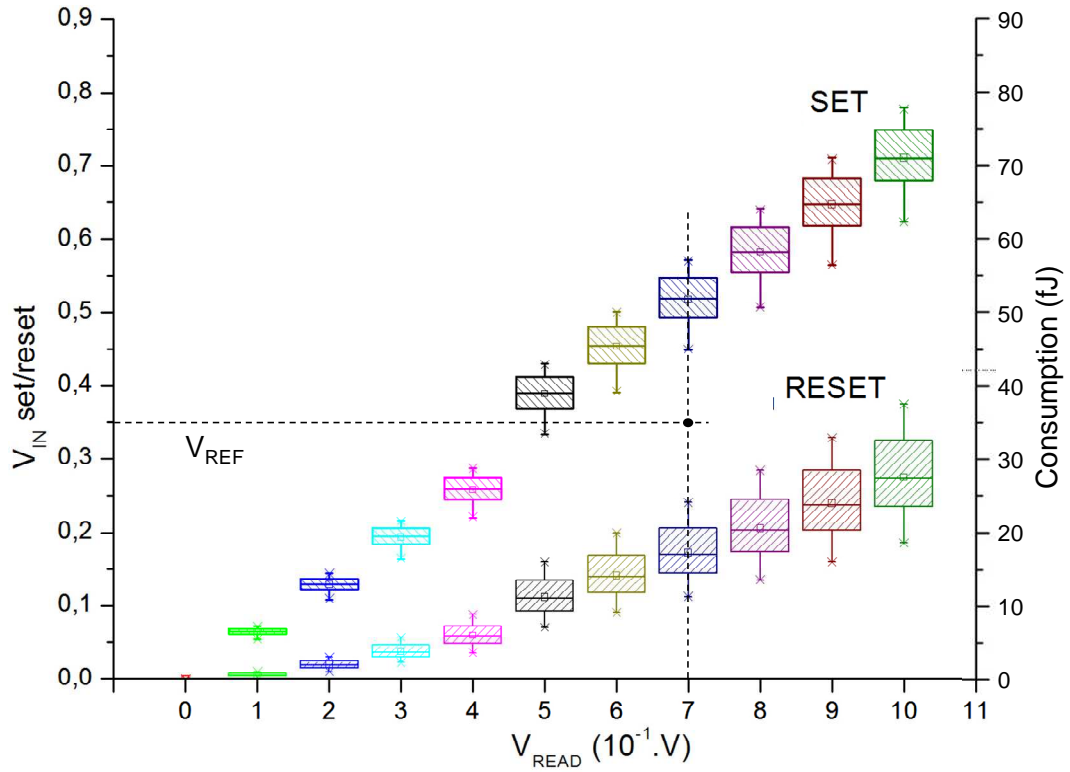


Figure 8. $V_{IN\ SET}$ and $V_{IN\ RESET}$ distributions versus cell variability [$\beta_{RedOx} \pm 5\%$ and $\beta_{HRS} \pm 1.5\%$] after 100 Monte Carlo runs @ $V_{read} = [0V, 1V]$