High-Temperature Coplanar Transformer

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***Abstract*—Power electronics tends to go higher in frequency and higher in power density. This requires integrated transformers which are able to withstand high temperature (over 200℃). This paper addresses the manufacturing and test of low power transformers used for the isolation in gate circuits power supplies.**

The transformers are built from a magnetic substrate (ferrite) using a microfabrication process detailed in the paper.

The presented transformers are intended for power below 1 W, voltage circa 10 V, switching frequency of 1 MHz, temperature ranging from –55℃ to 200℃ and an isolation capacitance below 10 pF.

***Index Terms*—Transformer, microfabrication, thick film inductors**

I. Introduction

Power electronics converters require transformers working as signal or power transformers. This is particularly true for the gate driver circuits, used to drive large power transistors. A half-bridge structure, as encountered in many converters, requires pulse transformers (to transfer the switching orders to the "upper" transistor) and an insulated power supply (to transfer energy to the gate drive circuit of the "upper" transistor). The recently introduced wide-band gap power transistors [1] can operate at higher junction temperature: most silicon-based devices are limited to 175 °C or less, while some SiC or GaN transistors can operate well beyond 200 °C. This enables converters operating in harsh environments (aeronautics, automotive, oil and gas extraction) [2], providing the other components of the converter can sustain such conditions.

Overall size reduction is also an important objective, and an efficient way to achieve it is to reduce the footprint of the transformer. To optimize the transformer footprint and volume, we propose to use microfabrication techniques starting from a magnetic substrate. This offers many advantages: high manufacturing resolution (thanks to photolithography), allowing finer structures to be built, batch manufacturing (many transformers are made simultaneously), and good performances (windings are made using pure copper, and a high performance magnetic material can be used).

A comparable manufacturing technique was previously applied to inductors [3] made on a YIG (Yttrium Iron Garnet) substrate. However, while YIG is non-conductive, this is not the case of the ferrite used here. Characterization of the magnetic material showed a non-negligible conductivity of $0.38\,\mathrm{S/m}$. An electrical insulation layer is therefore required between the copper windings and the magnetic substrate. This insulation is done using a 2 µm-thick silicon dioxide (SiO_2) layer, a material commonly used in microfabrication, and which offers very good dielectric properties (breakdown field of several hundreds of kilovolts and conductivity of $1 \times 10^{-15}\,\mathrm{S/m}$) and is capable of operating at high temperature.

The next section is dedicated to presenting the fabrication process. Section III describes the design of the transformer. Corresponding prototypes were made, and their characterization is presented in section IV.

II. Microfabrication

The process described here is based on previous work described in [3]–[5]. The original process was improved by replacing the YIG substrate with a more suitable ferrite material, adding a dielectric layer (silicon dioxide) to improve the insulation of the transformer, and placing a second magnetic element to create a closed magnetic path.

A. Substrate insulation method

The insulation process consists in two separate steps: first, the substrates are prepared (this includes wafering and polishing) and then they receive a coating of SiO_2.

Ferrite blocks (PLT64/50/5 made of 3F45 Ferroxcube) are cut into thin slices (≈1 mm) using a low-speed diamond saw (Escil Labcut 150). To achieve a suitable surface condition for silicon dioxide deposition and remove slicing striations, the substrates are attached to a metal support (using Buehler Crystalbond 555 mounting wax) and then polished (Presi Mecatech 334), starting with P1200 grit paper, followed by diamond slurries ranging from 9 µm down to 1 µm particle size. This results in a mirror finish. The substrates are removed from their support using hot water.

A careful cleaning is then performed to remove mounting wax residues and loose ferrite particles. The cleaning consists in three successive baths of 1 min each of deionized water heated up to 80 °C. After that, sample must be placed in a crystallizer of acetone during 2 min and dried and then in a crystallizer of ethanol during 2 min and dried. Both crystallizers are used in a heated ultrasonic cleaner.

A 2 µm-thick layer of SiO_2 is then deposited via plasma-enhanced chemical vapor deposition (PECVD), using an Oxford PlasmaLab 80+ reactor fed by a helium-silane mix and nitrous oxide as precursor.

B. Conductor growth

Despite their relatively low power rating (1 W), the transformers require thick (several tens of microns) copper windings, to

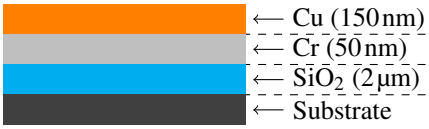


Figure 1: Isolated magnetic substrate (cross-sectional view)

ensure low winding resistance. Such copper thickness is usually achieved using electroplating.

As electroplating requires a conductive surface, thin "seed" metal layers must be applied to the SiO_2 surface. They are made using physical vapor deposition (PVD). A 50 nm-thick layer of chromium is used as an adhesion layer and a 150 nm thick layer of copper is used as a deposition layer, intended for conductor growth. In previous work [3], a titanium-based adhesion layer was used. However, titanium etching relies on HF-based chemicals, which would also react with the underlaying SiO_2 layer. Chromium etching solutions do not attack $Si0_2$.

The resulting isolated magnetic substrate and seed layers stack is depicted in Fig. 1.

Next, winding patterning is performed using photolithography. A dry photosensitive film (Dupont PM275, a 75 µm thick film) is laminated onto the substrate.

1) Film lamination: The film is laminated onto the magnetic substrates using a M300 laminator (Bernier Electronic) set at 110 °C, using the lowest speed and pressure settings. After lamination, the film is checked for wrinkles, and trimmed at the substrate size.

2) Photopatterning: Photopatterning is performed on a Quintel Q2001CT mask aligner, using plastic photoplotted masks commonly used for PCB manufacturing (6000 dpi resolution, from Laser Techno, France). Exposition is 5.6 s long with a 150 W power 365 nm UV lamp.

3) Development: As recommended by Dupont [6, p. 3], a 1% solution of sodium carbonate (Na_2CO_3) heated up to 30 °C is used. Development requires a steady spray (Braun oxyjet) maintained close to the film for 60 s.

4) Electrodeposition: Both anode (pure copper electrode) and cathode (substrate) are plunged into copper electrodeposition bath [5, p. 1669]. This is an acid solution made of:

- 220 g/L of copper sulfate ($CuSO_4$–H_2O),
- 32 mL/L of sulfuric acid (H_2SO_4),
- 8 mL/L of Rubin T200-G,
- 2 mL/L of Rubin T200-A,
- 2 mL/L of Rubin T200-E,
- 0.2 mL/L of hydrochloric acid.

They are connected to a Source and Measure Unit (SMU) Keithley 2410 which allows a precise current supply. Electrode polarisation allows the formation of metallic ions at the anode, which dissolve into the electrodeposition bath and then migrate to the cathode (substrate). The used current density is 10 mA/cm^2 which allows a 12 µm/h deposition rate.

5) Film and seed layer stripping: The final step consists in removing the dry photosensitive film and seed layers (the seed layer is made of conductive materials, so it must be stripped to prevent short-circuits). The dry photosensitive film is removed using a sodium hydroxide (NaOH) 3% solution heated up to 50 °C [6, p. 3]. For the seed layers, copper is etched first with Transene APS-100 copper etchant heated at 40 °C during 30 s.Then, chromium is etched by Transene chromium cermet etchant TFE heated at 50 °C during 30 s.

Finally, appropriate cleaning in order to prevent oxidation can be done.

- Rinse in a deionized water in a crystallizer (1 min),
- Rinse in running deionized water (1 min),
- Rinse in an ethanol crystallizer (3 min),
- Dry in a stream of nitrogen.

An example of a microfabricated tapped transformer is given in Fig. 2.

Figure 2: Microfabricated tapped transformer. (dimensions are given table II)

C. Final assembly

Thanks to the batch fabrication process, several transformers are built simultaneously on the same magnetic substrate. They are separated using a wafer dicing saw (Disco DAD 3220).

In some cases, to improve coupling between the primary and secondary of the transformer, a U-shaped ferrite cap is placed on top of the windings. This U-shaped core is also machined using the wafer dicing saw, manually placed on top of the transformer, and held in position with some polyimide adhesive tape. Adhesive tape was preferred as it does not introduce any additional spacing between the magnetic substrate and the ferrite cap (this would introduce an air gap in the magnetic path and degrade the coupling).

External interconnects are performed using gold ball bonding (50 µm wire) as shown in Fig. 3 after the transformer has been attached on a printed circuit board.

III. Design

This section describes the actual design of the transformer. It starts with the specifications given in table I, and the limits

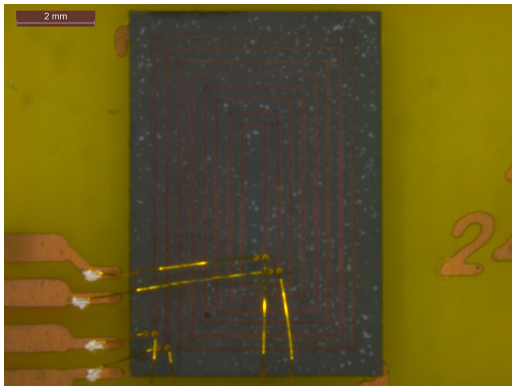


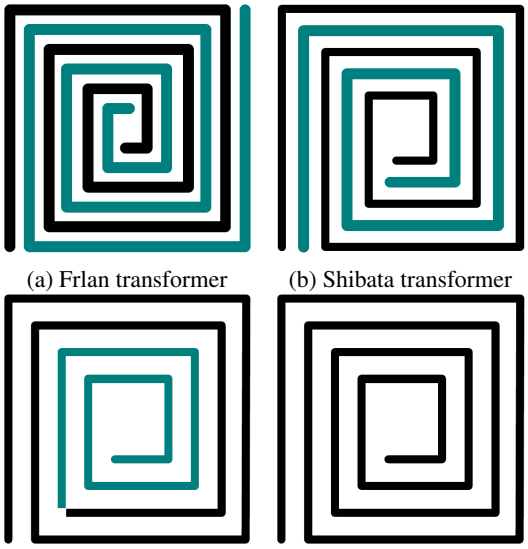
Figure 3: Transformer mounted on board with interconnections bondings

Table I: Specifications

Switching frequency f_{SW}	1 MHz
Isolation capacitance C_{ISO}	≤ 10 pF
Temperature range	$-55°C \leq T \leq 200°C$
Magnetization inductance L_M	3 µH
Winding ratio n	1:1
Input voltage V_{in}	9 V
DC winding resistance	≤ 300 mΩ
Power P	500 mW
Area A	1 cm^2

imposed by the manufacturing process described in the previous section.

Regarding the winding pattern, several configurations are possible: interleaved (Fig. 4a and 4b), tapped (Fig. 4c), or stacked (Fig. 4d). The performances of this latter configuration may be interesting, but the manufacturing process is more complex (one additional insulating layer and one more copper layer are required), so it will not be discussed further.



(a) Frlan transformer (b) Shibata transformer

(c) Tapped transformer (d) Stacked transformer

Figure 4: Planar transformer structures [7, p. 16]

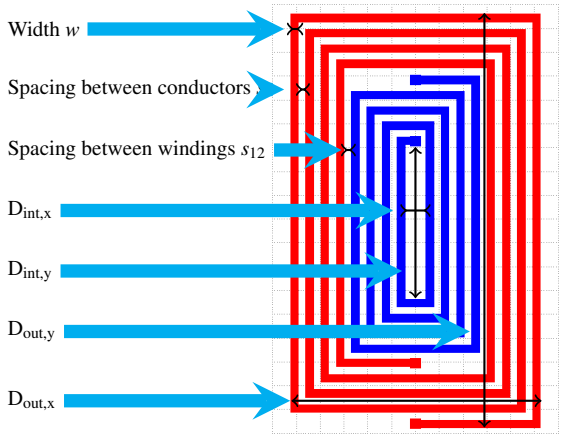


Figure 5: Tapped transformer

Table II: Geometrical parameters of the transformer

Conductor width	w	160	µm
Spacing between conductors	s	160	µm
Spacing between windings	s_{12}	160	µm
Conductor thickness	t_{CU}	60	µm
Magnetic substrate thickness	t_{MAG}	1	mm
Dielectric thickness	t_{ISO}	2	[µm
Internal diameter	$D_{INT,X}$	440	µm
Internal diameter	$D_{INT,Y}$	3240	µm
External diameter	$D_{OUT,X}$	5240	µm
External diameter	$D_{OUT,Y}$	8680	µm
Number of turns	N	4	

A. *Transformer description*

The geometrical parameters are described in Fig. 5 for tapped transformer. These parameters include the number of turns N, the spacing between turns s and between windings s_{12} (tapped transformer only).

As the analytical expressions used further are based on a square geometry, we introduce three additional parameters, calculated as the geometric mean of the X-axis and Y-axis lengths:

The inner diameter d_{INT} is expressed in equation (1) and depends on $D_{INT,X}$ and $D_{INT,Y}$.

$$d_{INT} = \sqrt{(d_{INT,X} d_{INT,Y})} \tag{1}$$

The outer diameter d_{OUT} is expressed in equation (2) and depends on $D_{OUT,X}$ and $D_{OUT,Y}$.

$$d_{OUT} = \sqrt{(d_{OUT,X} d_{OUT,Y})} \tag{2}$$

The average diameter d_{AVG} is expressed in equation (3) and depends on (1) and (2).

$$d_{AVG} = \frac{d_{INT} + d_{OUT}}{2} \tag{3}$$

The transformer's overall dimensions (corresponding to the transformer depicted in Fig. 2 and the geometric parameters are detailed table II.

Table III: Coefficients for a square inductor used in (4)

β	α_1 (d_{OUT})	α_2 (w)	α_3 (d_{AVG})	α_4 (N)	α_5 (s)
1.62×10^{-3}	-1.12	-0.147	2.40	1.78	-0.030

Table IV: Self-inductances values measured and calculated using analytic and numeric models.

	Measurement	Analytic		FEA	
	Value	Value	Error	Value	Error
Interleaved transformer					
L_1 [nH]	171	156.6	8.4%	174.7	2.2%
L_2 [nH]	132	115	12.9%	134.3	1.8%
Tapped transformer					
L_1 [nH]	327	338	3.3%	310	5.2%
L_2 [nH]	109	107.8	1.1%	137.3	26%
with U-shaped core					
L_1 [nH]	1669	3168	-90%	2755	65%
L_2 [nH]	591	1728	-93%	1023	73%

B. Analytical expressions

1) Inductance: Regarding the self-inductances, two cases must be considered, depending if the magnetic circuit is open or closed (i.e. if the cap is placed on top of the substrate or not). In the first case, accurate analytical expression of inductances can be found in [8]. Mohan introduces the following empiric formula mentioned in equation (4). For a square (air) inductor, coefficients α_1 to α_5 are mentioned in table III and are detailed in [9, p. 72].

$$L_0 = \beta d_{\mathrm{OUT}}^{\alpha_1} w^{\alpha_2} d_{\mathrm{AVG}}^{\alpha_3} N^{\alpha_4} s^{\alpha_5} \tag{4}$$

Earlier work by Roshen and Turcotte [10] shows that the relationship between an air-core inductor L_0 and an inductor on magnetic substrate L can be expressed as :

$$L = \frac{2\mu_r}{\mu_r + 1} L_0 \tag{5}$$

In fact, this depends on the magnetic substrate thickness and its relative permeability. With a 1 mm-thick substrate having a relative permeability μ_r of 900, L is basically doubled compared to the air inductor L_0 [11, p. 273].

Self-inductances values calculated by combining equations (4) and (5) are given in table IV.

Regarding the transformers with a closed magnetic circuit, analytical expressions of the self-inductance are based on reluctance equivalent circuits to take into account the presence of air gaps (an air gap is present between the substrate and the cap on the center of the inductor). This calculation is not detailed here for the sake of brevity.

2) Isolation capacitance: In gate driver applications, the transformers can be exposed to large voltage transients (in excess of $10\,\mathrm{kV/\mu s}$. As a consequence, they must present a low inter-winding (isolation) capacitance to limit parasitic currents.

The calculation of the isolation capacitance is based on the assumption that the electrostatic energy is located inside the silicon dioxide layer. Therefore, its value is almost independent from the U-shaped cap used to close magnetic circuits.

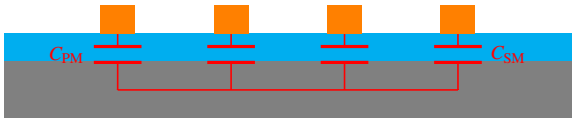


Figure 6: Simplified representation of transformer's isolation capacitance

Table V: Isolation capacitance results

	Measurement	Analytic		FEA	
	Value	Value	Error	Value	Error
C_{ISO}[pF]	88	79,6	$< 9,5\%$	88.2	$< 1\%$

The localization of the capacitance is depicted in Fig. 6. An equivalent capacitor called isolation capacitor C_{ISO} corresponds to the series association of two capacitors: C_{PM} (the capacitor between the primary winding, with a surface area A_{PM}, and the magnetic substrate) and C_{SM} (the capacitor between the secondary winding, with a surface area A_{SM}, and the magnetic substrate).

Therefore, assuming that the electric field is uniform, the isolation capacitance C_{ISO} can be expressed as:

$$C_{\mathrm{ISO}} = \frac{\varepsilon_0 \varepsilon_R}{e} \left(\frac{A_{\mathrm{PM}} A_{\mathrm{SM}}}{A_{\mathrm{PM}} + A_{\mathrm{SM}}} \right) \tag{6}$$

With e the thickness and ε_R the dielectric constant of SiO_2. The isolation capacitance values based on equation (6) are given in table V.

C. Finite elements design

In parallel with the analytic approach, the transformers were simulated using a finite elements analysis (FEA) software (Maxwell 3D from Ansys Electromagnetics Suite). The simulated transformer is represented in Fig. 7.

The transformer is simulated in a domain thrice the size of the longest edge of the transformer. The boundary condition is homogeneous Dirichlet i.e. zero-field conditions outside the resolution domain. Windings are excited by current during magnetostatic simulation (for inductance calculations) and voltage during electrostatic simulation (for insulation capacitance calculations).

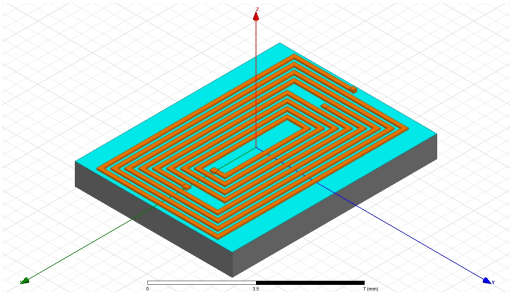


Figure 7: Simulated transformer (trimetric view)

Table VI: Material properties

	Copper	3F45	SiO_2
Relative permeability μ_r	1	900	1
Dielectric constant ε_R	1	8853	4
Electrical conductivity σ [$S\,m^{-1}$]	4.9×10^7	0.1	0

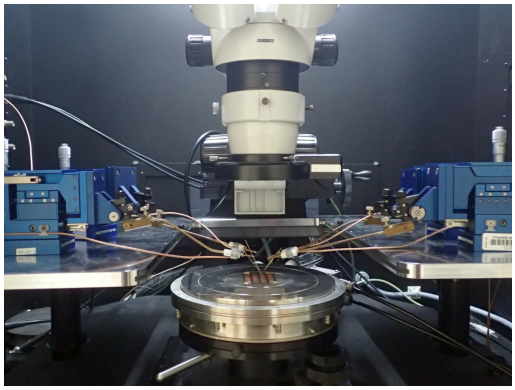


Figure 8: Test bench with device under test

Materials properties are given table VI, and the results are given in tables IV and V

IV. Characterization

A. Characterization apparatus

A small signal AC characterization of the transformers is performed before dicing the substrate, using a probe station (Fig. 8) and a Keysight 4294A impedance analyzer.

After compensation of the cabling parasitics, impedance is measured over the 10 kHz to 110 MHz frequency range.

B. Self-inductances

The self-inductance of a winding is extracted by measuring the impedance of that winding, while the other winding is left open (un-connected).

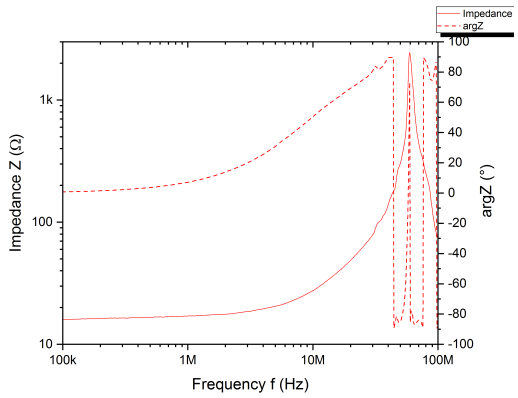
$$\begin{cases} L_S = \dfrac{\mathbf{Im}\,Z_S}{2\pi f} \\ R_S = \mathbf{Re}\,Z_S \end{cases} \tag{7}$$

Fig. 9a and 10a show an inductive behaviour up to 40 MHz. Obtained values from Fig. 9b and 10b are 327 nH and 109 nH for primary winding and secondary winding self-inductance respectively (table IV).

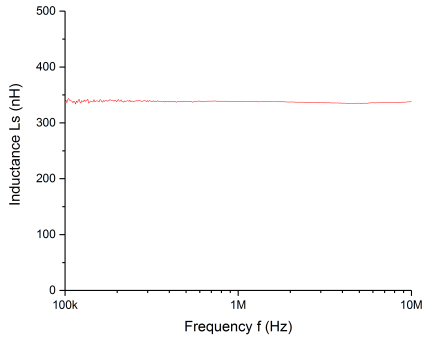
C. Isolation capacitance

Here, the impedance is measured between one terminal of the primary and one terminal of the secondary windings. This impedance is then expressed as a series resistance capacity circuit (equation (8)).

$$\begin{cases} C_S = -\dfrac{1}{2\pi f\,\mathbf{Im}\,Z_S} \\ R_S = \mathbf{Re}\,Z_S \end{cases} \tag{8}$$



(a) Primary winding impedance (modulus and argument)



(b) Self-inductance of primary winding

Figure 9: Primary winding impedance for the tapped design

This can be converted into parallel RC circuit [12, p. 692], which better represents the isolation capacitance and resistance between primary and secondary windings:

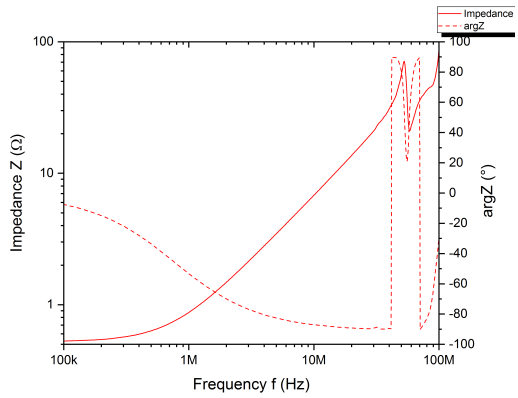
$$\begin{cases} C_{ISO} = C_S \dfrac{1}{1+\dfrac{1}{Q_S^2}} \quad \text{with} \quad Q_S = \dfrac{\mathbf{Im}\,Z_S}{\mathbf{Re}\,Z_S} \\ R_F = R_S\left(1+Q_S^2\right) \end{cases} \tag{9}$$

Up to 30 MHz, Fig. 11a shows a negative slope typical of a capacitive behaviour. Fig. 11b value is close to equation (6).

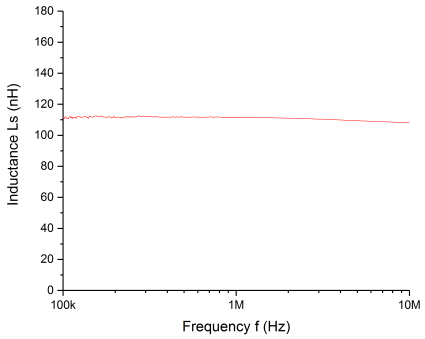
V. Conclusions

A new method to manufacture integrated transformers has been presented, along with models and experimental results.

A good correlation is found between analytical methods, FEA design and characterization. For closed circuit magnetic transformers, correlation between analytical method and FEA design has to be improved.Replacing the U-shaped cap with a E-shaped cap would remove the center air gap, improve coupling between primary and secondary windings, and probably result in closer analytical and FEA results. Regarding the electrostatic aspects, analytical methods are efficient enough to allow to skip the FEA modeling. They show that the current insulation capacitance is approximately one order of magnitude too high

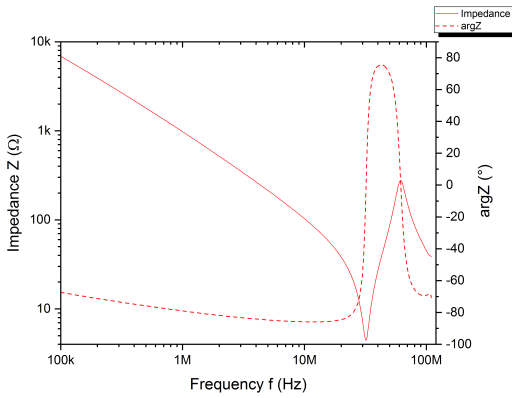


(a) Secondary winding impedance (modulus and argument)

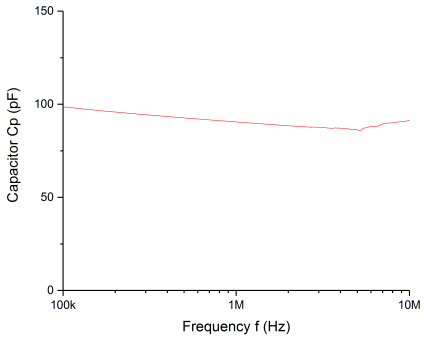


(b) Self-inductance of secondary winding

Figure 10: Secondary winding impedance



(a) Interwinding impedance (modulus and argument)



(b) Isolation capacitance

Figure 11: Interwinding capacitance

compared to the specifications (hundreds of pF vs. tens of pF). The analytical expression shown in equation (6) highlights some degree of freedom to reduce the capacitor value: use a thicker SiO_2 layer, replace SiO_2 with a lower permittivity material, or reduce the surface area of the windings.

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