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Wet oxidation of nitride layer implanted with low-energy Si ions for improved oxide-nitride-oxide memory stacks

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An alternative method for the formation of the top oxide in oxide-nitride-oxide dielectric stacks is proposed. This method combines low-energy (1 keV) silicon ion implantation into a thin nitride-oxide stack and subsequent low-temperature wet oxidation (850 °C for 15 min). Transmission electron microscopy shows that for an implanted dose of 1.5×10^{16} Si cm⁻², an 8-nm-thick silicon oxide layer develops on the surface of the nitride-oxide stack. Time of flight secondary ion mass spectrometry reveals: (1) transformation of the implanted silicon nitride to an oxygen-rich-silicon nitride layer and (2) pilling up of nitrogen atoms at the bottom silicon/oxide-substrate interface. The resulting oxide-nitride-oxide stack exhibits strong charge storage effects and excellent charge retention properties leading to a 1.5 V, 10 yr extrapolated memory window at 125 °C. These results suggest that the proposed fabrication route may lead to gate dielectric stacks of substantial potential impact for mainstream nitride-based memory devices.

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Nitride-based memory technology has the potential to fulfill the stringent requirements of nonvolatile memory cell downsizing.¹ This technology exploits the presence of discrete charge storage nodes in the form of deep traps distributed in nitride materials. Due to its promising in terms of scalability, the conventional polycrystalline silicon/oxide/nitride/oxide/silicon memory cell has regained a lot of attention nowadays.^{2,3}

Typical fabrication of the oxide/nitride/oxide (ONO) stack consists in the growth of a thin SiO₂ layer on a Si substrate and subsequent deposition of a Si₃N₄ layer. The top silicon oxide is obtained by either deposition techniques or high temperature wet oxidation^{4,5} of the Si₃N₄ layer. The latter approach has two main advantages. First, a thermal top oxide exhibits better insulating properties compared to a deposited oxide. Second, during the oxidation step a silicon oxynitride transition layer forms between the top oxide and the remaining silicon nitride, containing a high density of traps. This layer can efficiently accommodate a larger proportion of trapped carriers as compared to that of stoichiometric or Si-rich nitride.⁶ However, fabrication of functional thermal blocking oxides requires high oxidation temperatures (typically within the 1000 °C range⁷). For deep-submicron integration purposes, it is important to explore alternative technological routes that could lead to the formation of a thermal top oxide at lower oxidation temperatures.

In this work a method for the formation of the top oxide in ONO stacks is proposed. This method is based on low-energy Si ion implantation into oxide-nitride (ON) structures followed by low-temperature wet oxidation. The structural and chemical properties as well as the memory performance

of the resulting ONO stacks are reported and compared to those of unimplanted ONO stacks.

SiO₂ and Si₃N₄ stacks were first formed on a 4 in. *n*-type (100) Si wafer. The oxide layer (referred as tunnel or bottom oxide) was grown by dry oxidation at 850 °C to a thickness of 2.8 nm. The Si₃N₄ layer 6 nm thick was deposited by low-pressure chemical vapor deposition (LPCVD) at 800 °C using a mixture of dichlorosilane (SiH₂Cl₂) and ammonia gasses (NH₃). Subsequently, the wafer was cut in to four pieces referred hereafter as samples II and C1–C3. Sample II was implanted with 1 keV Si ions to a dose of 1.5×10^{16} cm⁻². Si implantation using accelerating energy as low as 1 keV allows for the introduction of Si atoms with a distribution confined in the nitride layer. Monte Carlo simulations using the TRIM code and energy-filtered transmission electron microscopy (TEM) analysis of high-temperature thermally annealed samples in N₂, indicate that the peak of the implanted profile is about 2.2 nm from the Si₃N₄ surface.⁸ In addition to Si enrichment of the implanted nitride materials, the implantation process produces a variety of defects such as vacancies, recoil N and Si atoms, and broken bonds that increase the density of reaction sites and thereby reduce the activation energy for oxidation. TRIM depth distributions of vacancies and recoil atoms exhibit a projected range of about 1.6 nm from the free nitride interface with tails extending up to the middle region of the tunnel oxide. While TRIM information on ion and defect distributions should be cautiously considered, especially in the case of low-energy high-dose ion implantation into thin dielectrics where a number of parameters^{9,10} (e.g., ion beam mixing, surface sputtering, and target swelling) contribute to the physicochemical changes of the target, one can assumed that the implantation process affects both the nitride layer and part of the tunnel oxide of sample II. Following the

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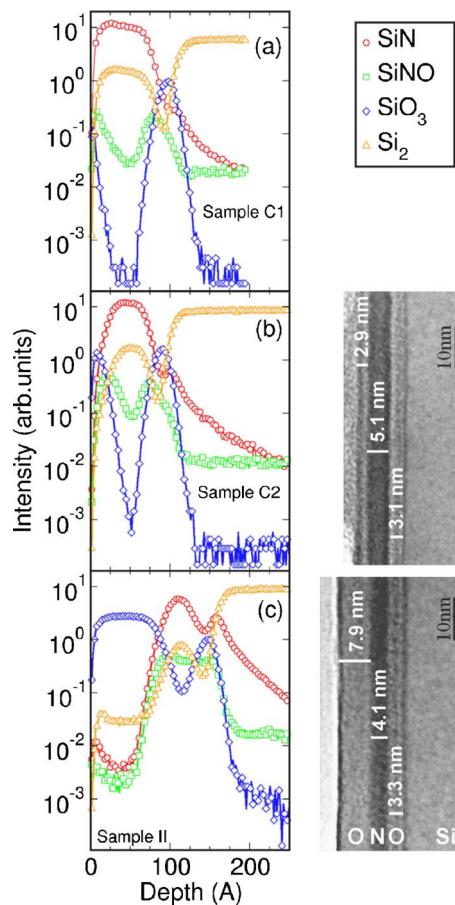


FIG. 1. (Color online) ToF-SIMS depth profiles of (a) unoxidized (sample C1), (b) wet oxidized (sample C2), and (c) Si implanted and wet oxidized (sample II) ON stacks. Defocused bright field cross-sectional TEM images are shown for samples C2 and II.

implantation step, sample II was thermally oxidized in wet ambient at 850 °C for 15 min to produce the top control oxide and further thermally annealed at 950 °C in N₂. The three control samples C1–C3 start with the non-Si-implanted ON stacks. Samples C1 and C2 consist of the dielectric stacks produced without and with the above wet oxidation step, respectively. Sample C3 refers to ONO stacks with 8-nm-thick top oxide produced by LPCVD at 700 °C using tetraethylorthosilane and subsequently, thermally annealed at 950 °C in N₂. The structural and chemical characteristics of the produced ONO stacks were investigated by TEM and time of flight secondary ion mass spectroscopy (ToF-SIMS). Finally, generic metal-ONO-semiconductor (MONOS) Al gate capacitors were fabricated to study the electrical properties and memory performance of the ONO stacks.

The effect of wet oxidation on the control and implanted ON structures was examined by cross-sectional TEM in defocused bright field conditions. The method for distance measurements on such images is given in Ref. 9, with error bars of ± 0.5 nm. Wet oxidation of the control sample C2 forms a thin oxide layer (mean thickness of 2.9 nm) on top of the nitride layer, while the remaining nitride mean thickness is 5.1 nm [see Fig. 1(b)] and the thickness of the bottom oxide is around 3.1 nm. The ONO stack of sample C2 exhibits almost identical tunnel and top oxide thicknesses. On the contrary, the Si implanted and wet oxidized ON structure (sample II) [Fig. 1(c)] presents an 8-nm-thick oxide on top of the remaining nitride layer (4.1 nm thick) and a bottom oxide

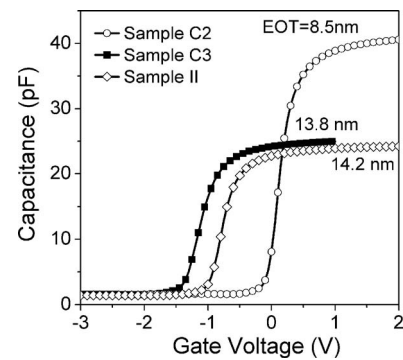


FIG. 2. Typical high-frequency C - V characteristics of MONOS capacitors from samples C2, C3, and II.

with a mean thickness of 3.3 nm. In addition, the interface of the top oxide with the nitride layer is flat and parallel to the bottom oxide-substrate interface indicating that the oxidation front is uniform.

Depth profile chemical compositions of the samples were obtained by ToF-SIMS. Sputtering was performed by Cs⁺ ions at 0.5 keV energy and 34 nA beam current. The analysis was made in negative polarity, using Ga⁺ at 25 keV energy and a current of 1.1 pA. Figure 1 shows the signals of the SiN, SiON, SiO₃, and Si₂ secondary ions. These signals are related to the presence of Si nitride (SiN and Si₂), silicon dioxide (SiO₃), and silicon oxynitride (SiON, SiN). Depth scale calibration was performed using a SiO₂ film of known thickness as a reference and assuming a constant sputter velocity throughout the ONO stack. The extracted layer thicknesses are in agreement with TEM analysis. In the case of the unoxidized ON stack (C1), [Fig. 1(a)], the presence of a double layer structure is detected. For the oxidized ON sample (C2) [Fig. 1(b)], the SiO₃ and SiON signals reveal a surface oxide layer on top of the remaining nitride.

In the case of sample II [Fig. 1(c)], SiO₃ signal shows the formation of a thick silicon oxide layer. In comparison to sample C2, the SiON signal intensity is higher in the bulk of the nitride layer and extends down to the Si substrate. This indicates non-negligible oxygen content in the remaining nitride layer and the presence of nitrogen within the tunnel oxide. Moreover, in sample II, the SiN signal exhibits an intense peak at the tunnel oxide/Si-substrate interface with a long tail extending into the Si substrate. The tail is due to a well-known artifact related to mixing phenomena occurring during the sputtering process. The peak at the tunnel oxide/Si-substrate interface indicates migration of nitrogen atoms toward the Si substrate during the implantation and oxidation processes.

Figure 2 shows typical high-frequency (1 MHz) C - V characteristics of the ONO structures under study. The measurements were performed in the low-field regime to avoid charge injection and trapping effects. The extracted equivalent oxide thickness of samples II and C2, 14.2 and 8.5 nm, respectively, confirm TEM and ToF-SIMS results regarding the enhanced oxidation of Si-implanted ON stack. Compared to sample C3, the flatband voltages (V_{FB}) of samples C2 and II are about 1.0 and 0.3 V shifted to more positive values, respectively. These results are not only in accordance with the previous observations¹¹ indicating that oxidation of nitride layer induces a positive shift of V_{FB} but also reveal that the latter effect is reduced for oxidized Si-implanted nitride

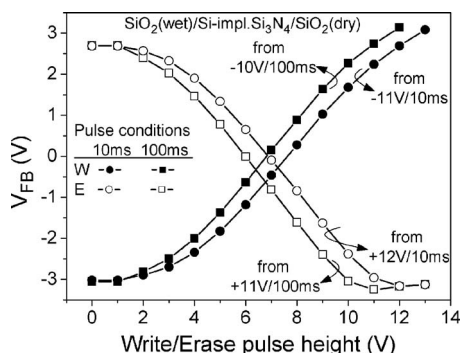


FIG. 3. Write/erase characteristics of Si-implanted-nitride ONO capacitors (sample II) for 10 and 100 ms pulse duration.

material. In our case, the origin of this effect is probably due to negatively charged defects such as the nitrogen vacancy with attached hydrogen atom.¹²

Memory performance of sample II MONOS devices under write/erase pulsed operation is shown in Fig. 3. Single write (positive) and erase (negative) pulses were applied after setting the devices in near-saturation erase and write states, respectively. Clear saturation is detected in the 10 and 100 ms erasing regimes. It is believed that such saturation arises from the competitive effects of substrate hole injection and gate electron injection. Memory windows as large as 5.7 V can be obtained for 100 ms, +11/−10 V and 10 ms, +12/−11 V write/erase pulses, respectively. It should be mentioned that the ONO stack with deposited top oxide (sample C3) exhibits no hole injection under erasing conditions and smaller V_{FB} shifts in the write regime (e.g., 4.1 V for 100 ms +11 V). The absence of hole injection for sample C3 is due to the thick bottom dry oxide used in the present experiments. While the bottom oxide of sample II presents a larger physical thickness, its modified chemical composition allows for efficient erase operation.

Figure 4 shows charge retention characteristics of sample II MONOS devices at 30 and 125 °C. The capacitors were initially charged using 100 ms, −10 and +11 V pulses for the erase and write states, respectively. The flatband voltage was monitored for waiting times as large as 10^5 s. The extracted charge (electron) loss rate for the write state was 0.23 V/decade at 30 °C and 0.29 V/decade at 125 °C. In the case of the erase state, charge loss rates of 0.24 and 0.29 V/decade were found at 30 and 125 °C, respectively. Long time extrapolation indicates 10 yr memory windows of about 3 and 1.5 V at 30 and 125 °C, respectively.

In summary, it has been presented that a combination of low-energy silicon ion implantation into ON structures and

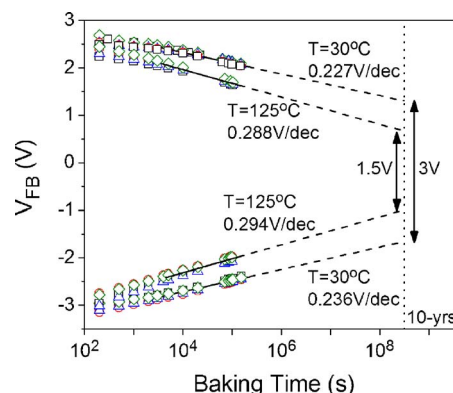


FIG. 4. (Color online) Charge retention characteristics of Si-implanted-nitride ONO capacitors (sample II) at 30 and 125 °C.

subsequent low-temperature wet oxidation provides an attractive technological route for the fabrication of ONO dielectric stacks. Such a route produces thick and reliable top oxides as well as transforms the nitride layer to silicon oxynitride materials. Both the write/erase and data retention characteristics obtained throughout the measurements performed so far suggest that the ONO stacks reported herein are attractive for the development of nitride storage memory cells.

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