Interface Circuit for Vibration Energy Harvesting with Adjustable Bias Voltage

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Abstract. This paper presents a new interface circuit for electrostatic vibration energy harvesting with adjustable bias voltage. An electronic switch is used to modify the circuit configuration so that the harvested energy increases the voltage across a biasing capacitor. Decrease of this biasing capacitor voltage occurs naturally due to the circuit imperfections. Such a control of the bias voltage enables to adjust the amount of energy converted by the variable capacitor on each cycle. This feature can be used to optimize the mechanical damping induced by the energy conversion process in order to maximize the harvested power. Another feature of this interface circuit is that it is capable to get high bias voltage whatever the battery voltage with low energy loss.

1. Introduction

Energy harvesting is a promising way of generation of electrical supply for powering miniature device, like those used in wearable electronics, medical implants and wireless sensor networks. Mechanical vibration is a common and well known energy source. Mechanical vibration energy harvesting concept consists in converting the energy of the parasitic ambient mechanical vibration into the useful electrical energy. Among several types of Vibration Energy Harvester (VEH), such as electromagnetic, piezoelectric, electrostatic, etc, Electrostatic Vibration Energy Harvesters (e-VEH) appears to be promising for miniaturization.

An e-VEH is actually based on a variable capacitor whose moving electrode is actuated by ambient vibrations. Such electromechanical device can be profitably miniaturized using MEMS technology. One of the main challenges of e-VEH implementation is the design of the interface circuit, whose power efficiency is a critical issue. Recently, several interface circuits without switches and inductive components have been proposed [1-4], whose simplicity enables efficient standalone implementation.

However, as shown by Dhorziev et al., these circuits do not intrinsically optimize the system performances: there exists an optimal power supply voltage at which output power is maximum [5]. Such optimization can be performed using Yen's circuit [6], but in a limited way because of the limited achievable voltage range.

The interface circuit presented here can theoretically generate voltages across the variable capacitor without upper limit, enabling to get high bias voltages whatever the battery voltage. Dragunov et al.

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[2] and De Queiroz [3] previously proposed interface circuits able to generate high bias voltage. However, their circuits include zener diodes as voltage stabilizer, which induce significant energy losses and lead to very poor efficiency. Contrary to those circuits, the proposed circuit has very high power efficiency. Moreover, its adjustable bias voltages can be used for real-time optimization of the harvested power, respectively with the variations of the ambient vibration characteristics.

2. Theoretical analysis of the proposed interface circuit

The new interface circuit for e-VEHs, shown in Figure 1, was derived from our previous work [4]. It is composed of biasing capacitor C_{bias}, a diode rectifier (D1and D2), an electronic switch SW and a multiplier circuit which consist of capacitors C1 and C2, and diodes D3, D4, D5. The input of the circuit is connected to the mechanically-actuated variable capacitor C_{var}, and the generated energy is stored in a rechargeable battery with V_{DC} voltage, which could be replaced by a capacitor or a supercapacitor.

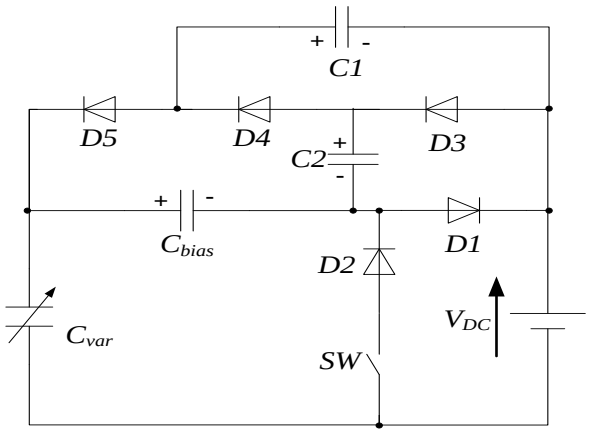

Figure 1. Schematic diagram of the proposed interface circuit

The operation of the circuit can be divided into two different modes. SW open: the variable capacitor is used for charging the biasing capacitor C_{bias}. SW closed: the variable capacitor is used for charging the battery. The following analysis is made assuming a steady variation of the capacitance C_{var} between a maximum value C_{max} and a minimum value C_{min}. Imperfections of the components are neglected.

2.1. SW open: charging of the biasing capacitor

Due to the diodes D3, D4 and D5, the variable capacitor is initially charged to voltage V_{DC}. When C_{var} decreases, the diodes D1 and D4 are conducting and the biasing capacitor is charged. The capacitors C1 and C2 are charged via the diode D4. The charging process ends when C_{var} reaches its minimum. Then, C_{var} increases and the diodes D1 and D5 become conducting. An electric current flows from the battery to C_{var} via D1 and C1. When C_{var} gets to its maximum, the voltage across C_{var} is greater than V_{DC} due to the previously charged C1. These different steps are repeated during the periodic variation of C_{var}, and the voltage across C_{bias} is progressively increased.

The charge-voltage diagram of the variable capacitor is shown in Figure 2. The diagram begins at point 1 with C1, C2 and C_{bias} initially discharged. The first QV cycle passes successfully at points 1, 2, 3, 4 and the second cycle passes at points 4, 5, 6, 7, 8 etc. The increase of the voltage across C_{bias} is represented by 4 to 5, 8 to 9 etc. At the end of each cycle, the charge Q of the variable capacitor increases. Hence, when the switch SW is open, the circuit may theoretically generate voltage values across the variable capacitor without upper limit.

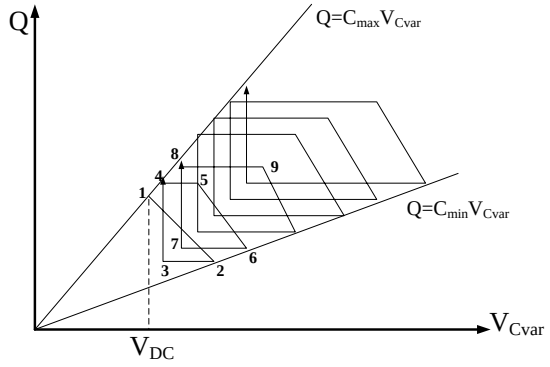

Figure 2. Theoretical charge-voltage diagram of the variable capacitor for the proposed circuit with SW opened

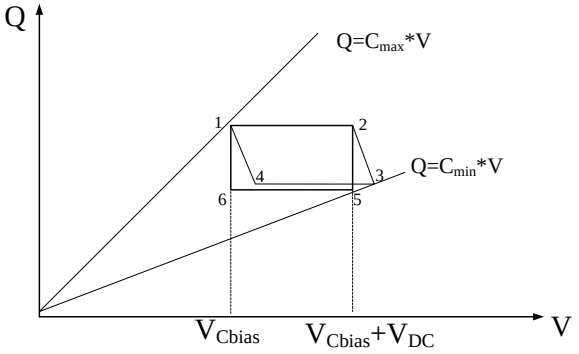

Figure 3. Theoretical charge-voltage diagram of the variable capacitor for the proposed circuit with SW closed

2.2. SW closed: charging of the battery

The charging of the battery may occur when SW is closed. In steady state operation, the voltage V_{Cbias} across the capacitor $C_{bias}$is greater or equal to $2*V_{DC}$. If V_{Cbias} is smaller than $2*V_{DC}$ and SW is closed, the charging of C_{bias} continues until V_{Cbias} reaches $2*V_{DC}$ and then the charging of the battery begins.

The charge-voltage diagram of the proposed circuit is shown in Figure 3. Due to D2, the voltage across C_{var} is greater or equal to V_{Cbias}. Between points 1 and 2, all the diodes are blocking and the charge of the C_{var} keep constant. Between points 2 and 3, D1 is conducting, meanwhile an electric current flows from C_{var} to the battery through C_{bias}. Between points 4 and 1, D2 is conducting, meanwhile an electric current flows from C_{bias} to C_{var}. Hence, the energy conversion cycles pass successively at points 1, 2, 3, 4 and 1. Assuming that the voltage variation C_{bias} is negligible, which is the case if $C_{bias}>>C_{var}$, the charge-voltage diagram tends to the rectangle passing at points 1-2-5-6. In this case, the harvested energy per cycle, with SW closed, can be expressed as (1).

$$W = V_{DC}V_{Cbias}C_{min}\left[\frac{C_{max}}{C_{min}} - \left(1 + \frac{V_{DC}}{V_{Cbias}}\right)\right] \qquad (1)$$

This equation shows that the minimum value of the capacitance ratio C_{max}/C_{min} for which energy can be harvested tends to 1 for high values of V_{Cbias}. Our previous circuits with multicell voltage multiplier enabled also to reduce the limit of the capacitor ration C_{max}/C_{min}. However, the number of cells of the multiplier determined a fixed ratio between V_{Cbias} and V_{DC}, making thus impossible to adjust continuously and independently V_{Cbias}. More precisely, the voltage across the variable capacitor of previous circuit varied between $N*V_{DC}$ and $(N+1)*V_{DC}$ with a N-cell multiplier, as depicted in Figure 4. It did not intrinsically optimize the system performances: previous works [5] showed that there exits an optimal power supply voltage at which output power is maximum. The proposed circuit enables to solve this problem. Since V_{Cbias} can be adjusted to any value greater than $2V_{DC}$, the e-VEH can be operated under an optimal bias voltage by controlling the switch SW.

One should note that in practice, imperfections of the circuit components progressively decrease the voltage $V_{Cbias.}$ We experimentally observed exponential voltage decrease with time constant of a few minutes. Thus, in practice V_{Cbias} can be adjusted in both directions. If dynamic tuning of the voltage across C_{bias} requires faster decrease, this can be obtained by inducing extra losses in the circuit. For instance, we experimentally decreased the discharge time constant to a few tenths of seconds by adding a 5 GΩ resistor in parallel with Cbias, this without visible reduction of the circuit efficiency.

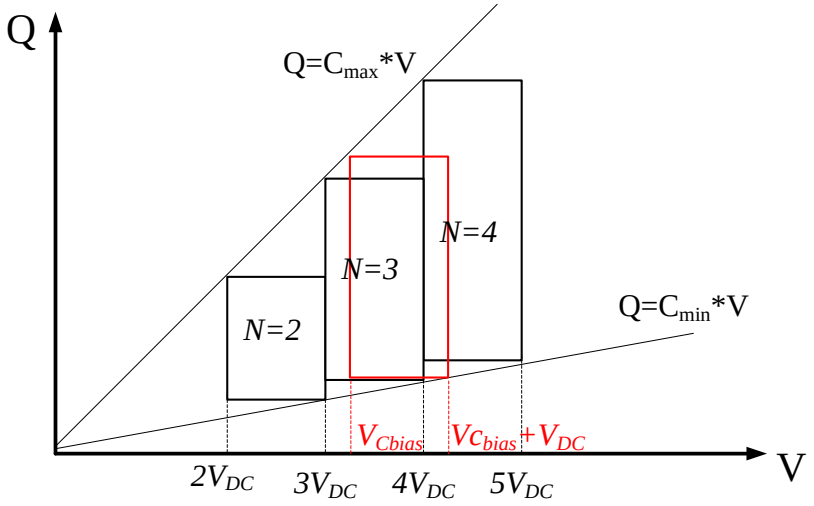

Figure 4. Charge-voltage diagram of the variable capacitor of the circuit using a multicell voltage multiplier (in black) and for the proposed circuit (in red)

3. Spice Simulation

To study the influence of the imperfection of electric components, the proposed circuit was modelled using LTSPICE software. The variable capacitor was varied from 25pF to 125 pF at 20 Hz frequency. The biasing capacitor was modelled by a 4.7 nF capacitor paralleled with a 2.10^{10} Ω resistor. The reverse current of the diodes was set to 10 pA and the forward drop voltage was set to 0.4 V. The ON and OFF states of the electronic switch SW were modelled by 1 Ω and 10^{10} Ω resistors respectively. The battery voltage V_{DC} was set to 5 V.

The circuit waveforms with periodic switching are shown in Figure 5. After 8 seconds initial charging of C_{bias}, SW was periodically turned ON and OFF with 8 s ON-time and 12 s OFF-time. One can clearly see that the output power is not null with SW closed, and that the power is increased when V_{Cbias} is larger. When SW is open, V_{Cbias} is increased. These simulation results confirmed the theoretical analysis of the proposed circuit. At the point where V_{Cbias}=25V, the simulated output power is 155 nW. This value represents 94% of the 165 nW theoretical power calculated using (1).

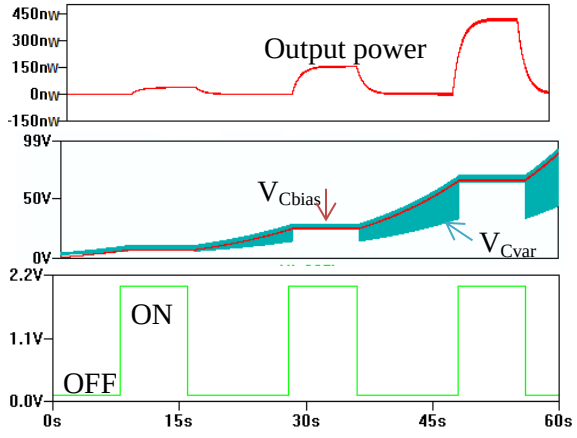

Figure 5. Simulated voltage of V_{Cbias} ,V_{Cvar} and power and SW control vs time

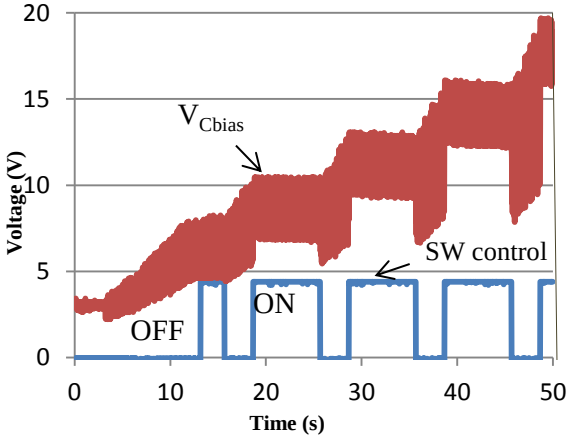

Figure 6. Experimental waveforms of V_{Cvar} and SW control signal vs time

4. Experimental results

The experimental validation was carried out using a rotating variable capacitor driven by a DC motor, with nearly 25 pF for C_{min} and 125 pF for C_{max}. The DC motor speed was 120 rpm, so the variable capacitor was varied at 20 Hz frequency. Low reverse current PAD5 diodes were used for *D1*, *D2* and *D3*. C_{bias} was a 4.7 nF capacitor. Due to the variable capacitor used, the generated power was not sufficient to power an electronic switch and its control electronics. Indeed, based on results presented by Dudka et al. [7], we estimated that the electronic switch and its integrated control circuit would consume about 1 µW. For this experiment, we emulated the electronic switch SW using an electromechanical relay controlled by a signal generator.

The experimental waveforms of the control signal of SW and V_{Cvar} voltage are shown in Figure 6. One can observe that these waveforms are quite similar to the simulation result of Figure 5 and confirm that the circuit operates as expected in both configurations.

5. Conclusion

This new interface circuit for electrostatic energy harvesters has a continuously adjustable bias voltage. It enables to generate high bias voltage whatever the battery voltage with very low energy loss. This degree of freedom can be used to optimize the mechanical damping induced by energy conversion process, in order to maximize the harvested power. Our future work will focus on the control principle and on the design of the integrated control circuit

6. Reference

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Acknowledgments

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