



# Power Aware Framework for Fast & Early Power Estimation on FPGA

Yehya Nasser, Jean-Christophe Prévotet, Maryline Hélard

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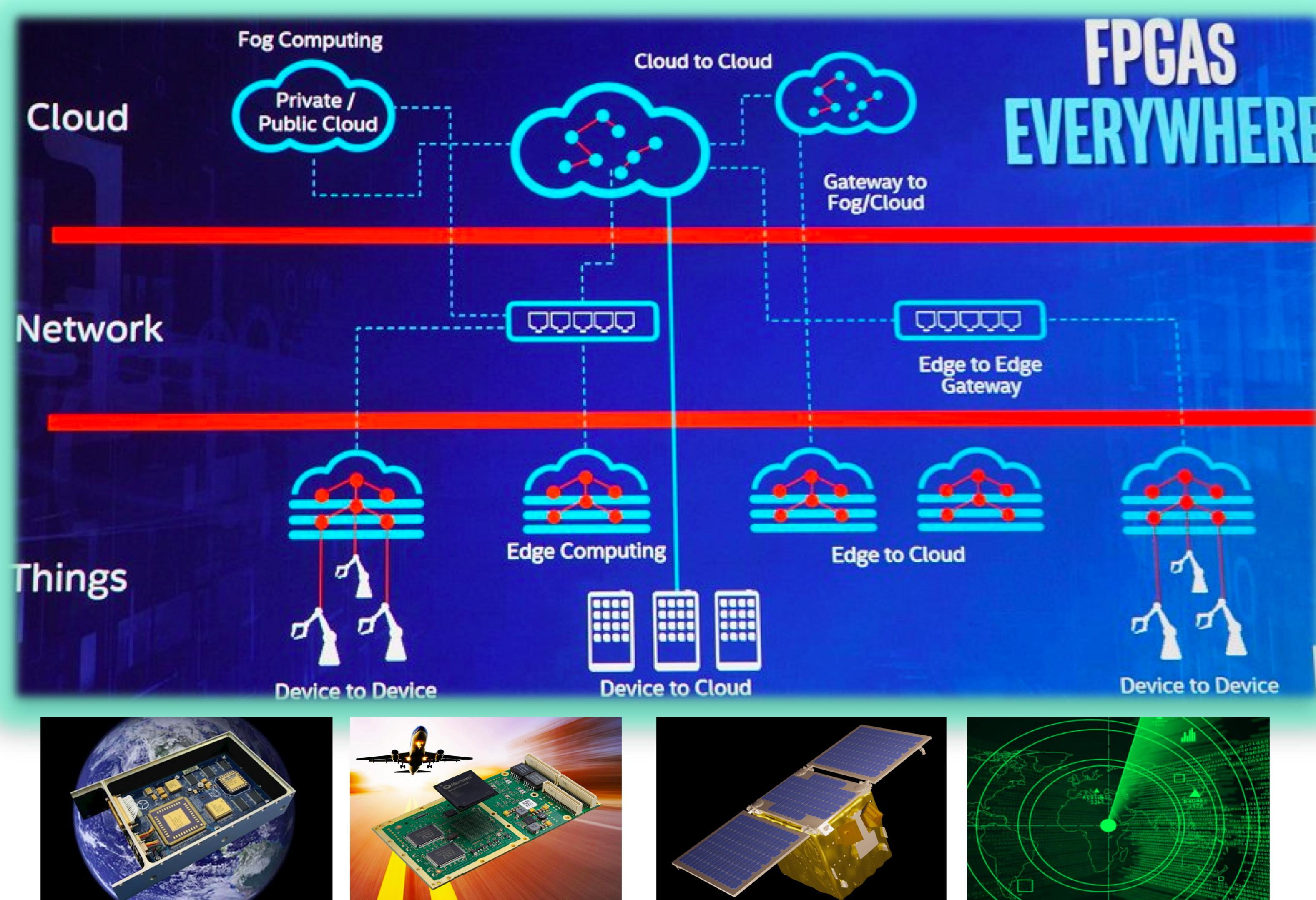
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## FPGA Advantages

- Faster Time To Market
- Field Reprogrammability
- Simpler Design Cycle
- More Predictable Project Cycle
- Reusability
- High-End Product
- Good processing speed
- No NRE (Non Recurring Expenses)



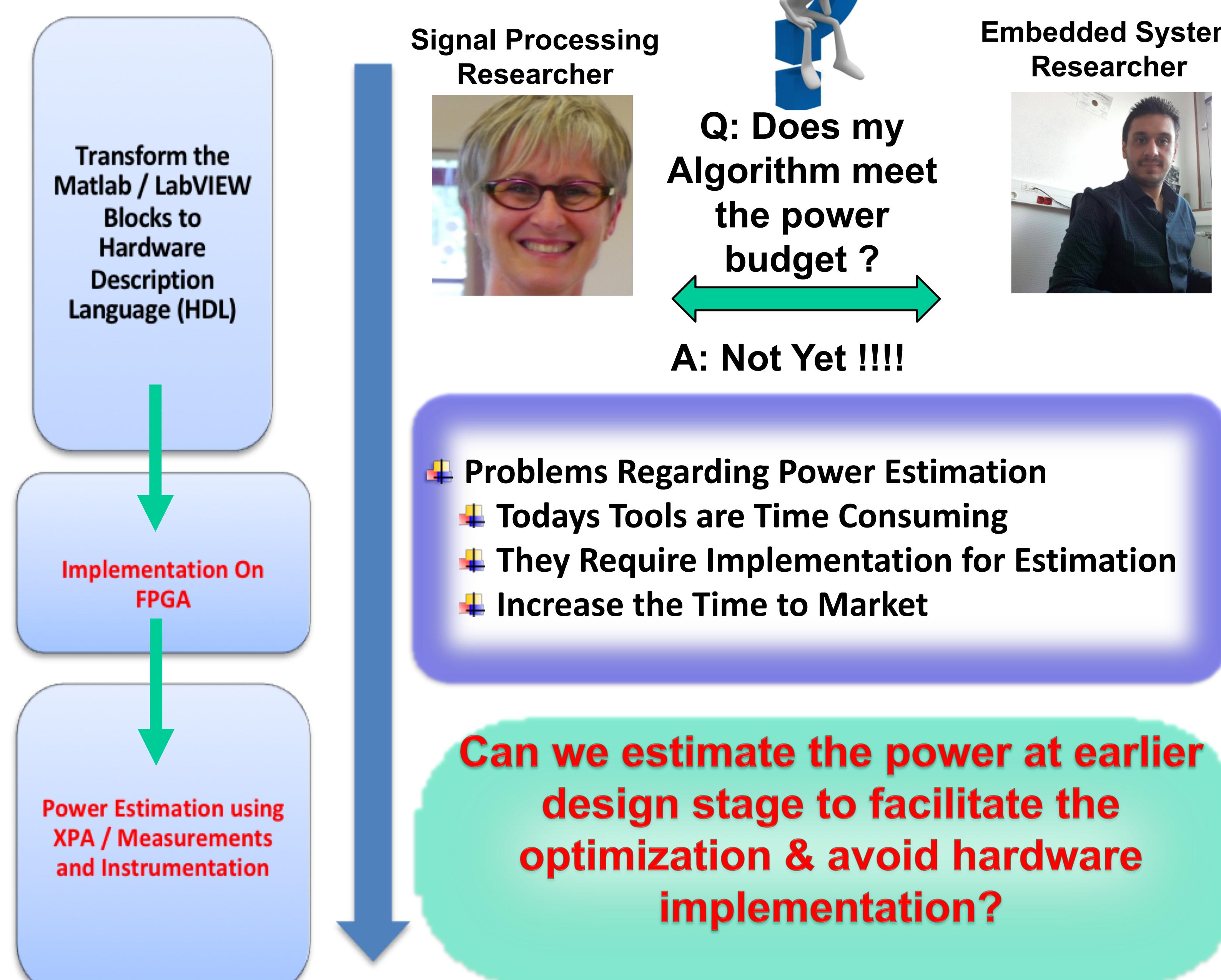
## FPGA Disadvantages

- High Power Consumption
- No Control on Power Optimization
- FPGA Limits The Design Size
- As Quantity Increases Cost Increases



## Problem Statement

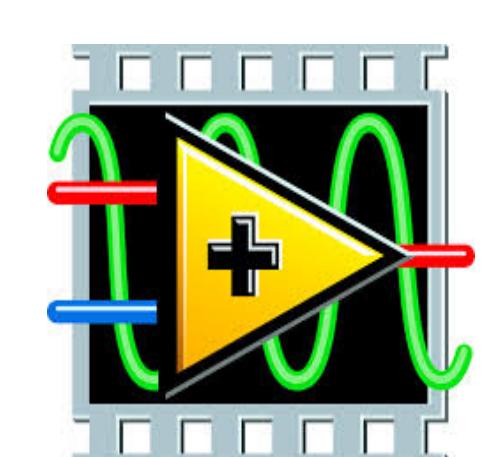
### Classical Flow



## Our Research Proposal

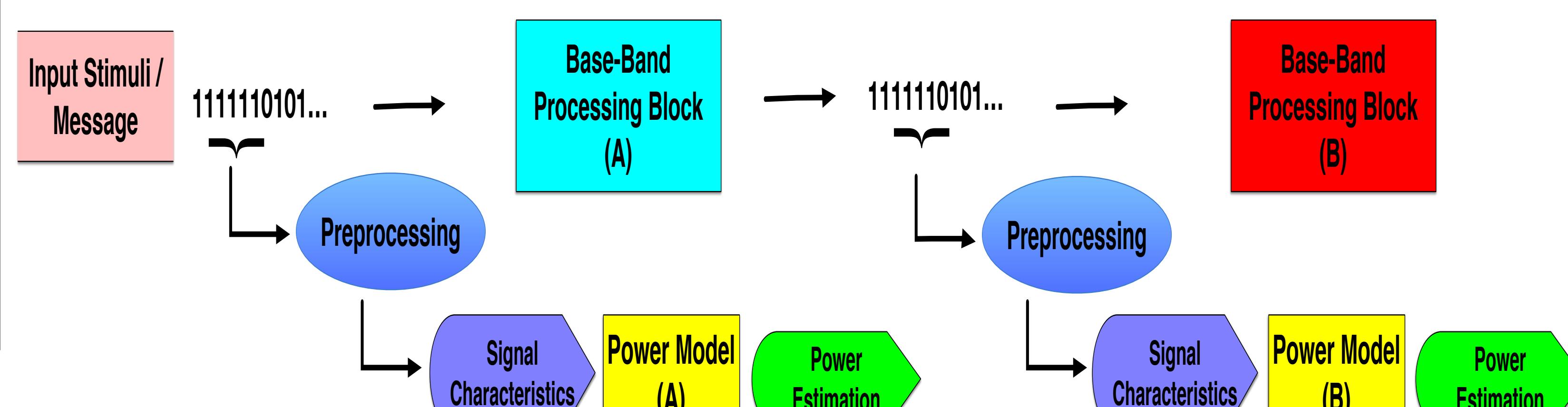
### Power Exploration Framework

Integrated In High Level Tools for POWER ESTIMATION



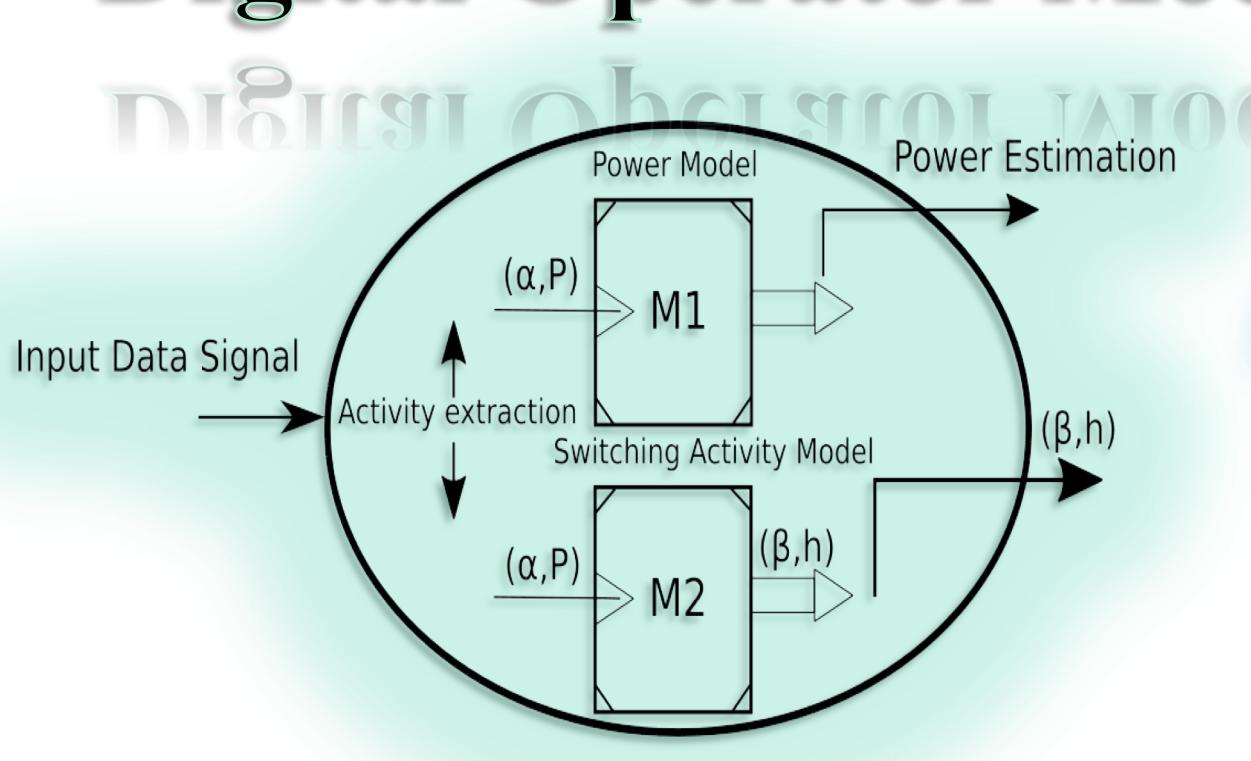
- Bottom up Approach
  - Low Level Power Characterization of an Operator on FPGA
  - Power Models to be Integrated in a Components Library
  - High Level Simulation for Power Estimation
  - Power Models Framework to Explore the Design Space

### Algorithmic Description (AD)

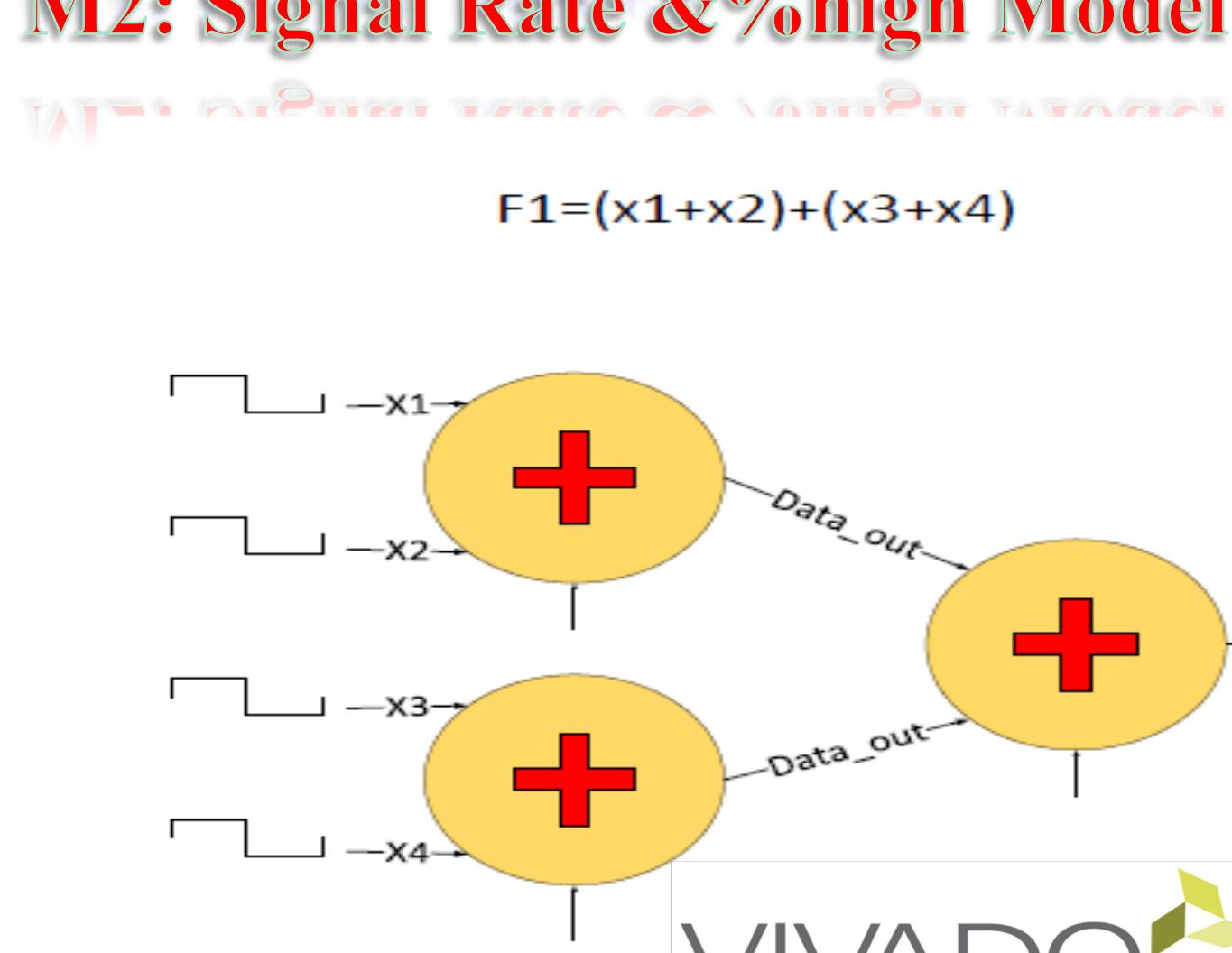
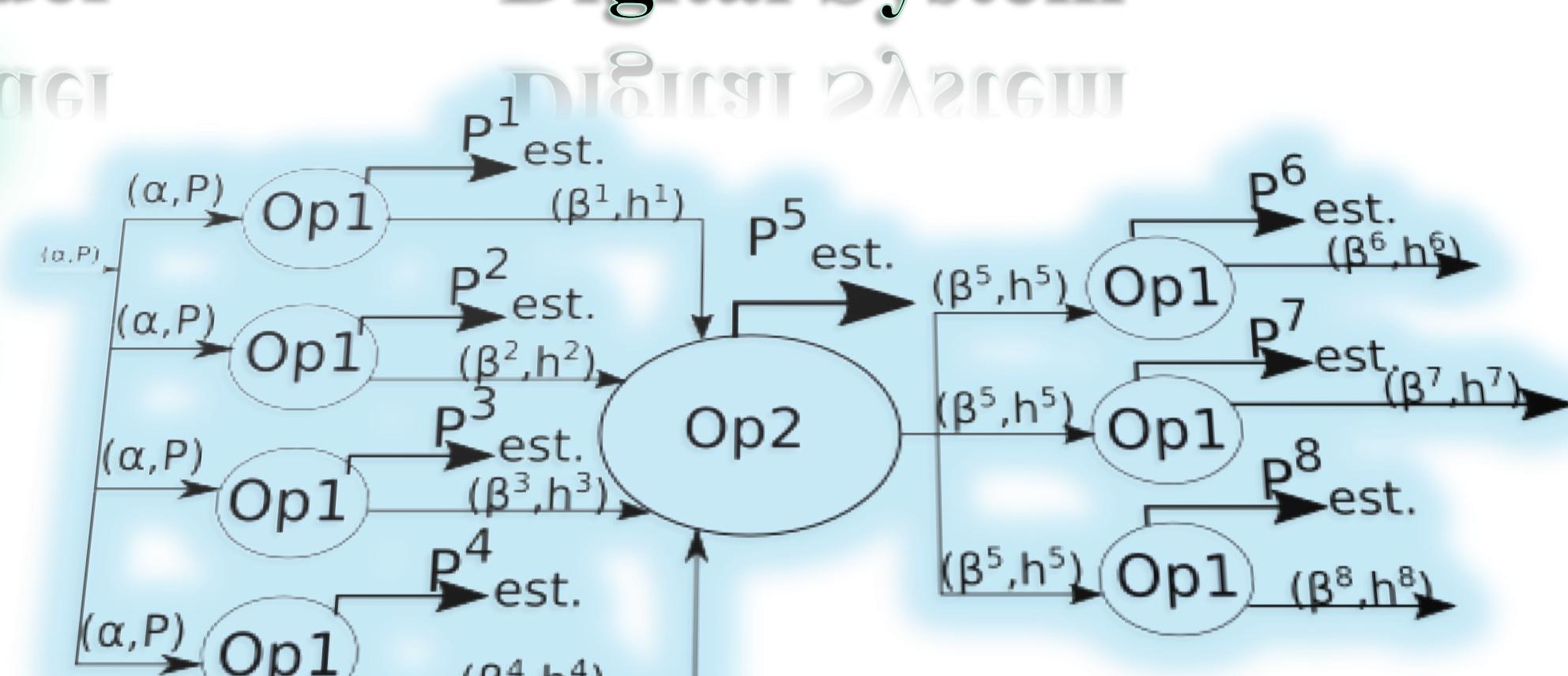


## Deep In The approach

### Digital Operator Model



### Digital System



### Comparing results using Xilinx Tool (XPA) and Power Models :

- Maximum Mean Absolute Error Less Than 1% per Operator
- Maximum Mean Absolute Error Less Than 8% per System

### Advantages:

- Fast and Early Power Estimation
- Flexible Power Evaluation of Different Architectural Scenarios
- Design Space Exploration

### Disadvantages:

- Less Accurate Approach
- Accuracy is Related to the Design Size
- Significant Characterization and Modeling Time

### Future Work:

- Extract Real Power Values from a Real Measurement Bench
- Improve Different Modeling Techniques