



**HAL**  
open science

## Power Aware Framework for Fast & Early Power Estimation on FPGA

Yehya Nasser, Jean-Christophe Prévotet, Maryline Héléard

► **To cite this version:**

Yehya Nasser, Jean-Christophe Prévotet, Maryline Héléard. Power Aware Framework for Fast & Early Power Estimation on FPGA. DATE 2018, PhD Forum, Mar 2018, Dresden, Germany. hal-01734885

**HAL Id: hal-01734885**

**<https://hal.science/hal-01734885>**

Submitted on 15 Mar 2018

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



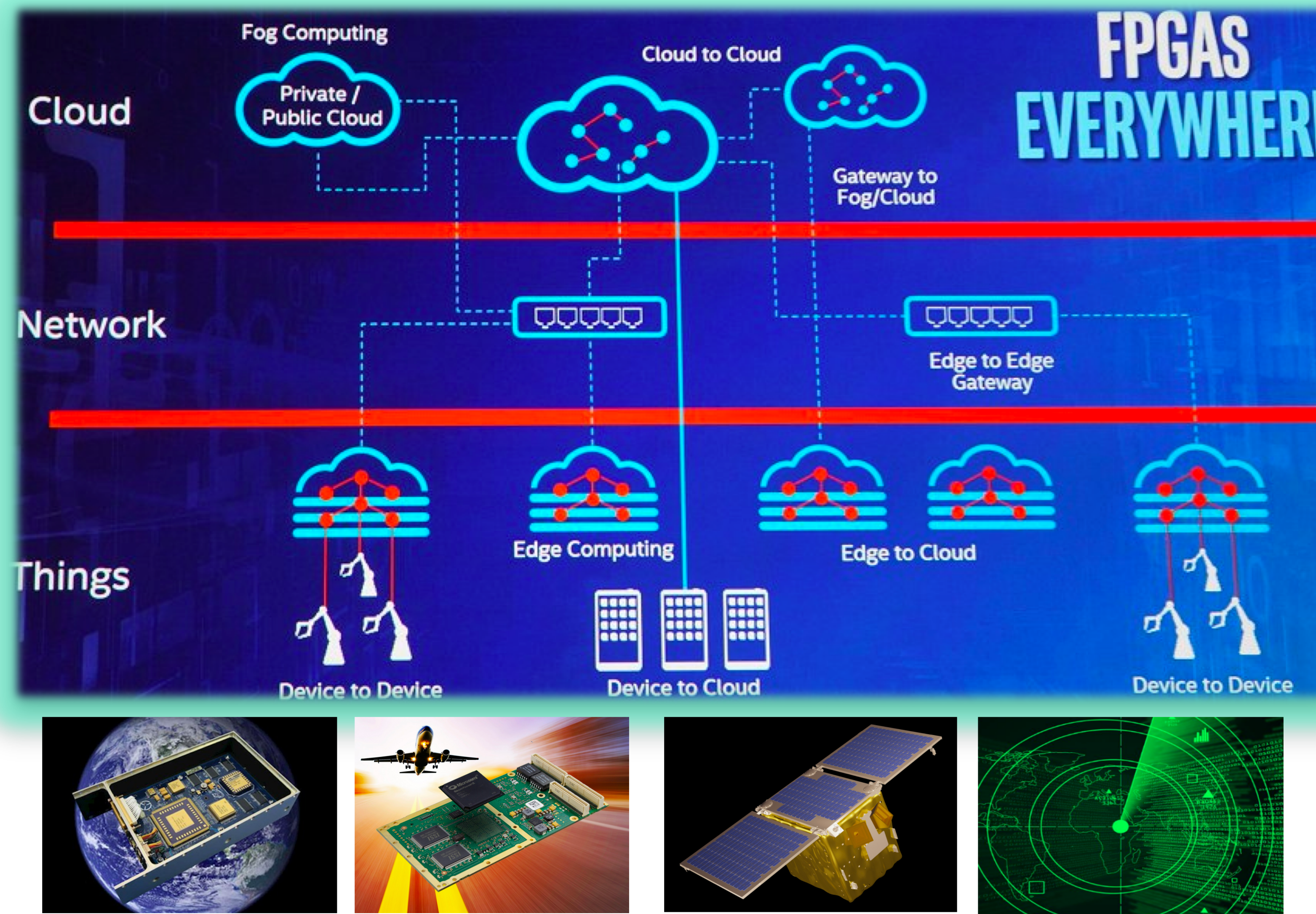
## FPGA Advantages

- Faster Time To Market
- Field Reprogrammability
- Simpler Design Cycle
- More Predictable Project Cycle
- Reusability
- High-End Product
- Good processing speed
- No NRE (Non Recurring Expenses)



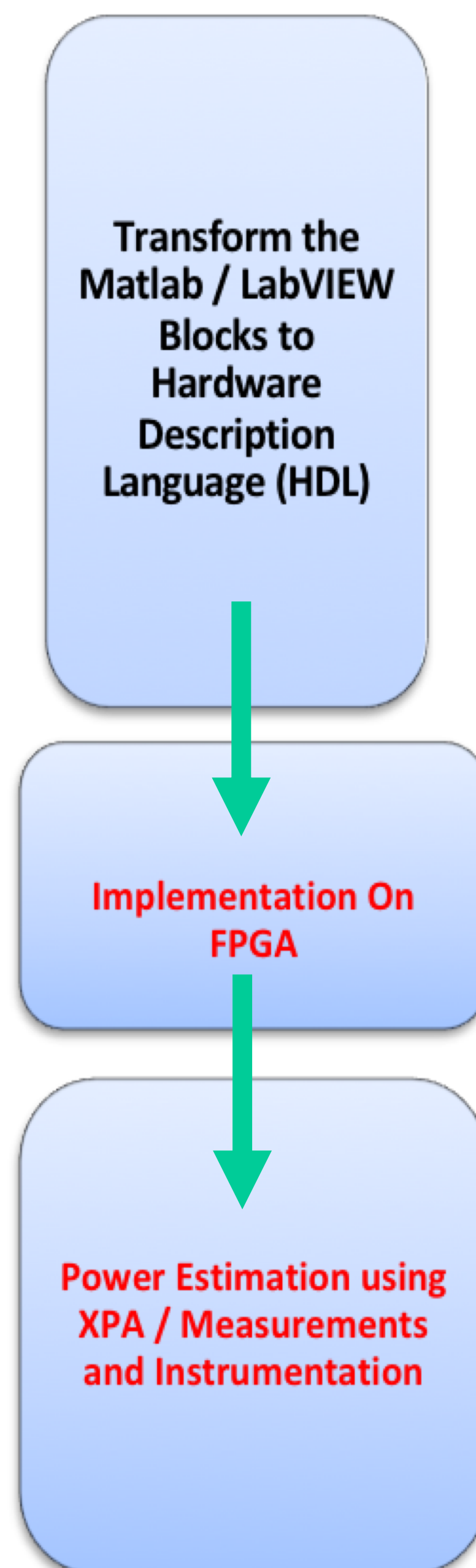
## FPGA Disadvantages

- High Power Consumption
- No Control on Power Optimization
- FPGA Limits The Design Size
- As Quantity Increases Cost Increases



## Problem Statement

### Classical Flow



Signal Processing Researcher



Embedded System Researcher



Q: Does my Algorithm meet the power budget?  
A: Not Yet !!!!

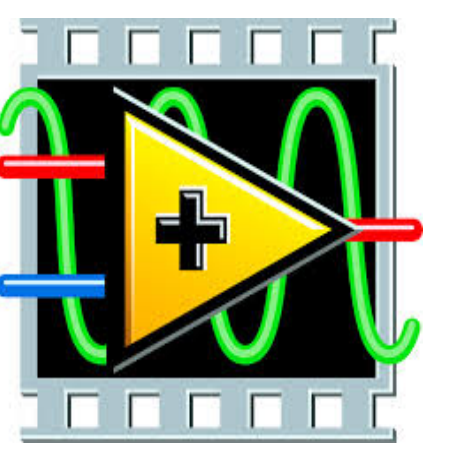
- Problems Regarding Power Estimation
- Today's Tools are Time Consuming
- They Require Implementation for Estimation
- Increase the Time to Market

Can we estimate the power at earlier design stage to facilitate the optimization & avoid hardware implementation?

## Our Research Proposal

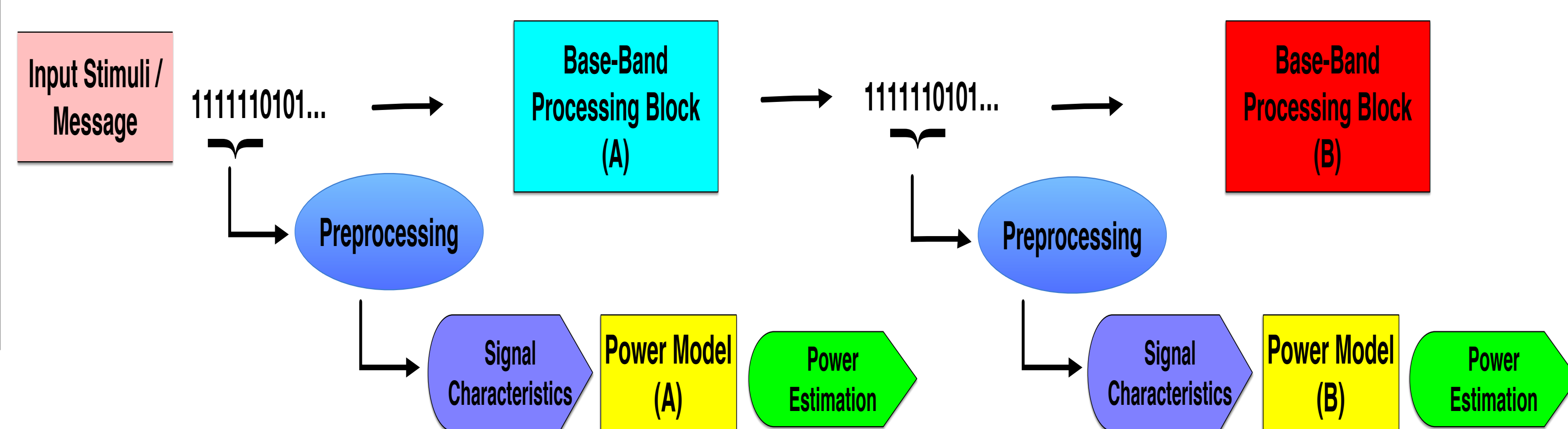
### Power Exploration Framework

Integrated In High Level Tools for POWER ESTIMATION



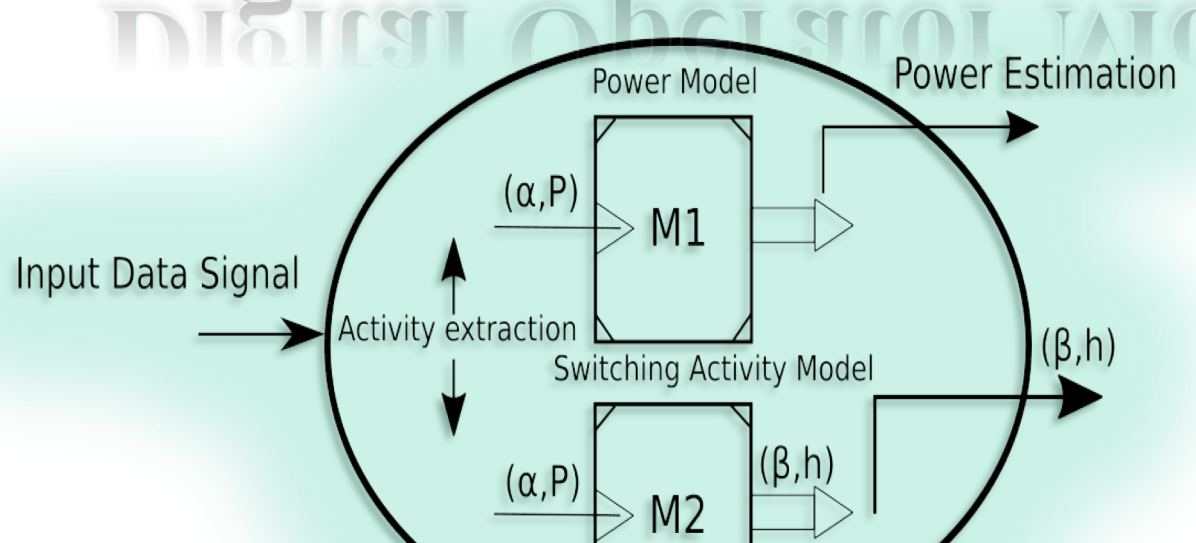
- Bottom up Approach
- Low Level Power Characterization of an Operator on FPGA
- Power Models to be Integrated in a Components Library
- High Level Simulation for Power Estimation
- Power Models Framework to Explore the Design Space

Algorithmic Description (AD)

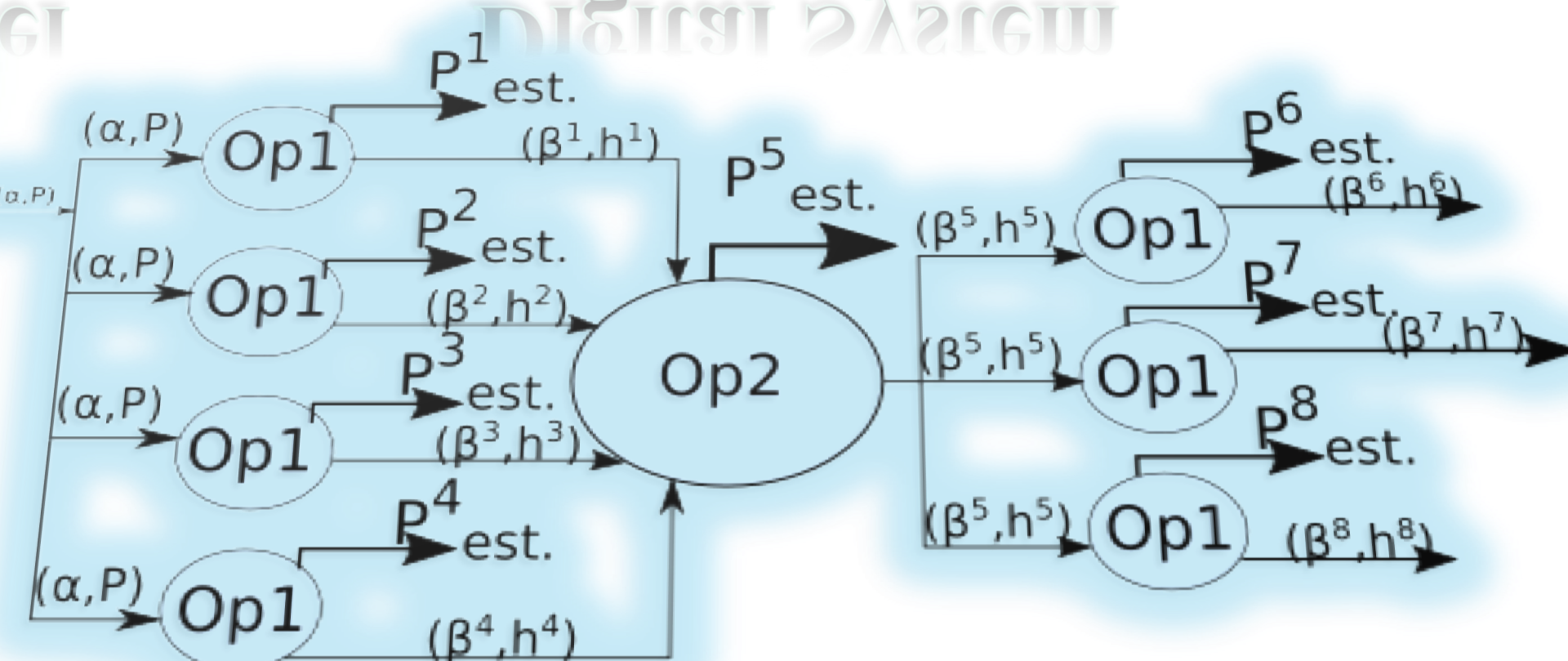


## Deep In The approach

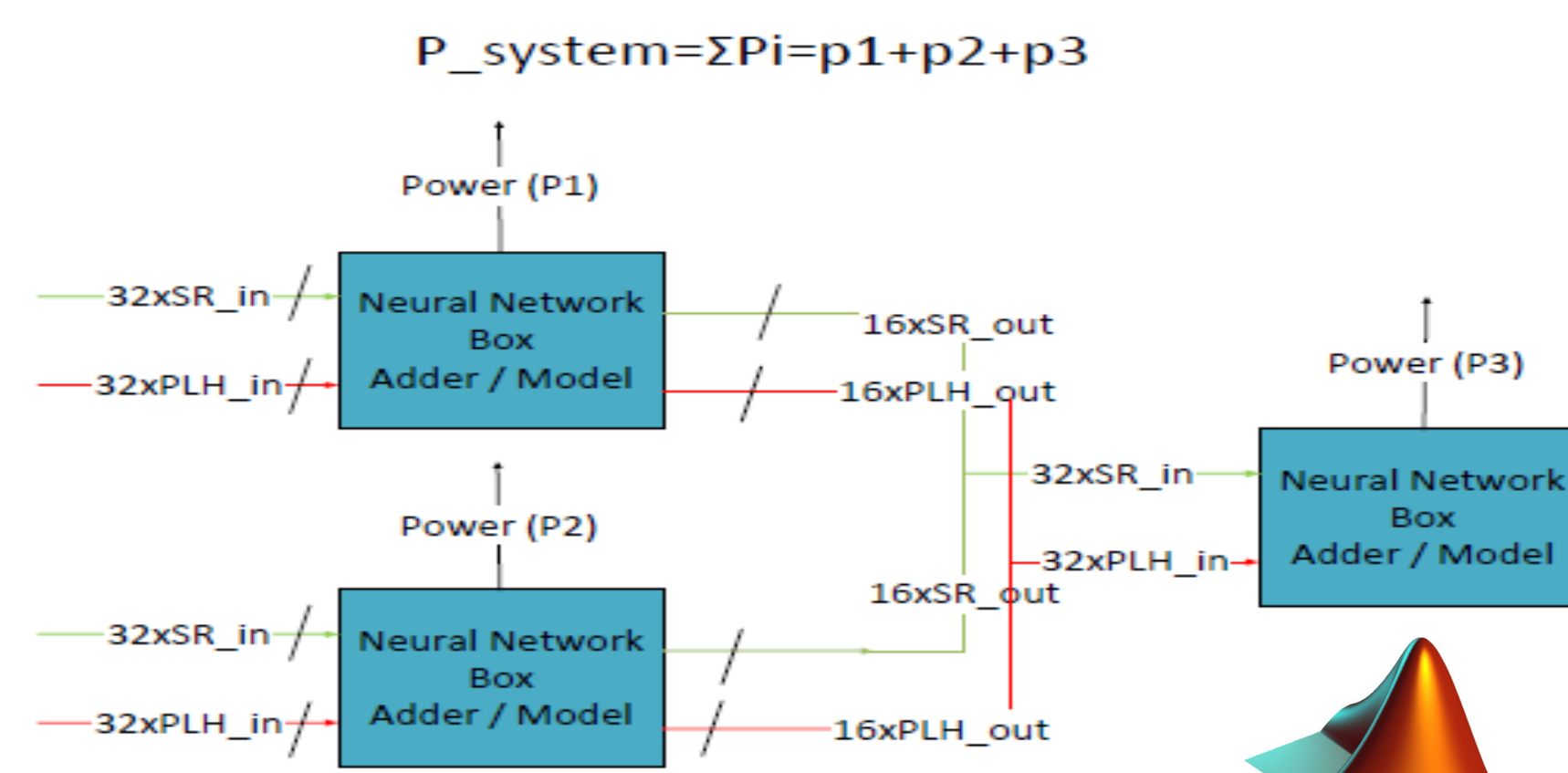
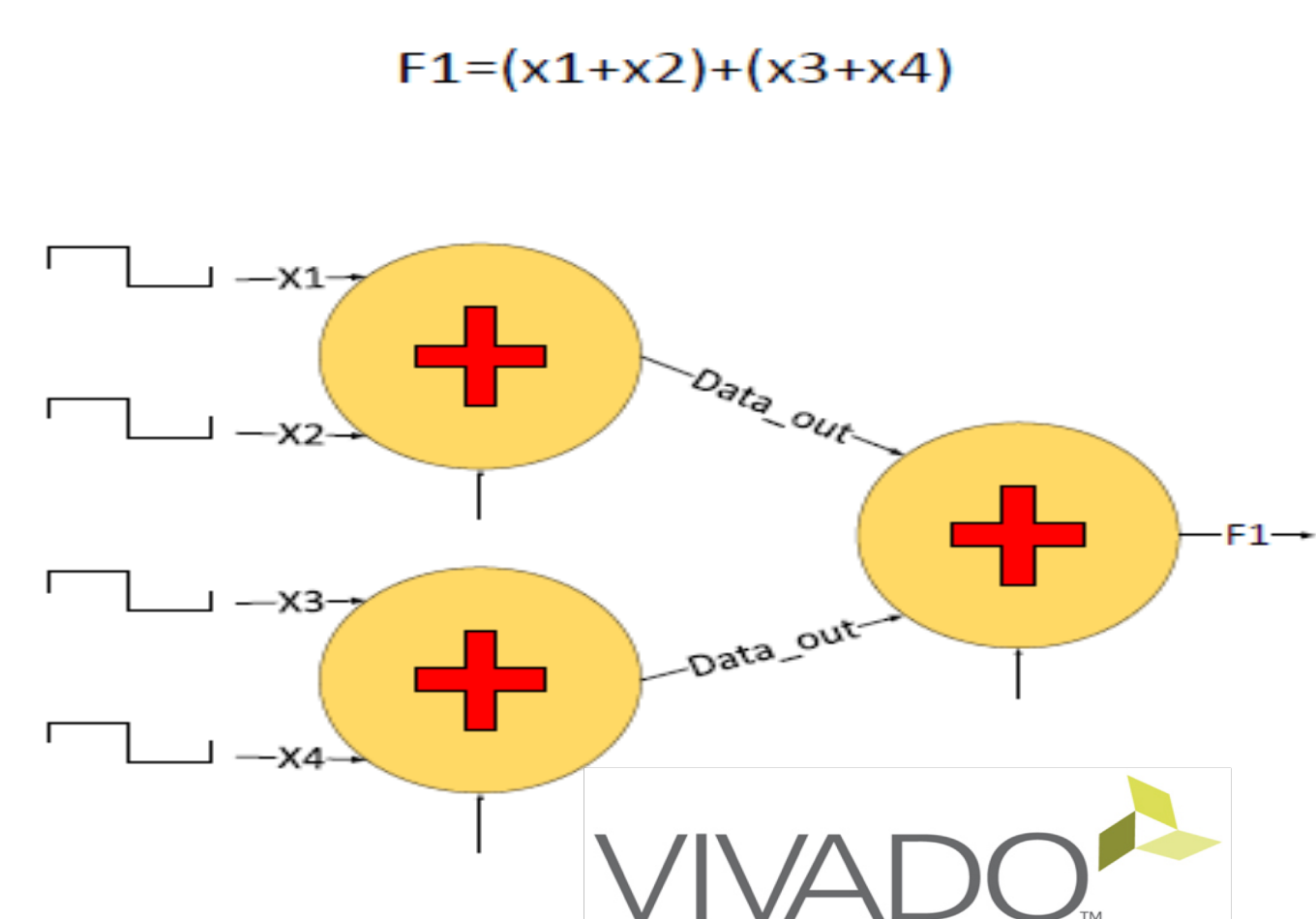
### Digital Operator Model



### Digital System



### Signal Characteristics Propagation



## Results and Conclusion

- ❖ Comparing results using Xilinx Tool (XPA) and Power Models :
  - Maximum Mean Absolute Error Less Than 1% per Operator
  - Maximum Mean Absolute Error Less Than 8% per System
- ❖ Advantages:
  - Fast and Early Power Estimation
  - Flexible Power Evaluation of Different Architectural Scenarios
  - Design Space Exploration
- ❖ Disadvantages:
  - Less Accurate Approach
  - Accuracy is Related to the Design Size
  - Significant Characterization and Modeling Time
- ❖ Future Work:
  - Extract Real Power Values from a Real Measurement Bench
  - Improve Different Modeling Techniques