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Yangping Zhao, Simon Hemour, Hao Chen, Taijun Liu, K. Wu. Power-Handling Capacity and Nonlinearity Analysis for Distributed Electronic Impedance Synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 10.1109/LMWC.2017.2779879 . hal-01722680

HAL Id: hal-01722680

<https://hal.science/hal-01722680v1>

Submitted on 26 Apr 2024

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Power-Handling Capacity and Nonlinearity Analysis for Distributed Electronic Impedance Synthesizer

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Abstract—With advantages of small size, light weight, and fast tuning capability, electronic impedance synthesizer (EIS) presents game-changing opportunities for industry. However, their widely acceptance is still restrained by the understanding of power-handling capacity and linearity issues. This work addresses both issues through the development of a voltage distribution theory which enables simulating voltage at the position of every PIN diode in the distributed EIS. It provides a way of understanding and predicting the power-handling capacity and nonlinearity of EIS from its linear region. As an example of validation for this theory, a 12-bit EIS along with an automatic measurement setup is presented. Experimental results show a good match among measurement, simulation, and analytical model. The 1 dB compression point (P1dB) of the EIS is larger than 35 dBm, and the third-order input intercept point is larger than 57 dBm. Since the proposed theory is validated, it is possible to be used as a criterion in the optimization process to enhance the power-handling capacity and linearity. Potential applications of such high-linearity EIS can be found in Load-Pull systems, noise measurements, variable impedance loads, tunable matching networks, reconfigurable components, and so on.

Index Terms—Electronic impedance synthesizer, impedance tuner, tunable matching network, power-handling capacity, voltage distribution, intermodulation distortion.

I. INTRODUCTION

ALTHOUGH the electromechanical impedance tuner and active tuner are the most used solutions in Load-Pull systems and noise measurements, the technique of electronic impedance synthesizer (EIS) has been discussed in the past few years mainly on the circuit level. Due to the advantages of fast tuning, light weight, small size, and easy to integrate, the EIS, which is based on either PIN diode, varactor, transistor or MEMS switch, has been deployed in Load-Pull

Manuscript received March 8, 2017; revised June 15, 2017 and August 15, 2017; accepted September 17, 2017. This paper was recommended by Associate Editor P. Maffezzoni. (*Corresponding author: Yangping Zhao.*)
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Digital Object Identifier 10.1109/TCSI.2017.2756020

TABLE I
STUDIES OF POWER-HANDLING CAPACITY AND NONLINEARITY OF EIS

	Voltage distribution	P1dB	IP3
[1]	Simulation	Measurement 28.5 dBm (self-actuation power)	Measurement 31 dBm
[4]	Simulation	–	–
[5]	–	–	Measurement OIP3 \approx 48 dBm
[6]	–	Measurement \approx 33 dBm	–
[7]	–	Measurement $P_{out 1dB} = -1dBm$	–
[9]	–	Measurement $>$ 40 dBm	–
[13]	Simulation	Measurement 36 dBm (self-actuation power)	–
[14]	–	Measurement 38.5 dBm	–
This work	Theory & Simulation	Measurement & Simulation 35 dBm	Measurement & Simulation IIP3 = 57 dBm

systems [1], noise measurements [2], tunable matching networks [3]–[8], reconfigurable devices [9]–[12], etc. However, power-handling capacity and nonlinearity are the limiting factors for the EIS development and its popular acceptance in the community.

Power-handling capacity is defined as the maximum average power that could be delivered to EIS without degrading its performance. The 1 dB gain compression point (P1dB) is often used as a metric to evaluate the power-handling capacity. As a matter of fact, every electronic component or system has some degree of nonlinearity, which can be described by the third order input intermodulation point (IIP3) from intermodulation distortion (IMD) test. As listed in Table I, limited work have been done on the power-handling capacity and nonlinearity of EIS. P1dB and IIP3 of an EIS usually can be obtained from measurements and Harmonic Balance simulation, but only for a limited number of impedance states. Because the simulations and measurements are time-consuming and inefficient, especially for the statistic study of an EIS involving thousands of impedance states, they are always used as verification [1].

It is quite a challenge to measure the voltage distribution, so that simulation of voltage distribution is commonly used

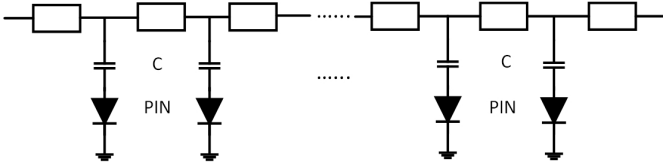


Fig. 1. Topology of distributed electronic impedance synthesizer.

to verify the impedance states [1], [4], or predict the power-handling capacity qualitatively [13]. By contrast, the proposed voltage distribution theory in this work can prove to be very useful to predict the power-handling capacity and nonlinearity quantitatively for distributed nonlinear circuits. The nonlinearity of EIS comes from the nonlinear devices (PIN diodes) in the circuit, therefore, the power handling capacity of an EIS is close related to the operation status of each PIN diode. The analysis of voltage distribution enables to find out the maximum peak voltage along the transmission line. Larger maximum peak voltage will result in lower power-handling capacity, and vice versa. Consequently, if the relationship between power-handling capacity and maximum peak voltage can be established from a small amount of simulations (e.g., 20), it is possible to estimate the power-handling capacity as well as nonlinearity by the proposed voltage distribution theory, and then used as a criterion in the design and optimization process to boost the power-handling capacity and linearity.

In order to validate the theory, a 12-bit distributed EIS is developed and studied statistically. Distributed topologies have a better Smith chart coverage than other topologies [1], [4]. As described in Fig. 1, it consists of a high impedance transmission line periodically loaded with PIN switches and capacitors. Simulation and measurement results are presented in section VI to verify the proposed voltage distribution theory. Good agreement is observed among measurement, simulation and analytical model.

II. METHODOLOGY

In order to simplify the analysis, lossless transmission line is first considered. Fig. 2 (a) shows the circuit of $(m-1)^{th}$ and m^{th} sections of the distributed EIS. The circuit before the $(m-1)^{th}$ diode can be replaced by Thevenin voltage $V_{th,m-1}$, and Thevenin impedance $Z_{th,m-1}$ (Fig. 2(b)). $Z_{th,m-1}$ is the input impedance seen from the position of diode $m-1$ by considering the voltage source as short circuit. In Fig. 2(c), the right-handed side circuit is considered as open circuit when calculating the Thevenin voltage at node m . The voltage $V(z)$ and current $I(z)$ at position z can be expressed as

$$V(z) = A \cdot (e^{-j\beta z} + e^{j\beta z}) = 2A \cos(\beta z), \quad (1)$$

$$I(z) = -j2 \frac{A}{Z_0} \sin(\beta z), \quad (2)$$

where A is the amplitude of the incident signal, β is the phase constant of the transmission line, and Z_0 is the characteristic impedance of the line. The voltage at $z = -l$ can also be calculated by

$$\begin{aligned} V(-l) &= V'_{th,m-1} - I(-l) \cdot Z'_{th,m-1} \\ &= V'_{th,m-1} - j2A \frac{Z'_{th,m-1}}{Z_0} \sin(\beta l), \end{aligned} \quad (3)$$

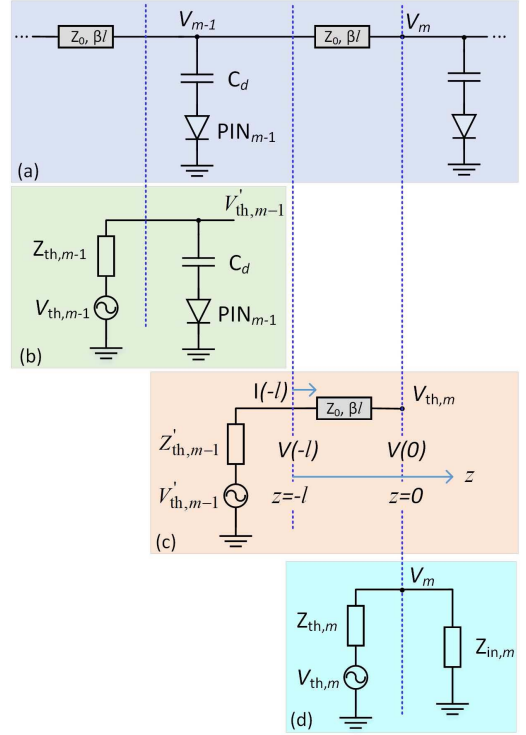


Fig. 2. Diagram for voltage distribution analysis. (a) Equivalent circuit of $(m-1)^{th}$ section; Thevenin equivalent circuit (b) at node $m-1$ with open termination; (c) at node m with open termination; (d) at node m with load.

where Thevenin voltage $V'_{th,m-1}$ and Thevenin impedance $Z'_{th,m-1}$ are intermediate variables after the $(m-1)^{th}$ diode. From (1) and (3), one can obtain the coefficient A

$$A = \frac{V'_{th,m-1}}{2(\cos(\beta l) + j \sin(\beta l) \frac{Z'_{th,m-1}}{Z_0})}. \quad (4)$$

Substitute (4) into (1), the Thevenin voltage at node m can be obtained by letting $z = 0$, and $V_{th,m}$ can be iterated until $m = 1$. If $Z_s = Z_0$, then $V_{th,1} = V_s e^{-j\beta l}$, where V_s is the source voltage, and it is expressed as $V_s = \sqrt{8 \cdot P_0 \cdot \text{real}(Z_s)}$. In order to further simplify the scenario, we assume the PIN diode used here as an ideal switch. As illustrated in Fig. 2(b), the Thevenin voltage $V'_{th,m-1}$ can be calculated from $V_{th,m-1}$ by the theory of voltage divider,

$$V'_{th,m-1} = V_{th,m-1} \cdot \frac{Z_c}{Z_c + Z_{th,m-1} \cdot S_{m-1}}, \quad (5)$$

where $Z_c = 1/j\omega C_d$, and S_{m-1} denotes the status (0 or 1) of the $(m-1)^{th}$ PIN diode. With iteration, one could obtain the relationship between the Thevenin voltage at each node and the source voltage as follows,

$$\begin{aligned} V_{th,m} &= V_s \cdot \frac{1}{\cos(\beta l) + j \sin(\beta l) \frac{Z'_{th,m-1}}{Z_0}} \\ &\times \dots \frac{1}{\cos(\beta l) + j \sin(\beta l) \frac{Z'_{th,1}}{Z_0}} \cdot \frac{1}{\cos(\beta l) + j \sin(\beta l) \frac{Z_s}{Z_0}} \cdot \\ &\frac{Z_c}{Z_c + Z_{th,m-1} \cdot S_{m-1}} \dots \frac{Z_c}{Z_c + Z_{th,1} \cdot S_1}, \end{aligned} \quad (6)$$

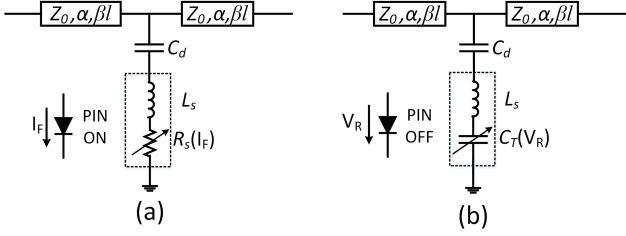


Fig. 3. Equivalent unit circuit model with PIN diode at (a) ON state, and (b) OFF state. Loading capacitor is still considered as ideal capacitor in order to keep the calculation concise.

where $m > 2$. As depicted in Fig. 2 (d), the voltage at node m can be calculated by

$$V_m = V_{th,m} \cdot \frac{Z_{in,m}}{Z_{in,m} + Z_{th,m}}. \quad (7)$$

In practice, the switch and capacitor as well as transmission line are not ideal components, the equivalent circuit model can be described as Fig. 3, in which α denotes the dielectric loss and conductive loss of transmission line. Let us take the parasitic parameters of PIN diode into account, ON state can be described by series inductor L_s and series resistor R_s , which is controlled by forward current I_F . On the other hand, OFF state is described by series inductor L_s and total capacitor C_T , which is controlled by reverse voltage V_R . The loss of transmission line can be included in the calculation by replacing $j\beta$ with $\alpha + j\beta$ in the above calculation. The Z_c in (5) is then changed to

$$Z_c = \frac{1}{j\omega C_d} + j\omega L_s + R_s, \quad (8a)$$

$$Z_c = \frac{1}{j\omega C_d} + j\omega L_s + \frac{1}{j\omega C_T}, \quad (8b)$$

for $S_{m-1} = 1$ and $S_{m-1} = 0$, respectively. And (5) will become

$$V'_{th,m-1} = V_{th,m-1} \cdot \frac{Z_c}{Z_c + Z_{th,m-1}}. \quad (9)$$

Through the voltage divider theory, the peak voltage on the m^{th} PIN diode will be obtained (Fig. 3)

$$V_{PIN,m} = V_m \cdot \frac{j\omega L_s + R_s}{1/j\omega C_d + j\omega L_s + R_s}, \quad (10a)$$

$$V_{PIN,m} = V_m \cdot \frac{j\omega L_s + 1/j\omega C_T}{1/j\omega C_d + j\omega L_s + 1/j\omega C_T}, \quad (10b)$$

for $S_{m-1} = 1$ and $S_{m-1} = 0$, respectively. Although the voltage distribution theory developed in this work is based on the distributed topology as shown in Fig. 1, similar method can be applied to any other distributed topology to help understanding the nature of voltage distribution.

In the linear operation region of EIS, the peak voltage at the position of PIN diode will increase proportionally as square root of operation power increases until harmonics appear. Knowing the voltage distribution of all PIN diodes along the transmission line can help improve the power-handling capacity of EIS in different ways. For a narrowband EIS,

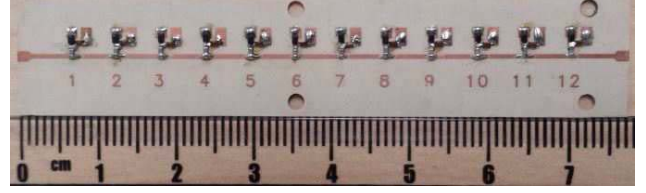


Fig. 4. Fabricated circuit of the EIS, biasing wires are not shown in the graph.

this analysis can be used in the optimization process to avoid the placement of PIN diode at the highest voltage position so as to improve the power-handling capacity [13]. Furthermore, one can remove the worst states in practical implementations and applications without doing a comprehensive power-handling capacity test for all impedance states. Moreover, PIN diode with high power-handling capacity can be placed at the position where high peak voltage appears, then power-handling capacity of the overall circuit will be enhanced.

III. DESIGN OF ELECTRONIC IMPEDANCE SYNTHESIZER

As a validation of the proposed technique, a uniform distributed EIS is designed and tested. In Fig. 4, PIN switches and capacitors are loaded periodically along a high impedance transmission line. In this work, we select the PIN diode SMP1320 with $8 \mu\text{m}$ intrinsic layer from Skyworks Solutions Inc. The impedance of transmission line is set to 83Ω in order to keep the loaded impedance close to 50Ω after loading the capacitors. The loading capacitance and distance between two sections are optimized to 1.8 pF and 5.71 mm , respectively. 12 bits is selected to generate enough impedance states and obtain high Smith chart coverage for 1.5 to 2.1 GHz. The total number of generated impedance states is then $2^{12} = 4096$.

This fabricated circuit (Fig. 4) is optimized by the criteria of Smith chart coverage and power loss. Smith chart coverage stands for the percentage of Smith chart covered by EIS. Visual observation on Smith chart is always used to evaluate the coverage [1], [13]. However, a subjective judgment leads to different results from person to person, and it is not helpful for the parametric study and optimization. To yield a meaningful result and build a goal function for optimization, a quantitative analysis is therefore required. Although the Smith chart coverage has been studied for tunable matching network [15], [16], this definition is not applicable to the case of EIS due to the different scenario. In this work, a similar criterion is developed for EIS.

As shown in Fig. 5 (a), let us first discretize the whole Smith chart, and make sure that there are enough points at each constant voltage standing wave ratio (VSWR) circle. In other words, the discretization process should guarantee enough resolution for applications. We predefined 1116 impedance points in this work for the whole Smith chart, the number of the predefined points varies with the application. Then the measured 4096 impedance points (Fig. 5 (b)) are projected to the predefined Smith chart, and the redundant points are removed, during which the point with minimum loss is preserved if several points are close to each other.

For any mismatched two port network, the insertion loss can be defined as three types of power gain: transducer power

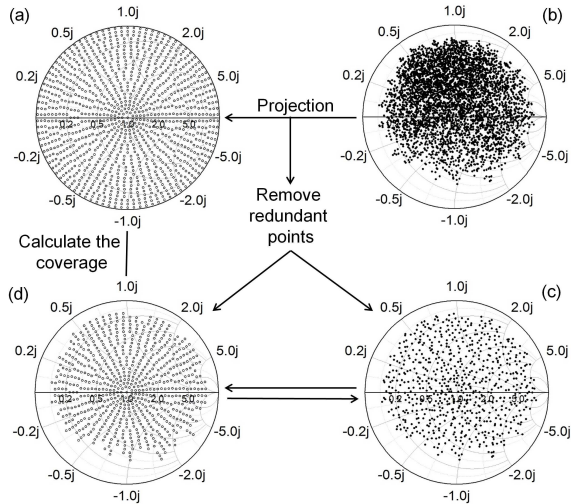


Fig. 5. (a) Predefine 1116 impedance points on Smith chart; (b) measured 4096 impedance points at 1.5 GHz; (c) selected 703 measured points; and (d) selected 703 predefined points.

gain G_T , power gain G_P , and available power gain G_A [17]. The loss definition can be selected according to different scenario. For example, in the calibration process, the EIS will be connected to a 50Ω instrument, the power gain G_P , the ratio of power available from the network and power input to the network, is suitable to describe the loss of the EIS. When an EIS is used as a tunable matching network for reconfigurable devices, both ports are probably not 50Ω , the transducer power gain G_T , which is defined by the ratio of power delivered to the load and power available from the source, is more suitable. It cares about the maximum power transferred to the load, and it considers the power dissipated in the EIS and the mismatching loss on both ports, as well as the conductive and dielectric loss. In this work, we choose the definition of power gain, also called power loss

$$G_P = \frac{|S_{21}|^2}{1 - |S_{11}|^2}, \quad (11)$$

because it is similar to the condition of calibration process or real test with both ports are terminated by 50Ω . In addition, we need to compare the theoretical loss with the measurement.

In a practical application of tunable matching network, the real loss would be smaller [4], benefiting from the port impedance matching. 703 useful impedance points are selected from the measurements (Fig. 5 (c)), and the corresponding 703 predefined impedance points are also selected (Fig. 5 (d)). Finally, Smith chart coverage can be expressed by the ratio of the selected predefined points to the total predefined points ($703/1116 = 63\%$).

The theory of impedance calculation is not presented in this work since it is not the key point. The comparison of Smith chart coverage in Fig. 6 suggests a good match between the theory and measurements. The EIS has more than 60% Smith chart coverage from 1.5 to 2.1 GHz. Since the main focus of this work is related to the power-handling capacity and nonlinearity analysis of EIS, only one frequency point (1.5 GHz) is chosen in the validation experiment due

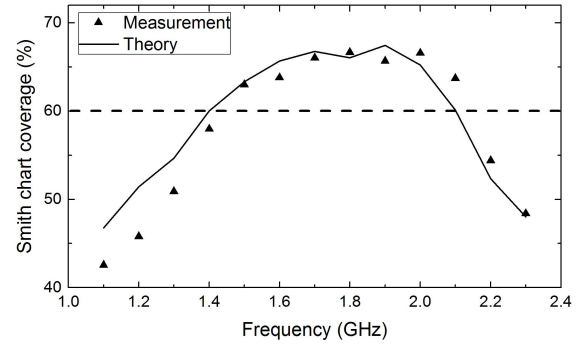


Fig. 6. Comparison of measured and theoretically calculated Smith chart coverage of the fabricated EIS.

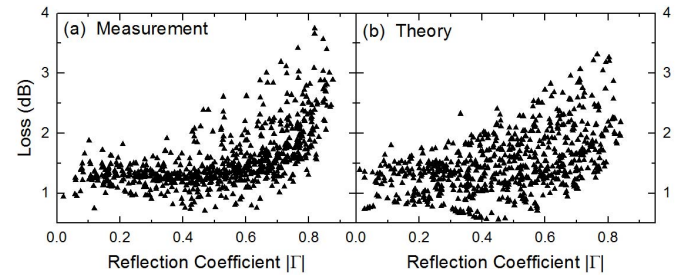


Fig. 7. Comparison of (a) measured and (b) theoretically calculated loss of 703 impedance states at 1.5 GHz.

to the availability of test instruments and components. The measured and theoretically calculated loss for 703 selected points are presented in Fig. 7, a small difference has been observed between measurements and calculations.

IV. AUTOMATIC MEASUREMENT SETUP

In order to develop a statistic power-handling capacity and nonlinearity analysis for the EIS, we programmed an automatic measurement setup (Fig. 8), which can measure the P1dB and IMD automatically for all the 703 impedance states. All the instruments are controlled through GPIB. A controller from Focus Microwaves Inc. is dedicated to switch the impedance state. For each impedance state, both the power-handling capacity test and IMD test need 1 minute, therefore, the total measurement time will be around 23 hours. It should be noted that this is just the measurement time for one frequency point.

Unlike varactor or transistor-based EIS, PIN diode-based EIS is a weakly nonlinear active device, the third-order distortion product is small while the IMD ratio is high. Small test power will result in a third-order distortion product under or near the noise floor of spectrum analyzer so that is not detectable. One solution is to increase the test power. However, when test power exceeds a certain level, more than one distortion mechanism will dominate, the third-order distortion product will increase dramatically [18]. As a result, a proper test power range need to be defined for the DUT according to its nonlinearity degree. In this work, we choose 30 dBm for the IMD test of the EIS, making sure there is only one distortion mechanism, and the distortion from setup is negligible. Further attention to the spectrum analyzer setting is essential.

Inside spectrum analyzer, a mixer is placed after the programmable attenuator, which behaves nonlinearly at high input

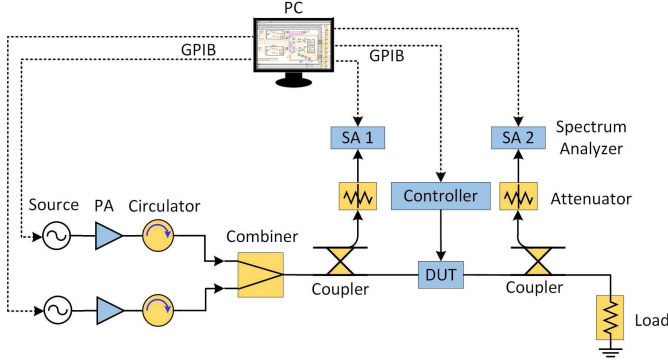


Fig. 8. Automatic measurement setup for power-handling capacity and nonlinearity test of weakly nonlinear devices. The controller is from FOCUS Microwaves Inc. and it can generate different combination for the 12 switches. The highlighted components are chosen to handle high test power.

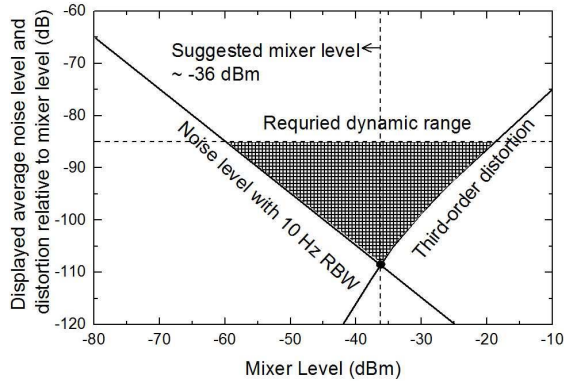


Fig. 9. Displayed average noise level and distortion relative to mixer level of spectrum analyzer, and illustration of suggested test region with enough dynamic range.

power level. To guarantee enough dynamic range and mitigate the distortion from the spectrum analyzer, a good understanding of the dynamic range chart of spectrum analyzer is helpful for the experimental setting. Displayed average noise level and distortion relative to mixer level of PXA N9030A from Keysight are shown in Fig. 9 [19]. As can be seen, the dynamic range of spectrum analyzer at different mixer level is limited by either noise level or third-order distortion, and the best dynamic range will occur at the intersection of the two curves, at which the mixer level is around -36 dBm. Actually, the dynamic range is dependent, directly or indirectly, on the mixer level, internal attenuation, resolution bandwidth, reference level, etc. By keeping the mixer level to the intersection point (-36 dBm), minimum internal attenuation (0 dB), proper resolution bandwidth (10 Hz), and reference level slight higher than maximum input power level (-30 dBm), it will result in a noise floor of -144 dBm with a best possible dynamic range.

In contrast with the internal attenuation, external attenuation will not affect the noise floor of spectrum analyzer, therefore, appropriate external attenuation of 66 dB will be placed to obtain the desired mixer level -36 dBm when the test power 30 dBm is applied. Under this power condition, the IMD ratio of EIS is around 70 dB, in order to have an accurate and stable readout from spectrum analyzer, 15 dB more dynamic range needs to be added. Therefore, the required dynamic range will be 85 dB, together with the noise floor curve and third-order

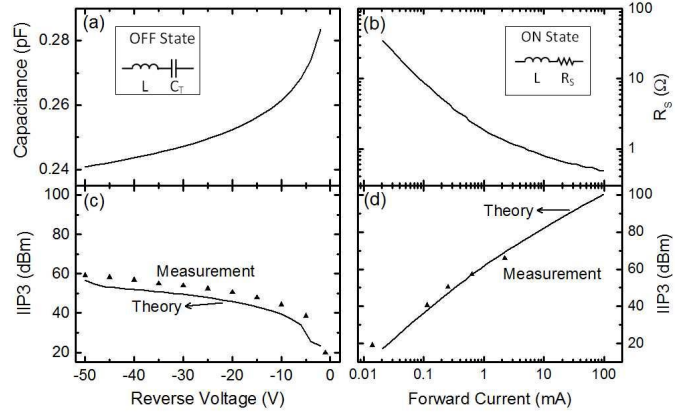


Fig. 10. Nonlinearity of (a) $R_S(I_F)$ and (b) $C_T(V_R)$ characteristics of PIN diode SMP1320. IMD test for both (c) OFF and (d) ON states. Dots denote measurement while line denotes theoretical predictions.

distortion curve, a triangle shadow region is obtained (Fig. 9). Only the measurement in this region can have an accurate result.

V. NONLINEARITY ANALYSIS OF PIN DIODE

The power-handling capacity and nonlinearity of an EIS are highly dependent on the performance of each PIN diode. Therefore, PIN diode needs to be evaluated prior to applying it in the design of an EIS. Appropriate biases of PIN diode for both ON and OFF states will be determined firstly from the IMD measurements. For OFF state, PIN diode can be considered as a voltage controlled capacitor in series with an inductor (inset in Fig. 10 (a)), the IMD is dominated by the nonlinearity of depletion capacitance with reverse bias (Fig. 10 (a)). The third-order intercept point can be predicted by [20]

$$\text{IIP3} = 6.5 - 10 \log(f \cdot Z_0^2 \cdot d^2 C / dV^2) \text{ dBm}, \quad (12)$$

where Z_0 denotes the characteristic impedance of system, and $d^2 C / dV^2$ denotes the second derivative of $C(V)$ characteristic. It has been demonstrated that PIN diode with thicker intrinsic layer has flatter $C(V)$ characteristic due to the small portion of depletion layer compared to the overall thickness [20]. Therefore, IIP3 for OFF state is proportional to the width of intrinsic layer, and inversely proportional to the operation frequency.

For ON state, PIN diode can be considered as a current controlled resistor in series with an inductor (inset in Fig. 10 (b)), the nonlinear IV characteristics in intrinsic layer is the main source of IMD (Fig. 10 (b)). The third-order intercept point can be expressed theoretically by [21]

$$\text{IIP3} = 69 + 15 \log(I_F \cdot \tau \cdot f / R_S) \text{ dBm}, \quad (13)$$

where I_F stands for the forward current, τ denotes the minority carrier lifetime or recombination lifetime, and f represents operation frequency while R_S is the high frequency resistance. Since $R_S = W^2 / 2\mu I_F \tau$, where W is the width of intrinsic layer and μ is ambipolar mobility, then IIP3 is proportional to forward current and operation frequency, and inversely proportional to the width of intrinsic layer.

In order to have a higher IMD for both ON and OFF states, PIN diode needs to be chosen with a tradeoff. The IMD test of

TABLE II
COMPARISON OF DIFFERENT ANALYSIS METHODS FOR
POWER-HANDLING CAPACITY AND NONLINEARITY OF EIS

	Pros	Cons
Analytical model	High computation efficiency	Limited parameters
Simulation	Full parameters	Low computation efficiency; Optimization for discrete problem is unrealistic
Measurement	Real work condition	Complicated measurement setup; Time consuming; Limited parameters

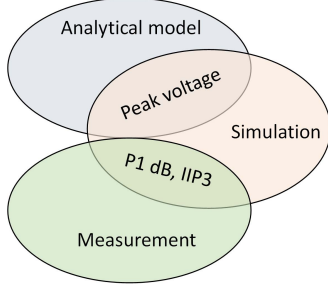


Fig. 11. Relationship between analytical model, simulation and measurement for power-handling capacity and nonlinearity analysis of EIS.

PIN diode SMP1320 under different reverse bias and forward currents are depicted in Fig. 10 (c) and (d). A low IIP3 is measured when a small reverse bias or small forward current is applied. In this case, smaller test power needs to be used for IMD test, otherwise too high test power will result in stronger nonlinearity [18]. As can be seen from Fig. 10 (c) and (d), the theoretical calculation based on (12) and (13) can be used to predict the power-handling capacity of the PIN diode. Finally, a half of the breakdown voltage -25 V is selected for OFF state, and forward bias 30 mA is selected for ON state so as to make sure single PIN diode will have IIP3 more than 50 dBm.

VI. POWER-HANDLING CAPACITY AND NONLINEARITY ANALYSIS OF EIS

As shown in Table II, each analysis method of power-handling capacity and nonlinearity has its own pros and cons. Fig. 11 gives the relationship between the analytical model, simulation and measurement. If the relationship can be managed properly, the analytical model can be used to predict the power-handling capacity and nonlinearity of EIS. First, let us make sure that the peak voltage obtained from analytical model and simulation match each other, and the P1dB as well as IIP3 obtained from simulation and measurement match well. Then we can build a relationship between peak voltage and P1dB, which can predict the real power-handling capacity approximately for thousands of impedance states in an efficient way.

A. Voltage Distribution Analysis

It should be noted that there are multiple reflection along the transmission line because the distributed circuit is not homogenous, while the reflection presented at the input port

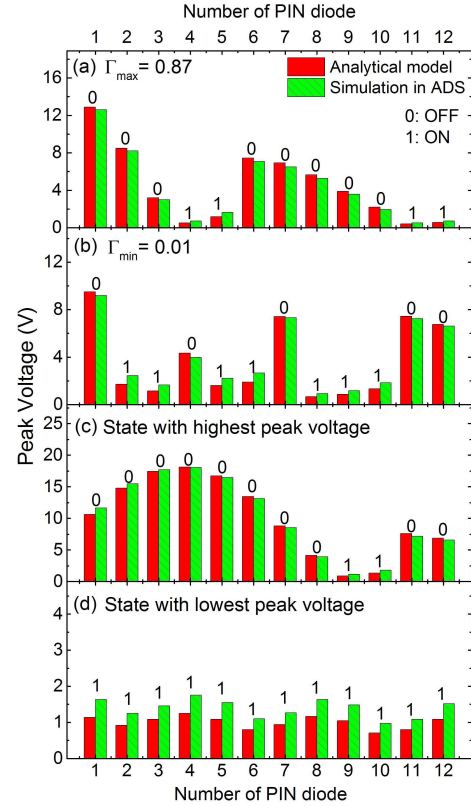


Fig. 12. Comparison of theoretically calculation and simulation results of voltage distribution at the position of PIN diode, under average power of one watt, for (a) the highest Γ state ($\Gamma_{max} = 0.87$); (b) the lowest Γ state ($\Gamma_{min} = 0.01$); (c) impedance state with the highest voltage distribution; and (d) impedance state with the lowest voltage distribution.

is a steady state result. The standing wave existing in the transmission line is not equal to the standing wave presented at the input port. This is validated by the comparison of analytical calculation and simulation with ADS (Fig. 12), and a good match between them shows the effectiveness of analytical model proposed in section II.

Voltage distribution of the two limiting states, called the highest Γ (0.87) and lowest Γ (0.01) under one watt input power, are shown in Fig. 12 (a) and (b), respectively. Fig. 12 (c) and (d) show the calculated and simulated voltage distribution of impedance states with the highest and lowest peak voltages among all the 4096 impedance states. As can be seen, the theoretical calculation matches the simulation very well. Three observations can be highlighted from Fig. 12. Firstly, large peak voltage always appears at the position of PIN diode with the OFF state. Since the series resistance is small for the ON state, small voltage will be assigned to the PIN diode according to the power divider theory. In the OFF state, compared to the loaded capacitance C_d , total capacitance of PIN diode C_T is small. According to the theory of two series capacitor, PIN diode will get most of the voltage. Secondly, the VSWR presented at the input port is not the same as the VSWR existing along the transmission line. For instance, in the lowest Γ case, the equivalent voltage standing wave presented at the input port is 1.02, while the standing wave existing in the transmission line is around 10. Thirdly, compared Fig. 12 (a) with (c), the impedance state with the highest Γ does not mean the largest VSWR existing in the

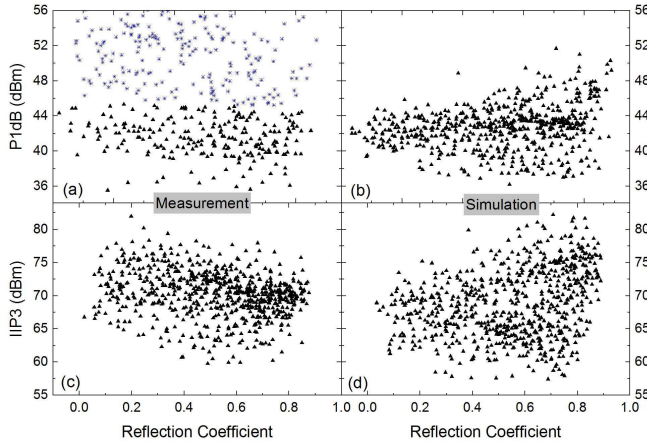


Fig. 13. (a) Measured and (b) simulated P1dB for the selected 703 impedance states. The measured P1dB exceeds 45 dBm (blue star marker) are not accurate because of the polynomial extrapolation accuracy problem. (c) Measured and (d) simulated IIP3 for the selected 703 impedance states under the test power of 30 dBm.

transmission line. In addition, it is not necessary to have the highest voltage distribution.

B. Power-Handling Capacity and Nonlinearity Analysis

With the automatic measurement setup, the P1dB and IMD measurements are implemented for the selected 703 impedance states. In order to avoid the damage caused by high power during the P1dB test, maximum 42 dBm is applied for the sweep. The input P1dB is more meaningful for EIS, because we care about the operation power limit. The measured input P1dB less than 42 dBm are considered accurate (Fig. 13 (a)). For those impedance states which have small compression until 42 dBm, the P1dB is obtained by 3 or 5 order polynomial extrapolation, which somehow will affect the accuracy after the fitting range. Hence, the extracted P1dB larger than 45 dBm are considered inaccurate, which are marked as blue stars in Fig. 13 (a). A possible way to obtain accurate P1dB for all impedance states is to increase the test power. However, the EIS may be burned in some states with a strong nonlinearity. Actually, the power-handling capacity of the EIS will be limited by those impedance states with low level P1dB, thus the minimum P1dB among all states will be considered as an evaluation criterion in the statistic study. The reason why we cannot have the point-to-point comparison in Fig. 13 is that the SPICE model we used in simulation may not be accurate under the condition of a strong nonlinearity. The difference of minimum P1dB from Fig. 13 (a) and (b) is within 2 dB, which means that the simulation could have similar results with measurements from a statistical perspective.

Measured and simulated results of IMD for the selected 703 impedance states are shown in Fig. 13 (c) and (d). As a matter of fact, the low-side third order intermodulation product is not always the same as the high-side product. The measured IIP3 shown in Fig. 13 (c) is the average value of the calculated IIP3 with both products. Similar to the P1dB analysis, the minimum level of IIP3 rather than the highest IIP3 is the limitation of the EIS. Comparing Fig. 13 (c) and (d) suggests that the difference of minimum IIP3 is within 3 dB.

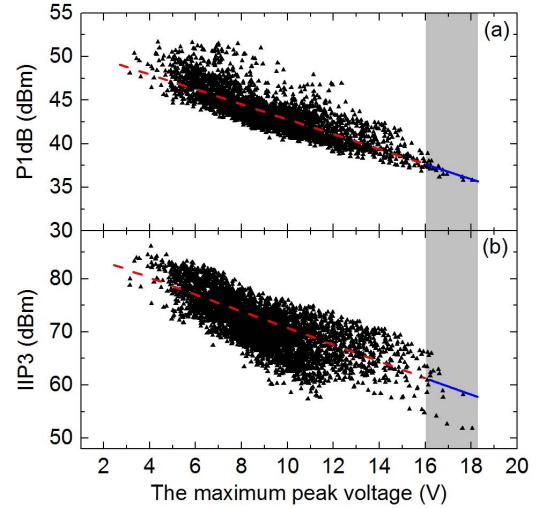


Fig. 14. Relationship of (a) P1dB and (b) IIP3 with the maximum peak voltage along transmission line for all 4096 impedance states, which are obtained from Harmonic Balance simulation in ADS with one watt input power. Blue solid line is the fitting curve of 20 impedance states that are shown in the gray area, while the red dash line is the extension of the fitting curve.

The P1dB and IIP3 of all states do not have a clear relationship with reflection coefficient (Fig. 13), because each impedance state is the result of combination of the ON and OFF states of 12 PIN diodes. Even so, the statistical study shows a good match between simulations and measurements of P1dB and IIP3 of the EIS. In other words, we could know the approximate power-handling capacity and nonlinearity without doing actual measurements.

As discussed in connection with Fig. 12, high peak voltages appear at the position of PIN diode with the OFF state. In addition, from Fig. 10 (c) and (d), we can see that the IIP3 of PIN diode on the OFF state (-25 V) is much lower than that of the ON state (30 mA). All evidences indicate that the nonlinearity of EIS is mainly caused by those PIN diodes with the OFF states, it is proved by the statistic study in Fig. 14, from which we can see that a higher maximum peak voltage results in a lower P1dB and IIP3.

Since the peak voltage is proportional to square root of power, it should have linear relationship with P1dB or IIP3 (dBm) under a linear power region. It is possible to predict the power-handling capacity and IIP3 with the simulation of a small amount of impedance states. As shown in Fig. 14, the blue line is the fitting curve of 20 impedance states with high maximum peak voltage, and the extended line can fit all the simulation results. In order to have a quantitative comparison between the extrapolation and the fitting with the whole set of points, the mean absolute percentage error (MAPE) is applied, and it is 0.3% for P1dB, and is 1.83% for IIP3.

The interesting point is that the proposed voltage distribution theory can help determine this small amount of points, so that we do not have to do the full simulation for all the impedance points. Note that the relationships in Fig. 14 are established under the input power of one watt. If the input power changes, the x-axis will change correspondingly, however, the slope of the fitting line will not change. In addition,

the relationship should be different if different nonlinear device is used.

With the fitted curve, this relationship can be integrated in the analytical model, then we can calculate the power-handling capacity and nonlinearity for all the 4096 impedance points within 30 seconds. By contrast, because of a low computational efficiency of Harmonic Balance (HB) simulations in the *Keysight's* Advanced Design System (ADS), it takes a few hours only for the presented work of Fig. 14. The simulation of one frequency even takes time, needless to say the optimization for an entire frequency band. Circuit simulation engines such as ADS have proven to be a good solution to verify circuit design [1], [4]. However, optimizing thousands of discrete states as well as further data processing are almost impossible within the ADS framework. This is also the major motivation to develop this work. The development of a pure optimization algorithm or technique in this connection is beyond the scope and interest of this work. If the proposed theory can be taken into consideration during the selection and optimization process, power-handling capacity and linearity can be enhanced in different ways. As can be seen from Fig. 12 (c) and Fig. 14, this theory can predict the worst voltage distribution so that one can simply remove the worst states in practical applications even after the circuit is fabricated. Furthermore, for a narrowband distributed EIS in [13], the proposed voltage distribution theory could replace the ADS simulation to find out the proper positions for varactors theoretically, which may result in close maximum rms voltage on each varactor. In this way, the power-handling capacity will be improved. Note that Smith chart coverage in [15] with return loss better than 10 dB and transmission loss better than 1.5 dB was considered as a fitness function in the optimization process with Genetic Algorithm (GA). If the proposed method is integrated, such a fitness function will be modified for the Smith chart coverage with the return loss better than 10 dB, the transmission loss better than 1.5 dB, and the peak voltage lower than a certain level (e.g., 15 V).

From (12) and (13) we know that the relationship of IIP3 with frequency is opposite for the ON and OFF states of PIN diode. Since EIS is the result of combination of the ON and OFF states, there is no clear relationship between the IIP3 with frequency.

VII. CONCLUSION

Power-handling capacity and nonlinearity of PIN diode-based distributed electronic impedance synthesizer (EIS) have been studied statistically from theory, simulation and experiment aspects. Close agreement was obtained between them. With the help of a small amount of simulations, the developed voltage distribution theory can predict the power-handling capacity and nonlinearity of EIS from its linear operation region. In addition, the voltage distribution analysis can largely reduce the computation complexity of EIS, especially involving thousands of discrete impedance states. Therefore, it could be used as a criterion in the selection and optimization process to enhance the power-handling capacity and linearity in different ways. Similar theory can be developed and deployed for any other distributed EIS with different nonlinear devices.

ACKNOWLEDGMENT

The authors would like to thank J. Gauthier, T. Antonescu, all with the Poly-Grames Research Center, Ecole Polytechnique de Montreal, Montreal, QC, Canada, for their technical assistance. The authors are also grateful to Zhebin Wang, with Focus Microwaves Inc., for the deep discussion about electronic tuner. The authors also would like to thank Focus Microwaves Inc. for providing the tuner controller.

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