Multilevel Inverter Topology for Renewable Energy Grid Integration

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***Abstract*—In this paper, a novel three-phase parallel grid connected multilevel inverter (MLI) topology with a novel switching strategy are proposed. This Inverter is intended to feed a microgrid from renewable energy sources (RES) to overcome the problem of the polluted sinusoidal output in classical inverters and to reduce component count, particularly for generating a multilevel waveform with a large number of levels. The proposed power converter consists of n two-level $(n+1)$ phase inverters connected in parallel, where n is the number of RES. The more the number RES, the more the number of voltage levels, the more faithful is the output sinusoidal wave form. In the proposed topology, both voltage pulse width and height are modulated and pre-calculated by using a pulse width and height modulation (PWHM) so as to reduce the number of switching states ($i.e.$ switching losses) and the total harmonic distortion (THD). The topology is investigated through simulations and validated experimentally with a laboratory prototype. Compliance with the IEEE 519-1992 and IEC 61000-3-12 standards is presented and an exhaustive comparison of the proposed topology is made against the classical cascaded H-bridge topology.**

***Index Terms*—Multilevel Inverter, conventional inverter topologies, Six level inverter, Pulse width and height modulation, THD optimization, power quality, grid integration, renewable energy sources.**

I. Introduction

CURRENTLY, there are over 300 GW of wind power generation and over 110 GW photovoltaic generation installed worldwide. Renewable power plants of more than 10 MW in capacity become a reality [1]. However, the renewable energy sources have highly variable daily and seasonal patterns, and consumer power demand requirements are also extremely variable in nature [2]. Therefore, it is difficult to operate a stand-alone power system supplied from only one type of renewable energy source unless appropriate energy storage facilities. If enough energy storage capacity is not available, especially in medium to large-scale systems, a grid-connected renewable power generation may be the only practical solution [3].

For grid integration, the use of simple conventional inverter, two level, produces a square wave which is not suitable for most of the intricate applications. In such cases, a pure sinusoidal wave is desired. Even more, the traditional converters rating power are limited to the rated power of the used semiconductor devices and the allowed switching frequencies [4]. Conventional inverters based on power-frequency transformers operating at 50 or 60 Hz and AC filters are generally used in renewable power generation systems to step up the voltage to the grid voltage levels of 6–36 kV and to reduce the voltage THD respectively. High investment and installation costs are required because of its heavy weight and large size [5]. With the arrival of new high-power semiconductor devices, new power converter structures are designed to meet the needs of future medium or high-voltage converter systems. In this highly active area, the modular multilevel cascaded (MMC) converter topologies and circuits have attracted a high degree of attention for their application in medium and high-voltage systems [6], [7], [8]. The component numbers of MMC converters grow up linearly with the number of levels, individual modules are identical and modular in construction thereby enabling the attainability of a high level number [9]. However, the MMC converter requires balanced multiple-isolated dc sources [10], [11]. Accordingly, its application is not straightforward, especially in renewable power generation systems.

From the Multilevel Inverter side, challenges are nowadays focused on increasing the inverter efficiency [12], [13], [14], improving the power quality and inverter efficiency by reducing THD, decreasing conduction and switching losses to name but a few [15], [16]. However, switching losses are higher than conduction losses and are proportional to the number of switching states [17], [18].

A good survey on multilevel dc-ac power converter topologies is given in [19], [20]. However, all these methods require a high switching frequency leading to increasing switching losses [21]. So, for practical implementation, the reduce of switching frequency is very essential also [22].

This work presents a novel three-phase parallel grid connected multilevel inverter topology with $(2n^2-2)$ levels in the line output voltage waveform, to feed microgrid with n renewable energy sources with an optimized THD. The proposed inverter consists of a parallel connection of n two-level $(n+1)$ phase inverters. Each stage of classic inverter is fed from a renewable energy source, for PV array through a DC–DC converter and for wind power through a AC–DC converter. A six level inverter application has been built in this work, the topology needs six legs (2 cascaded power switches per leg) fed by two renewable energy sources ($i.e.$ wind energy and PV energy) and controlled by a pulse width and height modulation technique. It uses only 12 switching states per period and allows to eliminate from 2^{nd} up to

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10^{th} order harmonics without an extra filtering circuit. This approach reduce significantly the number of required power switches and the switching frequency as compared to the classical topologies. Moreover, the proposed topology shows similarities with the Cascaded H-bridge (CHB) topology in two ways: 1) It needs multiple isolated input dc voltages; and 2) input dc voltage levels can be combined into all additive values. The proposed topology and the related analysis along with simulation and experimental verification is the main contribution of this work.

The paper is organized as follows. Section II describes the generalized topology of the proposed multilevel inverter. In section III, a six level inverter application is studied and discussed, a selected harmonic elimination method is discussed. In section IV the simulation and experimental results along with their compliance to various international standards are validated. A comparison of the proposed topology with classical topologies is presented in Section V. Conclusions are summarized in section VI.

II. Generalized Multilevel Inverter Topology and Operating Principle

Fig.1 shows the generalized three-phase multilevel inverter topology. It consists of n renewable sources (n DC sources) feeding microgrid. In general, the DC voltage sources can have different values. However, in order to optimize the total harmonic order of the multilevel output waveform, they are considered to be optimized, and regulated through DC-DC or AC-DC converters. The multilevel inverter consists of $2n^2+2n$ power switches, so $4n^2+4n$ insulated gate bipolar transistors (IGBT) with antiparallel diodes $S_{i,j}$ $(1 < i < 2n$ $, 1 < j < (n+1))$. For instance, when S_{11} and S_{22} are turned ON, the output voltage U_{ab} is equal to E_1, when S_{11}, S_{24}, S_{34}, S_{43}, S_{53} and S_{62} are turned ON the output voltages U_{ab}, U_{bc} and U_{ca} are $E_1+E_2+E_3$, $-E_3$ and $-E_2-E_1$ respectively. As$U_{ab}+U_{bc}+U_{ca}=0$ for each switching state, so a balanced system is obtained. Following the same combination, $n^2+2(n-1)$ possible levels $(E_1, E_2, (E_1+E_2), E_3, ...E_n)$ for the output waveform are obtained. Therefore, the switches have to withstand both positive and negative voltages. In addition, the switches have to conduct backward current that is a result of the grid inductive nature. It can be concluded that the switches must be bidirectional. There are several circuit configurations for bidirectional switches In this study, the common emitter topology is used as it, requires only one gate driver per switch. Table I shows the states of the switches for each output voltage value, 1 corresponds to the switch ON state, 0 corresponds to the OFF state and k is variable according to the switching state.

By considering Fig. 1, $2n^2+2n$ states are obtained, but some switching states are not allowed, to avoid a short circuits of renewable energy sources and/or output voltage, so:

-$S_{kj}$and $S_{(k+1)_j}(k=1,3,5,...2(n-1),\ j=1:(n+1))$ can not be ON in the same time to avoid a short circuit of renewable energy sources.

-$S_{ik}$and $S_{i(k+1)}(\ i=1:2n$, and$k=1:3)$ can not be ON in the same time to avoid short circuit of output voltages.

So, for each value of the output multilevel voltages, $2n$ switches must be turned ON, two from each renewable energy source corresponding inverter.

By considering Fig. 1,

$$N_{switch}=\begin{cases} 6, & \text{for } n=1 \\ 2n^2+2n & \text{for } n\geq 2 \end{cases} \tag{1}$$

$$N_{driver}=N_{switch} \tag{2}$$

$$N_{IGBT}=2N_{switch} \tag{3}$$

$$N_{source}=n \tag{4}$$

where, N_{switch} , N_{driver} , N_{IGBT} , and N_{source} are respectively the number of switches, number of switch drivers, number of IGBTs and number of renewable energy sources.

In addition, the number of levels synthesized by the topology is given by

$$N_{Level}=N=2n^2-2 \tag{5}$$

The peak voltage attained for such a configuration is given by

$$v_{max}=\textstyle\sum_1^n E_i \tag{6}$$

By considering $F_{S_{ij}}$as connection function of switch S_{ij}, so

$$F_{S_{ij}}=\begin{cases} 0 & \text{if switch } S_{ij}\text{is turned OFF} \\ 1 & \text{if switch } S_{ij}\text{is turned ON} \end{cases} \tag{7}$$

By using (7) and physical connection of the inverter, the electric potential at the output points a, b and c of the inverter with respect to the virtual neutral are deduced (see eq. 8).

The output phase-to-phase voltages can be obtained by using (8):

$$\begin{cases} U_{ab}=V_{a0}-V_{b0} \\ U_{bc}=V_{b0}-V_{c0} \\ U_{ca}=V_{c0}-V_{a0} \end{cases} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix} \tag{9}$$

III. A Six Level Inverter Application Considerations

The six-level topology shown in Fig. 2 uses two renewable sources (as wind and solar emulators), which represented by two voltage sources E_1 and E_2 across the two capacitors (C_1 and C_2). In this case $n=2$, from (1) this topology requires 12 switches $(S_{11}, S_{12}, S_{13}, S_{21}, S_{22}, S_{23}, S_{31}, S_{32}, S_{33}, S_{41}, S_{42}, S_{43})$ and from (3) the topology will require 24 IGBTs.

From (8) the electric potential at the output points a, b and c of the inverter referred to a virtual neutral potential are deduced (10):

$$\begin{cases} V_{a0}=(F_{S_{11}}-F_{S_{21}})E_1+(F_{S_{31}}-F_{S_{41}})E_2 \\ V_{b0}=(F_{S_{12}}-F_{S_{22}})E_1+(F_{S_{32}}-F_{S_{42}})E_2 \\ V_{c0}=(F_{S_{13}}-F_{S_{23}})E_1+(F_{S_{33}}-F_{S_{43}})E_2 \end{cases} \tag{10}$$

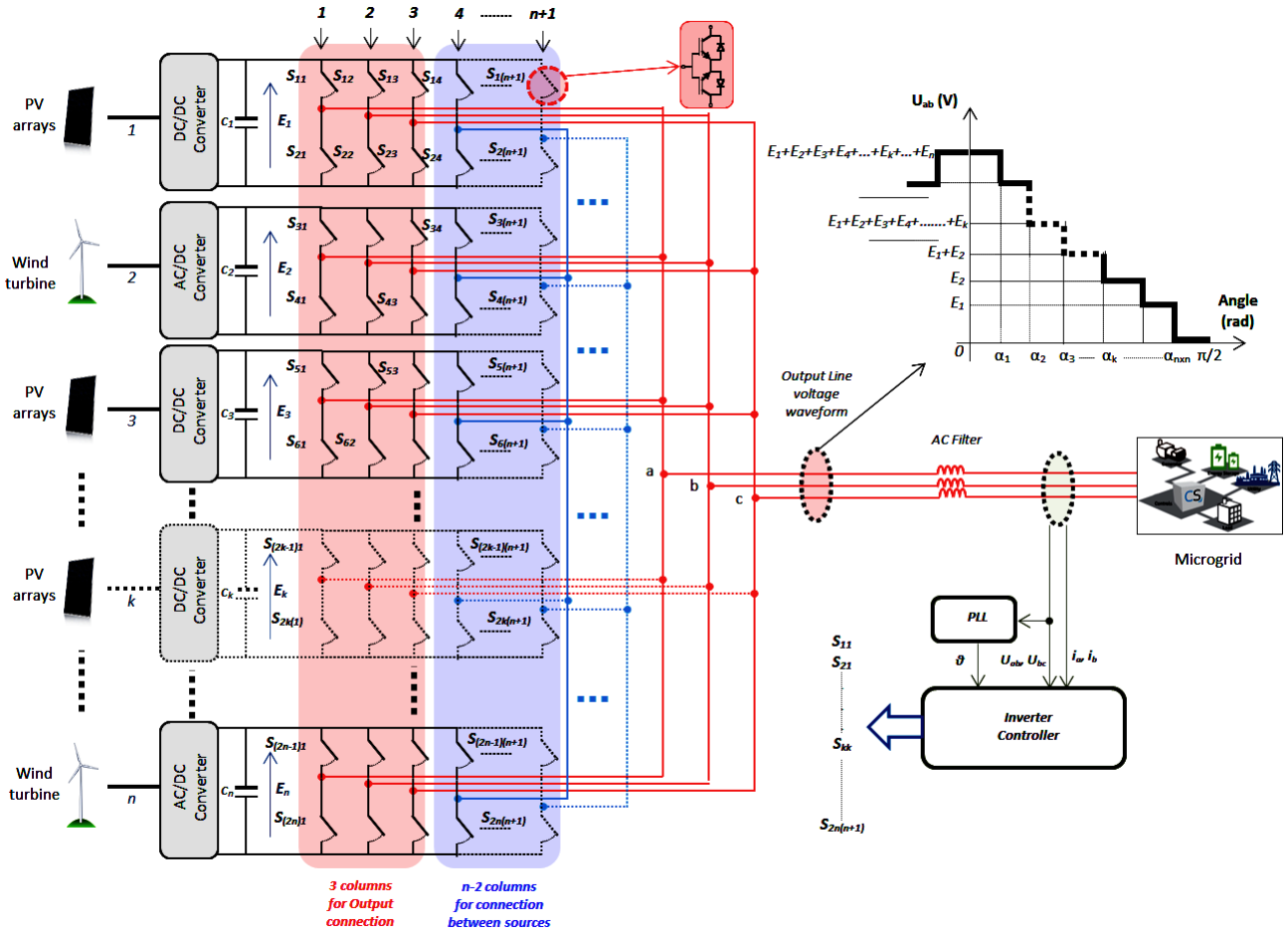

Fig. 1. Proposed generalized multilevel inverter topology

TABLE I
OUTPUT VOLTAGES FOR DIFFERENT STATES OF SWITCHES

State	Switches states																		U_{ab}	U_{bc}	U_{ca}
	S_{11}	S_{12}	S_{13}	S_{14}	$\cdots$	$S_{1(n+1)}$	S_{21}	S_{22}	S_{23}	S_{24}	$\cdots$	$S_{2(n+1)}$	$\cdots\cdots$	S_{n1}	S_{n2}	S_{n3}	S_{n4}	$\cdots$	$S_{n(n+1)}$			
1	1	0	0	0	$\cdots$	0	0	0	0	1	$\cdots$	0	$\cdots$	0	1	0	0	$\cdots$	0	$\sum_{i=1}^{n} E_i$	$-\sum_{i=1}^{k} E_i$	$-\sum_{i=k}^{n} E_i$
2	0	0	0	0	$\cdots$	0	0	0	0	0	$\cdots$	0	$\cdots$	0	1	0	0	$\cdots$	0	$\sum_{i=1}^{n-1} E_i$	$-\sum_{i=1}^{k+1} E_i$	$-\sum_{i=n-1}^{k-1} E_i$
$\vdots$	$\vdots$																					
N	1	0	0	0	$\cdots$	0	0	1	1	0	$\cdots$	0	$\cdots$	0	0	0	0	$\cdots$	0	E_1	$\sum_{i=2}^{n-k} E_i$	$-\sum_{i=1}^{n-k} E_i$

$$\begin{cases} V_{a0} = \sum_{i=1}^{n} \left[(F_{S_{(2i-1)1}} - F_{S_{(2i)1}})E_i + \sum_{j=4}^{n+1} (F_{S_{(2i)j}} - F_{S_{(2i-1)j}}) \left[\sum_{l=1,3,5..(l\neq i)}^{2n-1} (F_{S_{lj}} - F_{S_{(l+1)j}}) E_{\frac{l+1}{2}} \right] \right] \\ V_{b0} = \sum_{i=1}^{n} \left[(F_{S_{(2i-1)2}} - F_{S_{(2i)2}})E_i + \sum_{j=4}^{n+1} (F_{S_{(2i)j}} - F_{S_{(2i-1)j}}) \left[\sum_{l=1,3,5..(l\neq i)}^{2n-1} (F_{S_{lj}} - F_{S_{(l+1)j}}) E_{\frac{l+1}{2}} \right] \right] \\ V_{c0} = \sum_{i=1}^{n} \left[(F_{S_{(2i-1)3}} - F_{S_{(2i)3}})E_i + \sum_{j=4}^{n+1} (F_{S_{(2i)j}} - F_{S_{(2i-1)j}}) \left[\sum_{l=1,3,5..(l\neq i)}^{2n-1} (F_{S_{lj}} - F_{S_{(l+1)j}}) E_{\frac{l+1}{2}} \right] \right] \end{cases} \quad (8)$$

As a result, the output phase-to-phase multilevel voltages will be given by (11).

$$\begin{cases} U_{ab} = V_{a0} - V_{b0} \\ U_{bc} = V_{b0} - V_{c0} \\ U_{ca} = V_{c0} - V_{a0} \end{cases} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} (F_{S_{11}} - F_{S_{21}}) & (F_{S_{31}} - F_{S_{41}}) \\ (F_{S_{12}} - F_{S_{22}}) & (F_{S_{32}} - F_{S_{42}}) \\ (F_{S_{13}} - F_{S_{23}}) & (F_{S_{33}} - F_{S_{43}}) \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \end{bmatrix} \quad (11)$$

A. Operation Principle

The required six phase-to-phase voltage output levels ($\pm E_1$, $\pm E_2$ $\pm (E = E_1 + E_2)$) are generated as follows:

1) When turning ON the switches S_{13}, S_{22}, S_{31} and S_{43} during the first cycle $[0, \alpha_1]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = E_1 + E_2$, $U_{bc} = -E_1$ and $U_{ca} = -E_2$. Fig.3 (left) shows the current path for this mode.

2) When turning ON the switches S_{12}, S_{23}, S_{31} and S_{42} during the second cycle $[\alpha_1, \alpha_2]$, three levels are generated

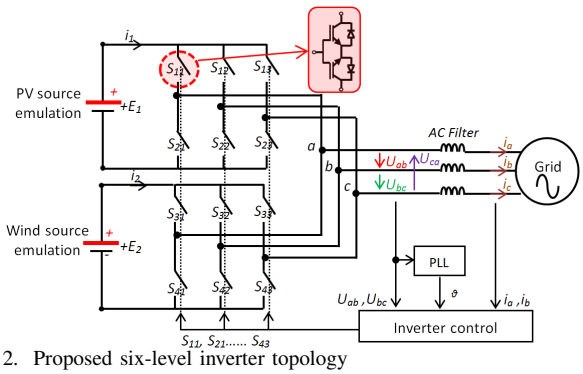

Fig. 2. Proposed six-level inverter topology

for the three phase-to-phase voltages i.e, $U_{ab} = E_2$, $U_{bc} = E_1$ and $U_{ca} = -E_1 - E_2$. Fig.3 (right) shows the current path for this mode.

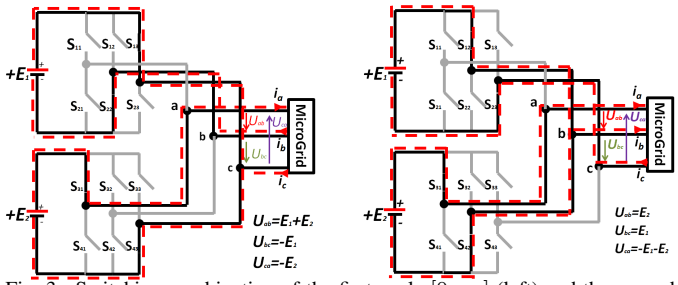

Fig. 3. Switching combination of the first cycle $[0, \alpha_1]$ (left) and the second cycle $[\alpha_1, \alpha_2]$ (right)

3) When turning ON the switches S_{11}, S_{22}, S_{32} and S_{43} during the third cycle $[\alpha_2, \alpha_3]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = E_1$, $U_{bc} = E_2$ and $U_{ca} = -E_1 - E_2$. Fig.4 (left) shows the current path for this mode.

4) When turning ON the switches S_{12}, S_{21}, S_{31} and S_{43} during the fourth cycle $[\alpha_3, \alpha_4]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_1$, $U_{bc} = E_1 + E_2$ and $U_{ca} = -E_2$. Fig.4 (right) shows the current path for this mode.

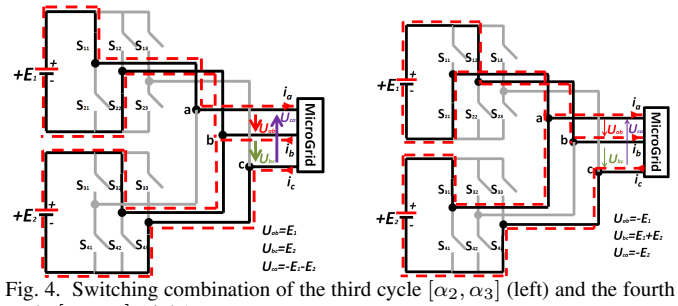

Fig. 4. Switching combination of the third cycle $[\alpha_2, \alpha_3]$ (left) and the fourth cycle $[\alpha_3, \alpha_4]$ (right)

5) When turning ON the switches S_{12}, S_{23}, S_{32} and S_{41} during the fifth cycle $[\alpha_4, \alpha_5]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_2$, $U_{bc} = E_1 + E_2$ and $U_{ca} = -E_1$. Fig.5 (left) shows the current path for this mode.

6) When turning ON the switches S_{13}, S_{21}, S_{32} and S_{43} during the sixth cycle $[\alpha_5, \alpha_6]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_1 - E_2$, $U_{bc} = -E_2$ and $U_{ca} = E_1$. Fig.5 (right) shows the current path for this mode.

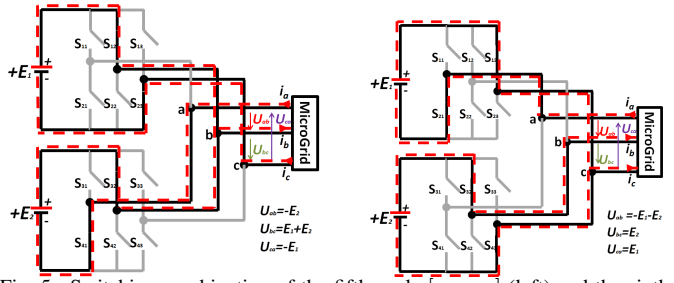

Fig. 5. Switching combination of the fifth cycle $[\alpha_4, \alpha_5]$ (left) and the sixth cycle $[\alpha_5, \alpha_6]$ (right)

7) When turning ON the switches S_{12}, S_{23}, S_{33} and S_{41} during the seventh cycle $[\alpha_6, \alpha_7]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_1 - E_2$, $U_{bc} = E_1$ and $U_{ca} = E_2$. Fig.6 (left) shows the current path for this mode.

8) When turning ON the switches S_{13}, S_{22}, S_{32} and S_{41} during the eighth cycle $[\alpha_7, \alpha_8]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_2$, $U_{bc} = -E_1$ and $U_{ca} = E_1 + E_2$. Fig.6 (right) shows the current path for this mode.

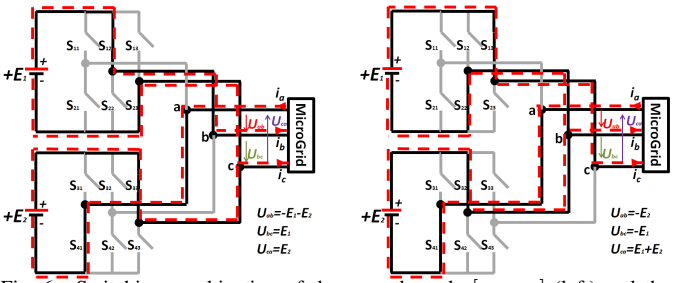

Fig. 6. Switching combination of the seventh cycle $[\alpha_6, \alpha_7]$ (left) and the eighth cycle $[\alpha_7, \alpha_8]$ (right)

9) When turning ON the switches S_{12}, S_{21}, S_{33} and S_{42} during the ninth cycle $[\alpha_8, \alpha_9]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = -E_1$, $U_{bc} = -E_2$ and $U_{ca} = E_1 + E_2$. Fig.7 (left) shows the current path for this mode.

10) When turning ON the switches S_{11}, S_{22}, S_{33} and S_{41} during the tenth cycle $[\alpha_9, \alpha_{10}]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = E_1$, $U_{bc} = -E_1 - E_2$ and $U_{ca} = E_2$. Fig.7 (right) shows the current path for this mode.

11) When turning ON the switches S_{13}, S_{21}, S_{31} and S_{42} during the eleventh cycle $[\alpha_{10}, \alpha_{11}]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = E_2$, $U_{bc} = -E_1 - E_2$ and $U_{ca} = E_1$. Fig.8 (left) shows the current path for this mode.

12) When turning ON the switches S_{11}, S_{23}, S_{33} and S_{42} during the twelfth cycle $[\alpha_{11}, \alpha_{12}]$, three levels are generated for the three phase-to-phase voltages i.e, $U_{ab} = E_1 + E_2$, $U_{bc} = -E_2$ and $U_{ca} = -E_1$. Fig.8 (right) shows the current path for this mode.

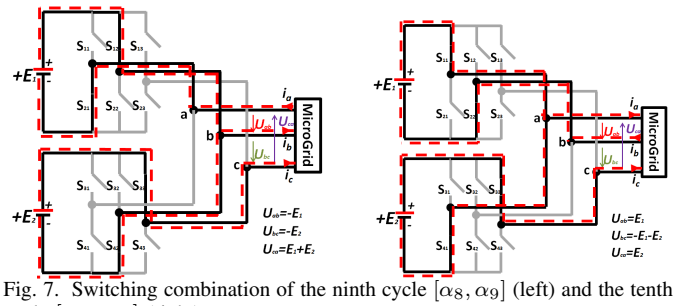

Fig. 7. Switching combination of the ninth cycle $[\alpha_8, \alpha_9]$ (left) and the tenth cycle $[\alpha_9, \alpha_{10}]$ (right)

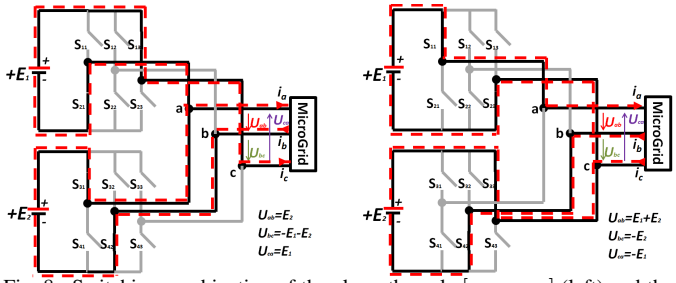

Fig. 8. Switching combination of the eleventh cycle $[\alpha_{10}, \alpha_{11}]$ (left) and the twelfth cycle $[\alpha_{11}, \alpha_{12}]$ (right)

The output waveform of the proposed six-level MLI can be seen in Fig. 9.

B. Calculation of losses

The losses associated with a power electronic converter can be equated with the aggregation of power losses incurred in the individual semiconductor devices. Losses incurred by a semiconductor device can be typically described under three categories: 1) when the device is blocking (i.e., OFF state); 2) when the device is conducting (i.e., ON state); and 3) when the device is switching (i.e., the state is changing from ON to OFF or vice versa). Since leakage currents during the blocking state are practically negligible [26], the losses are insignificant. Therefore, only conduction and switching losses are considered for the calculation of losses associated with the proposed inverter topology.

1) Conduction Losses: All switches required in the proposed topology are bidirectional conducting and bidirectional blocking, as shown in Fig. 1, the instantaneous conduction losses of typical transistor and diode are expressed as [28],

$$\rho_{c,T}(t) = \left[V_T + R_T i^{\alpha}(t)\right] i(t) \tag{12}$$

$$\rho_{c,D}(t) = \left[V_D + R_D i(t)\right] i(t) \tag{13}$$

where $\rho_{c,T}(t)$ and $\rho_{c,D}(t)$ denote respectively the instantaneous conduction losses of the transistor device and diode. V_T and V_D are the ON-state voltage drops, while R_T and R_D are the equivalent ON-state resistances of the transistor device and diode, respectively, and α is a constant governed by the transistor characteristics.

The conducting switches need to carry the output current $i_{a,b,c(t)}$ at a given instant of time. Both, transistor device and diode of a given switch conducts since all switches are bidirectional. Now, at any instant of time, let $N(t)$ be the number of conducting switches (i.e. diodes and transistor devices). Then, the average conduction losses can be expressed, by using equations (12) and (13), as

$$\rho_{c,avg} = \frac{1}{\pi}\int_0^{\pi} \left[\{N(t)V_T + N(t)V_D\} i_{a,b,c}(t) + \left\{N(t)R_T i_{a,b,c}^{\alpha+1}(t)\right\} + \left\{N(t) i_{a,b,c}^2(t)\right\} d(\omega t) \tag{14}$$

2) Switching Losses: To calculate the total switching losses, a typical switch is first considered, and individual switching losses are then added to obtain the total switching losses of the inverter. To calculate the switching losses of an individual switch, a linear approximation of voltage and current during a switching period (transition from ON state to OFF state and vice versa) is used [28]. Energy losses during turn-on can be calculated as

$$\begin{aligned} E_{on,j} &= \int_0^{t_{on}} v(t) i(t) dt \\ &= \int_0^{t_{on}} \left[\left\{V_{o,j}\frac{t}{t_{on}}\right\}\left\{-\frac{I}{t_{on}}(t - t_{on})\right\}\right] dt \\ &= \frac{1}{6} V_{o,j} I t_{on} \end{aligned} \tag{15}$$

Where

$E_{on,j}$	turn-on loss of the j^{th} switch;
t_{on}	turn-on time;
I	current through the switch after turning on;
$V_{o,j}$	voltage that the j^{th} switch needs to block.

Similarly, energy losses of the j^{th} switch during turning off can be calculated as

$$\begin{aligned} E_{off,j} &= \int_0^{t_{off}} v(t) i(t) dt \\ &= \int_0^{t_{off}} \left[\left\{V_{o,j}\frac{t}{t_{off}}\right\}\left\{-\frac{I^{'}}{t_{off}}(t - t_{off})\right\}\right] dt \\ &= \frac{1}{6} V_{o,j} I t_{off} \end{aligned} \tag{16}$$

where t_{off} is the turn-off time for the j^{th} switch and $I^{'}$ is the current through the switch before turning off. In 1 s, the j^{th} switch makes f_j number of transitions, where f_j is its switching frequency. Hence, by assuming that $I = I^{'}$, the total switching power losses can be calculated as

$$\rho_s = \sum_{j=1}^{2n^2+2n} \left[\frac{1}{6} V_{o,j} I \left(t_{on} + t_{off}\right) f_j\right] \tag{17}$$

In Section V, eq. (17) is used to demonstrate that the proposed topology incurs lower switching losses as compared to the classical CHB topology for a six-level PWM output. The total inverter losses can now be obtained by using (14) and (17) as

$$\rho_{losses} = \rho_{c,avg} + \rho_s \tag{18}$$

C. Optimized control parameters

1) Fourier analysis: To optimize the THD of the output phase-to-phase voltage waveform, pulse weight and height modulation PWHM technique is used. Heights (magnitudes -"E_1,E_2") and widths (angles - "α_1, α_2") of the output waveform are calculated in order to cancel the maximum number of harmonics and optimize the THD (Fig.9).

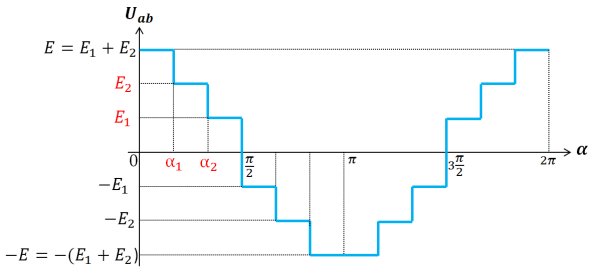

Fig. 9. Six-level output phase-to-phase voltage waveform

Equation 19 gives the Fourier coefficients of the phase-to-phase voltage U_{ab}.

$$\forall k \in N, \begin{cases} a_k = \frac{2}{\pi}\int_0^{\pi} U_{ab} cos(k\alpha) d\alpha \\ b_k = 0 \end{cases} \quad (19)$$

The three phase-to-phase voltages (U_{ab}, U_{bc}, U_{ca}) are assumed to have the same symmetrical properties as an ideal three phase voltage system. Antisymmetric properties with respect to $\frac{\pi}{2}\left[u_{ab}(\frac{\pi}{2}+\alpha) = -u_{ab}(\frac{\pi}{2}-\alpha)\right]$ allows to cancel all even order harmonics. By using different symmetrical properties, $\alpha_2 = \frac{\pi}{3}$ is obtained and the phase-to-phase voltage Fourier coefficients can be expressed in the interval $\left[0, \frac{\pi}{3}\right]$ as given by (20)

$$a_{k=2p+1} = \frac{8}{\pi} cos(k\frac{\pi}{6}) \int_0^{\frac{\pi}{3}} U_{ab} cos(k(\frac{\pi}{6}+\alpha)) d\alpha \quad (20)$$

By using $k=3(2p+1)$, $cos(k\frac{\pi}{6}) = cos\left[(2p+1).(\frac{\pi}{2})\right] = 0$ is obtained. This means that all even and multiple of three order harmonics are canceled.

The remaining non-canceled harmonics are of order $6q \pm 1$. Eq.20 shows that setting the value of U_{ab} is possible only within the interval $\left[0, \frac{\pi}{3}\right]$. The symmetry property of an ideal three-phase voltage system allows us to determine the value of U_{ab} over the interval $[0, 2\pi]$. So, the next analysis will be limited within the interval $\left[0, \frac{\pi}{3}\right]$.

The phase-to-phase voltage U_{ab} is assumed to have two DC levels $(E,\ E_2)$ within the interval $\left[0, \frac{\pi}{3}\right]$ as illustrated in Fig.10. U_{ab} is assumed to have two pulses. The first pulse is of height (amplitude) E and width (angle) α_1. The second pulse is of height E_2 and width $(\frac{\pi}{3} - \alpha_1)$. Heights and widths are set to cancel the maximum number of successive harmonics.

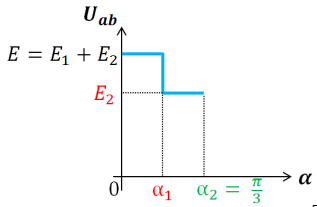

Fig. 10. Phase-to-phase voltage waveform u_{ab} within $\left[0, \frac{\pi}{3}\right]$

By replacing the value of the phase-to-phase voltage U_{ab} as seen in Fig.10 in (20), the Fourier coefficients in this case can be written as:

$$\frac{a_{k=6q\pm1}}{E} = \frac{8}{k\pi} cos(k\frac{\pi}{6}) \left\{(1-r)\, sin\left[k\left(\frac{\pi}{6}+\alpha_1\right)\right] + r\, sin\left[k\left(\frac{\pi}{6}+\frac{\pi}{3}\right)\right] - sin\left(k\frac{\pi}{6}\right)\right\} \quad (21)$$

Where, $r = \frac{E_2}{E}$ is the ratio of the two DC voltage levels and α_1 is the switching angle from E to E_2 . α_1 and r represents the two available adjustable variables. The selection of α_1 and r can be seen in next section i.e. in III-C2.

2) Harmonic elimination technique: Selected harmonics can be eliminated by a proper selection of adjustable variables α_1 and r.

The system of nonlinear equations (see eq.21) can be mathematically solved only if the number of equations corresponds to the number of unknown variables. Since two adjustable variables are available, only two harmonics from (19) can be canceled. It is well known that low order harmonics are the most harmful than the higher order ones. The previous analysis shows that among low-order harmonics (less than 10^{th}), only harmonics of 5^{th} and 7^{th} order are not canceled. They are eliminated only if the condition (22) is fulfilled.

$$\begin{cases} \frac{a_5}{E} = 0 \\ \frac{a_7}{E} = 0 \end{cases} \quad (22)$$

In such case, the first non-zero harmonics is the 11^{th} order since $k \in \{1, 11, 13, 17, 19, ..., 6q \pm 1\}$. By combining (21) and (22), a nonlinear system of two equations with two unknowns $(\alpha_1,\ r)$ is obtained.

$$\begin{cases} (1-r)\, sin(5\alpha_1 - \frac{\pi}{6}) + r\, sin(5\frac{\pi}{3}\alpha_1 - \frac{\pi}{6}) = -\frac{1}{2} \\ (1-r)\, sin(7\alpha_1 - \frac{\pi}{6}) + r\, sin(7\frac{\pi}{3}\alpha_1 - \frac{\pi}{6}) = +\frac{1}{2} \end{cases} \quad (23)$$

By solving (23), the values of α_1 and r are:

$$\alpha_1 = \frac{\pi}{6} \quad \text{and} \quad r = \sqrt{3} - 1 \quad (24)$$

Accordingly,

$$\begin{cases} \frac{a_1}{E} = \frac{12}{\pi}(2-\sqrt{3}) = 1.0235 \\ a_{(k=12p-1)} = -\frac{a_1}{k} \text{ and } a_{(k=12p+1)} = \frac{a_1}{k} \\ a_k = 0\ if\ k \neq 12p \pm 1 \end{cases}$$

So, the remaining non-zero harmonic orders are $\{11, 13, 23, 25, 35, 37, 47, 49, ..., 12p\pm1\}$ as illustrated in Fig.11.

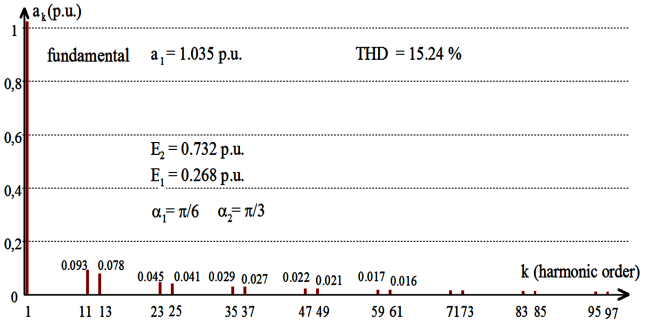

Fig. 11. Harmonics spectrum of U_{ab}

Again, by using symmetry properties of an ideal three-phase system, the output voltages are reconstructed within $\left[\frac{\pi}{3}, 2\pi\right]$ [23]. Fig.12 shows the reconstructed output waveforms of the

modulated output phase-to-phase voltages U_{ab}, U_{bc} *and* U_{ca}. Consequently, a third voltage level E_1 appears in the interval $\left[\frac{\pi}{3}, \frac{\pi}{2}\right]$, with $E_1 = E–E_2$, where

$$E = 1\,p.u.$$
$$E_2 = rE_1 = 0.732\,p.u$$
$$E_1 = E_3 - E_2 = 1 - 0.732 = 0.268\,p.u.$$

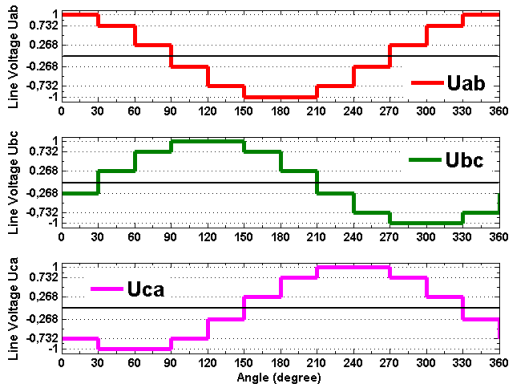

Fig. 12. Three phase six-level output phase-to-phase voltage waveforms

For laboratory practical considerations, two DC supplies are used with E_1=0.268 $p.u.$ and E_2=0.732 $p.u.$ The benefit of the proposed topology is that the first DC level can be obtained easily without extra cost since, E=E_1+E_2=1 $p.u.$ In this case, the obtained fundamental magnitude will be $\frac{a_1}{E_1}$=1.0235 $p.u.$

IV. Simulation and Experimental Validations

To examine the performance of the proposed MLI, simulations are carried out by using Matlab/Simulink and a prototype is implemented based on $dSPACE$ 1-1103 card (Fig.13). The circuit uses twelve bidirectional power switches $S_{11}, S_{12}, S_{13}, S_{21}$, S_{22}, S_{23} fed by $E_1$and $S_{31}, S_{32}, S_{33}, S_{41}$, S_{42}, S_{43} fed by E_2. The power IGBT module from $SEMIKRON: SKM145–GB123D$, with built-in freewheeling diodes $(1200V, 100A)$ is used. From (2), a twelve-gate driver board is built using opto-couplers $CNY17–4$. The DC voltage inputs of the topology were provided by laboratory regulated DC voltage supplies to emulate renewable energy sources (Wind or Solar).

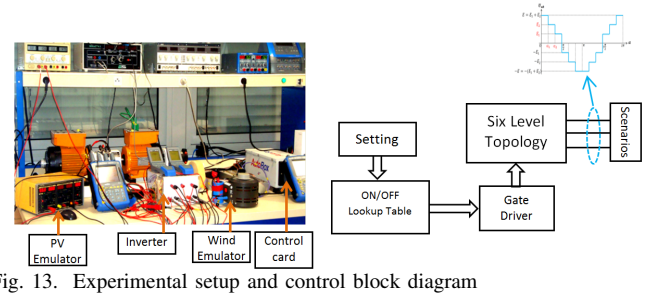

Fig. 13. Experimental setup and control block diagram

A. Simulation results

The r.m.s value can be calculated from within 0 to $\frac{T}{4}$, where T is the period of the signal (25).

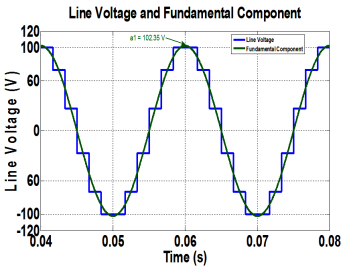

Fig. 14. Inverter phase-to-phase output voltage and its fundamental

$$U=\sqrt{\frac{4}{T}\int_0^{\frac{T}{4}} u_{ab}^2 dt} \quad \Rightarrow \quad U=\sqrt{\frac{4}{T}\frac{T}{12}(E_1^2+E_2^2+E^2)} \qquad (25)$$

In this case, E_1=26.8V and E_2=73.2V so E=E_1+E_2=100 V and U=100$\sqrt{\frac{1}{3}(1+0.732^2+0.268^2)}$=73.2 V

The output phase-to-phase voltage where α_1=$\frac{\pi}{6}$ r=$\sqrt{3}$−1 can be seen in Fig.14. The voltage across the power switch can be seen in Fig. 15. To better evaluate the performance of the proposed topology, three simulation scenarios are considered. The different parameters are:E_1=26.8 V , E_2=73.2 V and E=E_2+E_1=100 V. The scenarios consist of feeding a star connected resistive, inductive and grid connected loads.

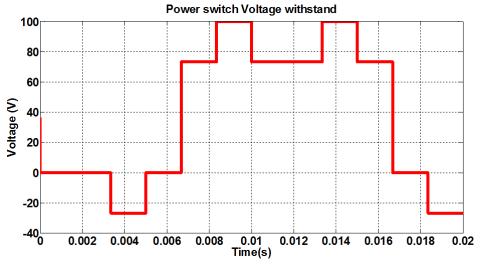

Fig. 15. The voltage across the power switch

1) Scenario 1. Pure resistive star connected load $R = 45\,\Omega$. : In this scenario, star connected power resistor is considered $R = 45\,\Omega$. Fig.16 shows that the line current has the same form as the phase-to-phase voltage because of the load resistive nature. The value of the current THD is 15.24 % where the fundamental magnitude is 0.928 A.

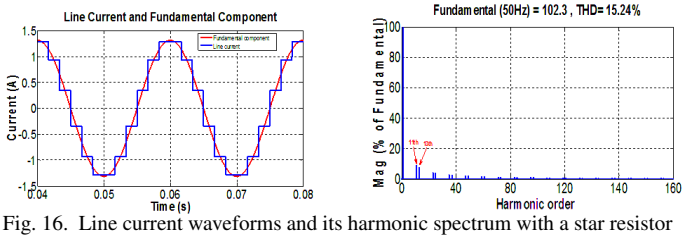

Fig. 16. Line current waveforms and its harmonic spectrum with a star resistor load

2) Scenario 2. Pure inductive star connected load $L = 245\,mH$: In this case, a star connected pure inductive load is considered. Fig.17 shows that the current waveform has almost no harmonics. Also the value of THD in this case is very low $i.e.$ 1.05 % and the first non-zero harmonic order is the 11^{th} with a magnitude of 0.0044 %. The main reason of having very low THD is the inductive load behaving as a low pass filter.

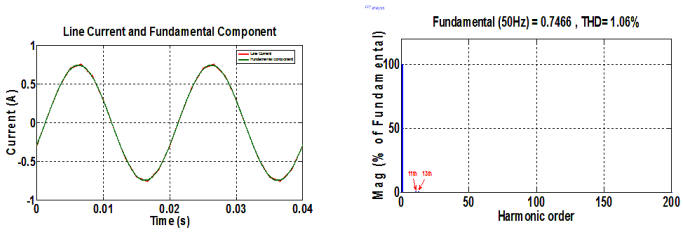

Fig. 17. Line current waveform and harmonic spectrum with an inductive load

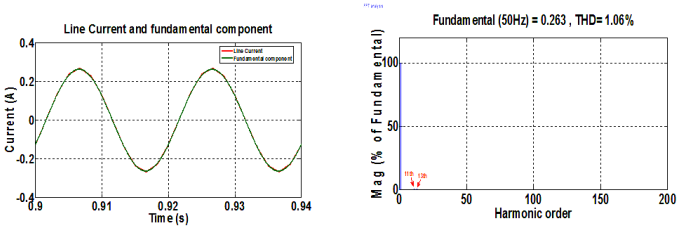

Fig. 18. Line current waveform and harmonic spectrum for grid connection

3) Scenario 3. Inverter connected to the grid : Fig.18 shows the current waveform and harmonic spectrum for scenario 3. In this case, the inverter was connected to the grid. The THD is very low. The results show the capability of the proposed inverter to generate the desired output voltage waveform, the optimized output staircase phase-to-phase voltage is depicted Fig.9, and line current waveforms in Figures 10,11and 12 for resistive load, inductive load and grid connected scenarios respectively. Simulation results demonstrate the effectiveness of the proposed harmonic elimination technique $(i.e.$ selection of α_1 and $r)$. Figures16, 17 and 18 show also the first 100 harmonics (FFT) of line currents for the three different scenarios. The phase-to-phase voltage FFT analysis shows that 5^{th} and 7^{th} harmonics have been eliminated. The first non zero harmonic is of order 11.

B. Experimental verification

The first two simulation scenarios have been verified experimentally while we were not able to experiment the third scenario $(i.e.$ grid connection) because of the non-availability of adequate equipment in the laboratory. Fig. 19 shows the control pulse signal for switches $(S_{11}, S_{12}, S_{13}, S_{21}, S_{22}, S_{23})$ and $(S_{31}, S_{32}, S_{33}, S_{41}, S_{42}, S_{43})$. Each switch has only 4 commutations per fundamental cycle, thus reducing power losses.

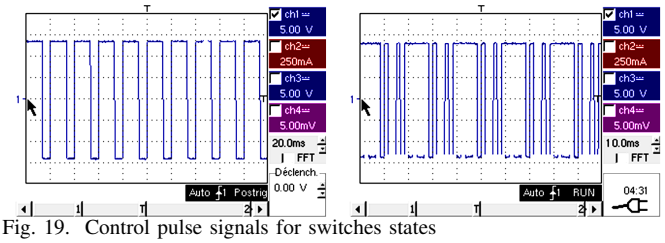

Fig. 19. Control pulse signals for switches states

Each power switch commutes with a frequency equal to $F_{semiconductor}$=$4.F_{fundamental}$, thus switching losses are reduced in comparison with conventional PWM methods.

1) Scenario 1. Pure resistive star connected load $R = 45\,\Omega$: Fig.20 shows the output voltage and current waveform and harmonics spectrum feeding a resistive star connected load . The output voltage is 200 V_{PP} and the output current is 2.7 A_{PP}, the frequency is 50 Hz.

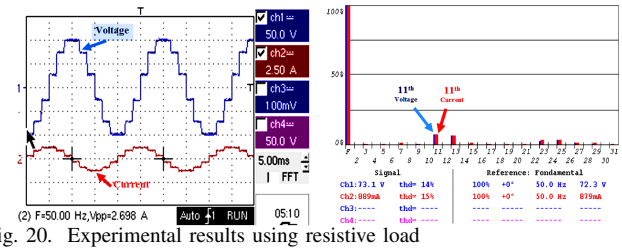

Fig. 20. Experimental results using resistive load

It shows a match between the simulation and experimental results. In fact, both voltage and current harmonic spectra show that the first nonzero harmonic is of 11^{th} order, followed by harmonics of 13^{th}, 23^{th} and the 25^{th} orders.

2) Scenario 2. Pure inductive star connected load $L = 245\,mH$: In the case of inductive load. Fig. 21 illustrates the experimental voltage and current waveforms and harmonic spectrum. The output phase-to-phase voltage is $72.5V$ and the output current is $538mA$. The inductive load cancels the output current harmonic. It behaves as a low pass filter, generating a sinusoidal line current.

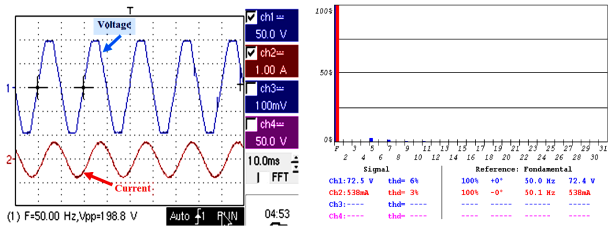

Fig. 21. Experimental results test with inductive load

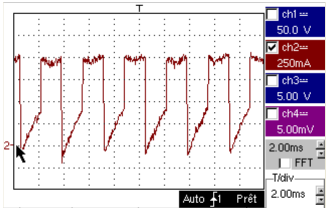

Fig. 22. DC bus current

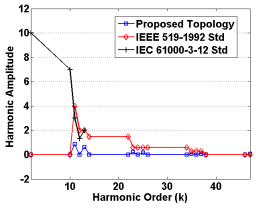

Fig. 23. Inverter waveform compliance with IEEE and IEC standard

Fig.22 shown the evolution of the current over the DC bus.

Fig.20 and Fig.21 show the measured output phase-to-phase voltages, line currents and their frequency spectrum. The output phase-to-phase voltage frequency for all scenarios was 50 Hz with maximal magnitudes equal to E_1+E_2=100 V. The first non-zero harmonic is of 11^{th} order. The output current exhibits a sinusoidal-shape since the load behaves as an RL low pass filter. The output currents contain less high-order harmonics than the output voltages.

TABLE II
COMPONENT REQUIREMENTS AND TOTAL VOLTAGE STRESSES FOR THREE-PHASE MLIS (N IS THE NUMBER OF LEVELS IN PHASE VOLTAGE)

Inverter type / component	NPC	Flying capacitor	Cascaded H-Bridge	Proposed Topology
Number of main switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2N+2\sqrt{2N+4}+4$
Number of main diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2N+2\sqrt{2N+4}+4$
Number of clamping diodes	$3(N-1)(N-2)$	0	0	0
Number of DC bus capacitors / Isolated supplies	$(N-1)$	$(N-1)$	$3(N-1)/2$	$\frac{1}{2}\sqrt{2N+4}$
Number of flying capacitors	0	$(3/2)(N-1)(N-2)$	0	0
Total component count	$(N-1)(3N+7)$	$(1/2)(N-1)(3N+20)$	$27(N-1)/2$	$4N+\frac{9}{2}\sqrt{2N+4}+8$

C. Compliance with IEEE 519-1992 and IEC 61000-3-12 standards

The $IEEE\,519-1992$ and $IEC\,61000-3-12$ standards provide limits for the harmonic currents produced by electrical equipment's [24], [25]. For inductive loads (electric machines, passive filters, transformers), which represent 80% of the power converter applications, the output current harmonic magnitudes are $a_{k(current)} = \frac{a_{k(voltage)}}{k}$, where k is the harmonic order .

Fig. 23 shows clearly the compliance of the proposed six-level inverter output signal with internationally recognized standards. The first nonzero harmonic is the 11^{th} order, meaning that the most harmful harmonics of 5^{th} and 7^{th} orders are canceled along with all even-order harmonics.

V. COMPARISON WITH OTHER TOPOLOGIES

In this section, comparison of the proposed topology is made with other topologies. In Section V-A, the topology is compared with classical topologies in terms of component requirements. In Section V-B, an exclusive and exhaustive comparison is carried out with the CHB topology because, as mentioned earlier, the proposed topology resembles the CHB in configurational and functional features.

A. Overall Comparison With Classical Topologies

The component requirements of various topologies for a three-phase configuration are given in Table-II in terms of the number of voltage levels (N) in the phase-to-phase voltage. It can be inferred from the table that the number of components in the proposed structure is lower than those in other topologies, particularly for higher number of voltage levels. For example, implementing a thirty-level inverter will entail component counts of 2813, 1595, and 391 for the NPC, FC, and CHB topologies, respectively, but only 164 in the proposed topology.

B. Comparative Analysis of the Proposed Topology With the CHB Topology

In this section, a comparison between the proposed inverter and CHB inverter is carried out in terms of voltage level and power component requirements and switching losses. For the purpose of comparison, both topologies are configured such that both have equal number of dc sources as input. Thus, with "n" number of sources, each equal to V_{dc} for CHB topology and E_1 and E_2 for the proposed topology (see Fig.2), the number of levels is given by (5) for the proposed topology and $2n+1$ for CHB topology [26], [27], and the maximum output voltage attained is given by (6) for the proposed topology and $n\,V_{dc}$ for CHB topology [28].

Voltage levels and power switch Requirements: With "n" number of dc sources, the CHB topology provides "$2n+1$" voltage levels, while the proposed topology provides "$2n^2-2$" voltage levels. The difference in the numbers of voltage levels is significantly large. For example, for a three-phase 30-level voltage, a CHB inverter requires 14 dc sources and 174 power switches, whereas the proposed topology needs only 4 dc sources and 80 power switches.

Switching Losses: With an appropriate switching control, the proposed topology can be implemented with lower switching losses as compared to the CHB topology. For a five-level inverter with two equal input dc sources of voltage V_{dc} for the CHB topology and the six level inverter with dc sources of voltage E_1 and E_2 for the proposed topology (see Fig.2), such as $E_1+E_2=2.V_{dc}$, the average switching power loss ρ_s in the switch caused by switching transitions can be defined by using (17) as

$$\rho_s = \frac{1}{6}V_0 I_0(t_{on}+t_{off}).\, f \tag{26}$$

where t_{on} and t_{off} are the turn-on and turn-off crossover intervals, respectively, V_o is the voltage blocked by the switch, I_o is the switch current, and f is the switching frequency. For simplification, it is assumed that switches operate with the same t_{on} and t_{off} values while they carry the same current I_o. Thus, ρs can be approximated as

$$\rho_s = \zeta V_0 f \tag{27}$$

where ζ $[=\frac{1}{6}I_o(t_{on}+t_{off})]$is a constant. Thus, switching power losses in the CHB five-level inverter in which all twenty-four switches operate at a high switching frequency ($f_s \geqq 21.f_0$, based on carrier signals, f_0 is the fundamental frequency) while blocking the same voltage V_{dc} can be averaged as

$$\rho_{s,CHB/5L} = 24\zeta V_{dc} f_s = 504\zeta V_{dc} f_0 \tag{28}$$

Similarly, the switching power losses of the proposed six-level inverter with twenty-four switches operating at low switching frequency ($f_s = 4.f_0$, since each switch commutes fourth's time per period in six level topology as depicted in section-III-A while blocking the dc voltage E_1 and E_2 corresponding for each switch can be obtained as

$$\rho_{s,proposed/6L} = 12\zeta E_1 f_s + 12\zeta E_2 f_s = 192\zeta V_{dc} f_0 \quad (29)$$

While $E_1 + E_2 = 2.V_{dc}$.

It is clear from (28) and (29) that, the switching losses incurred in the proposed topology are almost half the switching losses incurred in the CHB topology.

VI. Conclusion

The proposed multilevel inverter topology can be a good solution to feed microgrid from renewable energy sources. A six-level inverter was considered and controlled by using a PWHM technique, requiring only twelve switching states per period. Simulation studies have been performed on a six-level inverter based on the proposed structure and have been validated experimentally. The obtained simulation and experimental results have shown a $15\,\%$ voltage THD rate, zeroed successive harmonics from 2^{th} to 10^{th} orders. The first non-canceled harmonic is 11^{th} order with $9\,\%$ of the fundamental magnitude. The proposed configuration gives a compact and low cost system with both minimum number of switches and less number of switching states with a simplified inverter control scheme. The efficiency, performance and compliance with $IEEE519-1992$ and $IEC61000-3-12$ standards have been validated. The low-frequency switching reduces the inverter power losses leading to a better efficiency of the proposed topology. Comparisons of the proposed topology with conventional topologies reveals that the proposed topology significantly reduces the number of power switches and associated gate driver circuits. Analytical comparisons on the basis of losses indicate that the proposed topology is highly competitive. On the horizon, the detailed real and reactive power control of the proposed inverter will be considered.

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