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► **To cite this version:**

Ousseynou Yade, Christian Martin, Christian Vollaire, Arnaud Bréard, Marwan Ali, et al.. Improved Layout of Inverter for EMC Analysis. More Electrical Aircraft (MEA), Feb 2017, Bordeaux, France. hal-01715021

**HAL Id: hal-01715021**

**<https://hal.science/hal-01715021v1>**

Submitted on 22 Feb 2018

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# Improved Layout of Inverter for EMC Analysis

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## Abstract

This paper details EMC (electromagnetic compatibility) analysis on an inverter application. The work deals with the whole power chain ( $\pm 270\text{Vdc}$  input voltage to 3-phase 115 Vac output voltage). This inverter is composed by modular parts (power module and EMC filters) that supply motors in more electrical aircraft. Through our analysis an approach is defined to design a detailed lumped circuit model of the power module layout by using Q3D extractor and SABER software. From this first step, the power module layout design is improved by reduced parasitic impedances at high frequency (around 30 MHz). Then whole power converter is modeled in SABER by including switches (SiC MOSFET models), LISN (line impedance stabilization network), harness, and load models.

## I Introduction

The more electrical aircraft aims to offer many benefits [1]. On the one hand, it reduces operating costs, fuel consumption and the environmental impact of the future air travel. On the other hand, the use of electrical equipment leads to advantages in terms of maintenance, power control and efficiency [2], [3]. Thanks to this concept, electrical systems should substitute conventional power sources used in aircraft. As a result, they take a significant part of the total aircraft mass. Among these systems, there are power electronic converters that control actuator energy. Different efforts are made in order to improve power electronic converter efficiency by considering new semiconductor technologies (GaN, SiC ...). These efforts also allow to increase switching frequency and, operating temperature in the way to reduce passive components and cooling requirements. Within the scope of the EU research and innovation program Horizon2020 [4], the I<sup>2</sup>MPECT project [5] aims to bridge this gap and create synergies for the aircraft industry with other industries. The goals of the I<sup>2</sup>MPECT project are the following:

- Increase efficiency, power density of power electronic conversion systems through the use of wide band gap devices and innovative cooling technology.
- Increase reliability and efficiency by use of advanced packaging and thermal management solutions.
- Enable reduced maintenance cost and increase availability by employing health-monitoring techniques.
- Reduce qualification and certification cost through the availability of modularized power electronic modules.

The I<sup>2</sup>MPECT project aims to demonstrate these achievements with a 45 kW 3-phase bidirectional DC-AC power converter featuring a power to weight ratio

of 15 kW/kg at an efficiency of 99% for the power electronics core component.

In this project the use of SiC MOSFET should make possible to increase switching frequency to reduce passive components size. However, high switching frequency implies EM (ElectroMagnetic) disturbances that must be taken into account in the design phase. This paper presents detailed lumped circuit model of the advanced layouts of the inverter by combining both Q3D extractor (3D EM Simulator) and SABER software (Electrical Circuit Simulator). This approach allows analysing the distribution of impedances through these layouts and act to improve layout design in order to decrease stray inductance at high frequency. The coupling between Q3D and SABER allows simulating the whole system (layout model, active component model (MOSFET), control part, LISN ...).

Section II explains the importance of detailed lumped circuit model for EMC analysis. In section III, the simulation approach and layout design improvement are described. The simulation results are summarized in section IV. A conclusion and perspectives are given in section V.

## II Simulation approach of layout circuit model

To analyse EM disturbances and design EMC filters, it's necessary to model the whole power converter in order to get EM signatures. There are two main approaches to get simulation model: the first one is behavioural modelling approach [6] which is suitable when there are no details about inverter layout and it requires few computational time. However, since there is no information about impedance distribution, it is not possible to correlate EM disturbances to the layout. As a result, this technique cannot be used to improve layout. The second one is a detailed lumped circuit modelling approach based on the physics of the circuit. It is the classical way to model any electronic circuit. The interconnections like wires and printed circuit board (PCB) traces are modelled using

passive RLC equivalent circuit or impedance matrix [7]. Other passive components like resistors, capacitors and inductors can be directly measured using an impedance analyser. The equivalent circuit models for the PCBs are usually extracted by electromagnetic numerical tools like Q3D extractor [8], [9]. The main benefits of lumped circuit models are accuracy, adaptability and scalability as everything is based on physics. However, it requires more large computational resources and time to simulate precisely the full model.

Stray impedances are extracted by using Q3D software. It can provide RLC elements with the same solver by combining finite element method and the method of moments. Typical power module layout designed for this project is shown in fig .2. The control pins are designed on a PCB flex and there are no bondings on the power part. This power module is composed of two main parts:

- The power part which generates the main part of the parasitic impedance. Depending on the power module version, it is composed by (at least) two MOSFETs SiC per switch, shunt resistors for currents sources measurements, DC link connection and output phase.
- The control and measurement part on PCB flex above the power part with temperature sensor (NTC), shunt resistor and gate control.

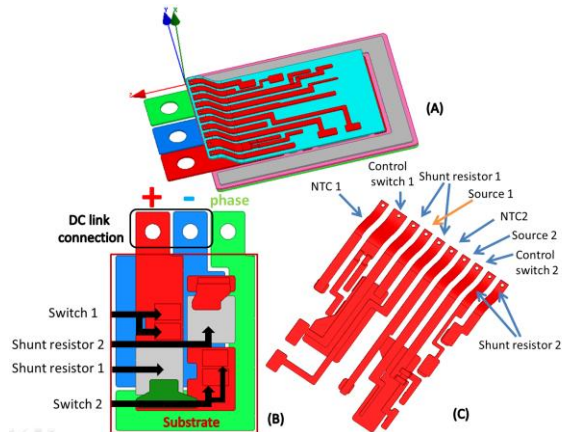


Fig .2 inverter layout for “one phase” leg (A), power part (B), control and measurement part (C)

After imported or built layout on Q3D extractor, Simulation procedure is launched and parasitic impedance behavior can be computed and analyzed. To build electrical model, Q3D extractor provide us a “.cir” file which include all parasitic impedance values for one frequency. These parasitic impedances are then converted as electrical model in order to embed it on saber platform. Fig.3 shows the extraction process that allows building circuit model of the power module layout.

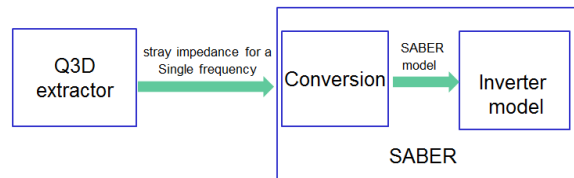


Fig.3 translation procedure from Q3D extractor to SABER software

The loop inductance plays an important role in the switching phase. An evaluation of this stray inductance has been performed. As shown in fig.2.B, the stray inductance is induced by DC link connection and substrate. Simulations have shown that the DC link takes around 50% of the total stray inductance. Table 1 shows stray inductance for both DC link connection and substrate. The loop inductance of the switching cell is the sum of both values (around 9.1 nH). As substrate dimension is imposed by SiC chip location and thermal criteria, it is difficult to change the form of the substrate. As conclusion, the modification of the DC link seems to be a good way to reduce the total loop inductance.

	DC link	Substrate
<b>Stray inductance (nH)</b>	4.3	4.8

Table 1 stray inductance of the two main part of the power part

A geometrical modification of the DC link allows to reduce this stray inductance by choosing parallel plate overlap as DC link structure (fig.5) [10]. This improved design allows reducing stray inductance around 50% as shown in Table 2 (L change from 9.1nH to 5.37nH). This part will be detailed in the full paper.

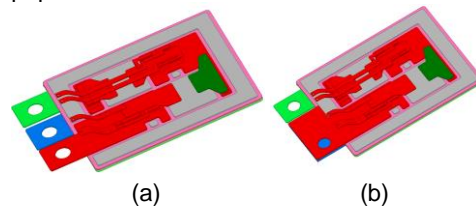


Fig.5 original layout (a) improved layout (b)

	Loop inductance(nH)	Reduction (%)
<b>Original layout</b>	9.1	0
<b>Improved layout</b>	5.37	47

Table 2 stray impedance reduction

### III Circuit model and simulation results

In order to evaluate this improved layout, its EM signature is compared to original layout one. Fig.6 shows electrical circuit model used to extracted EM signature and Table 3 summarizes passive components and DC fed values. By associating coupling capacitor to the power module layout, the

differential impedance seen between switching cells is lower with the improved layout than with original (for 5 dB). That's mean differential mode disturbances provided by inverter to DC side decreases to 5 dB $\mu$ A. This improvement is available from 700 kHz to higher frequencies as shown in Fig.7. It also contributes to

increase cut-off frequency of the further EMI filters and to reduce passive components value required to mitigate EM disturbances seen from DC side. Common mode impedance measurements will be done by including common mode parasitic capacitor and analyse impedance between ground and DC link.

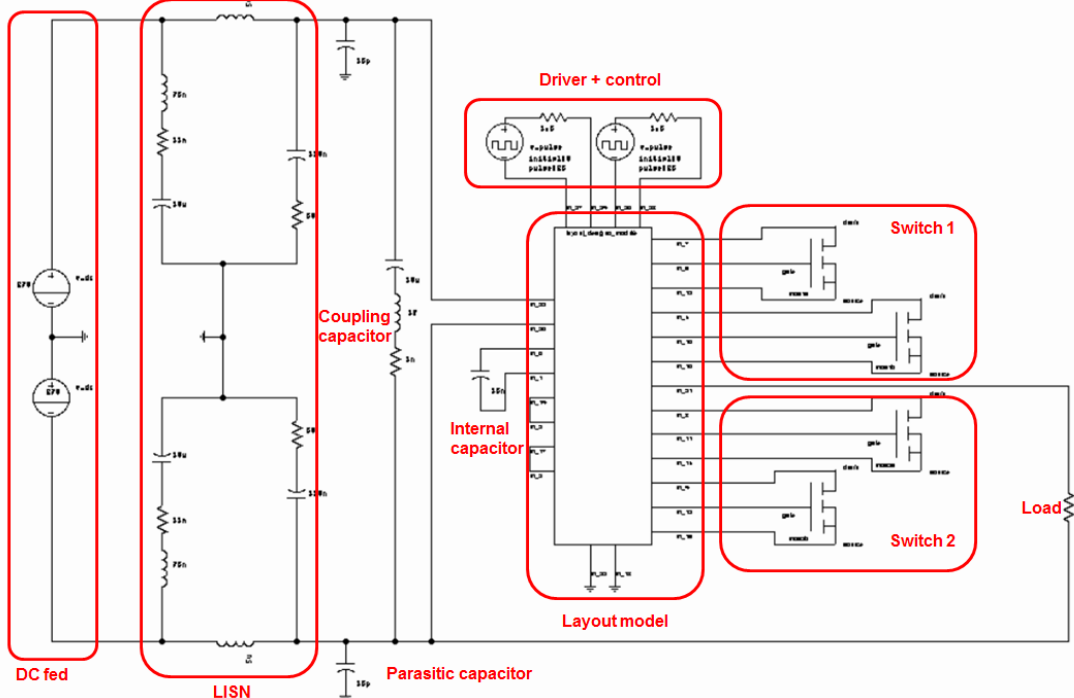


Fig.6 circuit model to extract EM signature

	Value
<b>DC fed</b>	$\pm 270$ V
<b>Coupling capacitor</b>	10 $\mu$ F
<b>Internal capacitor</b>	15nF
<b>Parasitic capacitor</b>	15pF
<b>Load</b>	8 $\Omega$

Table 2 stray impedance reduction

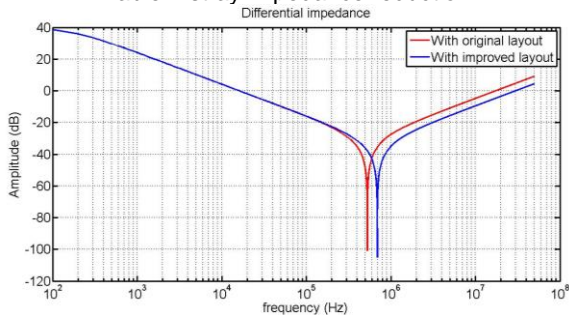


Fig.7 Differential impedance seen from switching cells

Fig.8 shows the novel layout design with three MOSFETs per switch in order to reduce stress current through each MOSFET. This design will be embedded as power module in the whole converter with separate parts: LISN, harness, motor and SiC MOSFETs. A three phases pulse width modulation is used with 15 kHz as switching frequency and 100 Hz as output phase frequency. This power module is supplied by a DC fed with  $\pm 270$  Vdc input voltage.

The LISN is defined by DO-160 standard. Electrical coupling capacitor model is built as an RLC model the capacitor value is 30  $\mu$ F. The model is based on SPICE level1 MOSFET model with channel mobility modulation effect (level 3) [11] [12]. As load, a 15 kW R-L model is used for proof of concept of our design approach. This model can be applied for higher load values (45 kW).

This circuit model allows analyzing conducted EM disturbances from each part of inverter layout. Fig.9 shows EM disturbances seen from DC side for 15 kW (input voltage  $\pm 270$  V and current load 30 A). Current and voltage slopes during the switching phase reach 2.577 kA/ $\mu$ s and 12.591 kV/ $\mu$ s respectively.

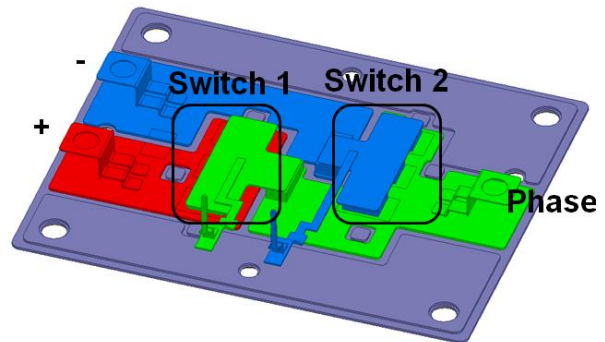


Fig.8 power module embedded in the inverter

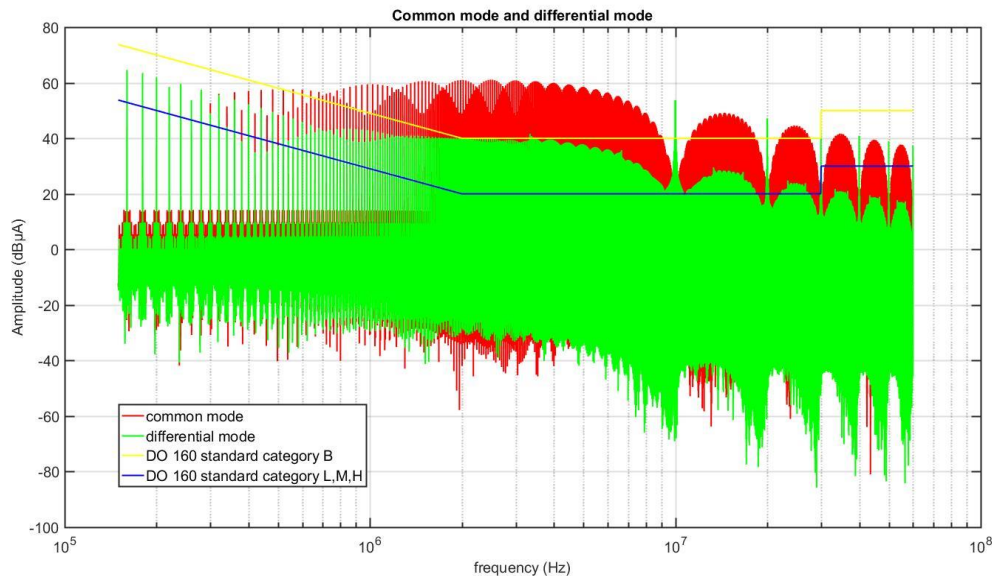


Fig.9 EM disturbances seen from DC side

## V Conclusions

This paper summarizes detailed lumped circuit model technique applied on advanced inverter layout model. In order to reduce stray impedances, it's necessary to overlap DC link. This approach is accessed by comparing provided results to experimental measurements. Time domain simulations are also accessed through current waveforms and slope during switching phase for the whole converter. For further works EM disturbances will be identified and mitigated through passive EMI for DC and AC side.

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