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SiC JFETs may have the lowest overall losses of switching devices and can operate at temperatures over 400°C. Over different junction field-effect transistor (JFET) designs the trenched and implanted (TI) gate vertical JFET (TI-VJFET) is very attractive since it may have the lowest on-resistance and its fabrication does not require epitaxial overgrowth or multiple angled implantation. 4H–SiC TI-VJFETs have been fabricated with self-aligned nickel silicide source and gate contacts using a process sequence that greatly reduces process complexity as it includes only four lithography steps. Different design factors, including channel width, channel length, and mesa height, are considered. The effect of the channel geometry on the electrical characteristics has been studied by varying their width (1.5-5μm). The specific ON resistance (R_{ON}) of the fabricated devices, at V_{GS}=0V, varied from 12.5 to 6.2 mΩ·cm^2 with increasing the channel width. The effect of the channel width was more tremendous on the breakdown voltage of the transistors passing from 80 V to 500 V showing the importance of the static-induction effect (saddle point potential influenced by drain potential) on the transistor blocking characteristics. Indeed, the blocking voltage gain is varying from 50 to single digit values when increasing the channel width. The physical reason is that the blocking gain to first order depends exponentially on the channel dimensions as the drain-source current is exponentially related to the saddle point potential.

1 Introduction

Power transistors based on wide band gap semiconductors are subject of intensive research during the last decade. The high current and high voltage capabilities of these devices, largely exceeding that of Si counterparts, represent a challenge on various aspects related to the device fabrication, characterization and packaging [1]. Currently, SiC is the wide band gap semiconductor material of choice for fabricating high power devices. Particularly SiC, when compared to silicon, has three times wider bandgap (E_g), ten times higher critical electric field (E_c), nineteen orders of magnitude lower intrinsic carrier concentration (n_i), three times larger thermal conductivity (λ) and higher saturation velocity (v_{sat}). These characteristics show great potential to make power devices that can operate at higher power, higher temperature and higher frequency with lower leakage current, smaller conduction and switching losses, less stringent requirements in heat removal.

In recent years, numerous SiC high power switching devices such as Schottky barrier diodes (SBDs), metal–oxide–semiconductor field-effect transistors (MOSFETs), junction field-effect transistors JFETs), bipolar junction transistors (BJTs), and insulated gate bipolar transistors (IGBTs) have been demonstrated and some of them have already entered successfully the commercial market.

All things considered, the MOSFET is the most promising device in the SiC field. Its technology is more mature and it is a normally-off device with little demand on the drive circuits. However, reliability issues (oxide and threshold voltage stability) still exist despite the long and important effort devoted. The SiC BJT main advantages as power switch are its low conduction loss combined with fast switching. Moreover, BJTs are generally very robust devices. The most crucial parameter for SiC BJT optimization is to increase the current gain at application temperature. This has been addressed by performing special surface passivation based mainly on oxides, which obviously

is subject to reliability issues related to the passivating oxides.

SiC JFETs, having no interface issues, can fully benefit from the superior properties of SiC. They have the lowest overall losses of switching devices and their fabrication process is characterized by its simplicity. Moreover, JFETs are very robust devices with a channel not largely affected from surface effects. The main drawback with VJFETs is that they are usually normally-on (depletion mode), which is considered unsafe in power applications. For these reasons, SiC JFETs have been chosen to be developed aiming specific applications such as high-temperature and space-related ones.

There are many possibilities in terms of JFET geometry and most of them have been investigated in the case of SiC [2, 3]. The usual 4H-SiC JFETs are either purely vertical (VJFETs) [**Erreur ! Signet non défini.**, 4, 5] or semi-lateral (SLJFET) [6]. Optimum SLJFET fabrication requires many step implantation and/or re-epitaxial growth after material etching on specific locations. The vertical trenched VJFETs require only one implantation step and a smaller number of lithography steps [7]. The only difficulty is the tight control of the dimensions, which are of the order of 1-2 μm for both source pillars and gate pitch resulting, thus, in an issue of tight registry control. Indeed, different lithographic approaches, metallization schemes, isolation dielectrics and gate implantation conditions have been tested in previous experiments. [8, 9]. This effort resulted in the fabrication of SiC TI-VJFET with self-aligned nickel silicide source and gate contacts using a process sequence that greatly reduces process complexity as it includes only four lithography steps. In the present paper, the effect of design factors including channel width, channel length, and mesa height, are investigated with the fabrication of VJFETs that combine different values of these parameters.

The device structure and the fabrication process of the transistors employed in the present study is first exposed followed by their electrical characterization results. Note that in the previous reports [8, 9], the fully optimized process employed for the last fabricated transistors employed in the present study is not included. An analysis of the characterization results is performed to extract the conclusion on which optimized structures according to the targeted application can be designed.

2 Device structure and fabrication

The cross-section of the fabricated 4H-SiC TI-VJFETs is shown in Fig. 1. A series of optimization runs have been performed in order to choose this optimized structure [8, 9]. Different epitaxial structures and gate implantation geometries were used [9]. For the transistors of the present study, the epitaxial structure on the top of the n^+ 4H-SiC wafer was composed by a 8 μm (L_{dr}) blocking thick n-layer with $N_d=5\times10^{15}$ cm^{-3}, an 1.2μm ($L_{ch}+L_{Pchan}$) channel layer n-layer with $N_d=1\times10^{16}$ cm^{-3} and a top 1μm (L_{Pcont}) thick n^+ layer with $N_d=1\times10^{19}cm^{-3}$. Gate regions were formed by local Al ion implantation and post-implantation annealing resulting in an implanted region with p-type doping of $1\times10^{19}cm^{-3}$. Two different configurations have been employed for the fabrication of 4H-SiC TI-VJFETs. The main differentiation between these two configurations is the implantation depth which is equal to L_G=0.65μm in the first and 1.75μm in the second one respectively. The two transistor types will be distinguished by mentioning them as the "short" (0.65μm) and "long" (1.75μm) channel VJFET. The mentioned values of gate length correspond to the depths where the Al chemical concentration, as measured by Secondary Ion Mass Spectroscopy (SIMS) measurements, is equal to the background n-type dopant density. This assumes a high electrical activation of Al implanted atoms and this assumption is based on the Scanning electron Microscopy (SEM) image contrast from cross-section of the completed devices (Fig.2).

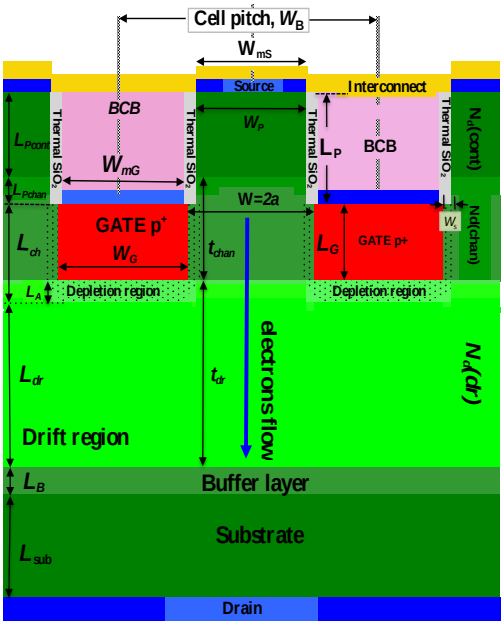


Figure 1. Schematic of the device cross-section.

A second differentiation in fabricated device geometry is on the mesa height (L_{Pcont} +L_{Pchan}) namely the depth of the etched trench for the Al implantation and the formation of the gate regions. The mesa height equals to 2.5μm for the "short" channel transistors while for the long ones, it is equal to 2μm.

Source fingers and gate trenches were formed by reactive ion etching (RIE) by using the first lithographic step. Devices with different channel widths (1.5, 2, 2.5, 3, 4 and 5μm) according to the lithography mask have been fabricated. The same multilayer metal mask was used to perform the above patterning by RIE etching and to form gate regions by ion implantation. Aluminium was implanted at temperature of 425 °C with normally incident ion beam (sample's surface and ion beam are perpendicular). Individual implantation energies and

fluencies were calculated using the SRIM 2D simulation program to form the Al profile. The ion implantation was followed by a thermal annealing at 1600-1800ºC. The gate profile has been checked by Secondary Ion Mass Spectroscopy (SIMS) performed on as-implanted and as-post-implantation-annealed witness samples. A significant lateral straggling has been observed in long device (Fig. 2).

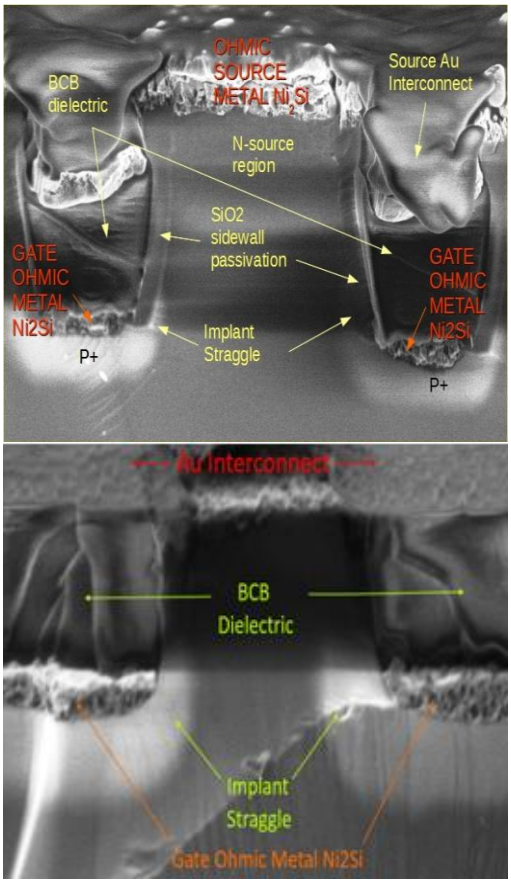


Figure 2. SEM micrographs showing cross sectional views of the completed "short" (top) and "long" (bottom) devices.

A study on optimum gate-source isolation showed the necessity of a dielectric layer on the sidewalls of the source pillars. The samples were, thus, oxidized to form a 35 nm thick oxide on the Si-face and a 240 nm thick oxide on mesa-structure sidewalls. The thick oxide film grown on the sidewalls consumes unintentionally Al-doped source-finger-sidewalls and prevents formation of a leaky gate-source p^+-n^+ SiC junction. The oxide from the Si-face was removed subsequently by anisotropic RIE.

Following, 50 nm thick Ni contact was deposited by e-beam evaporation in a self-aligned way on the tops of source fingers and in gate trenches. The samples were patterned with photoresist (second photolitho-thography step) to re-remove the metal from the edge termination and device separation regions. A 100 nm thick Ni layer is also deposited on the wafer back-side.

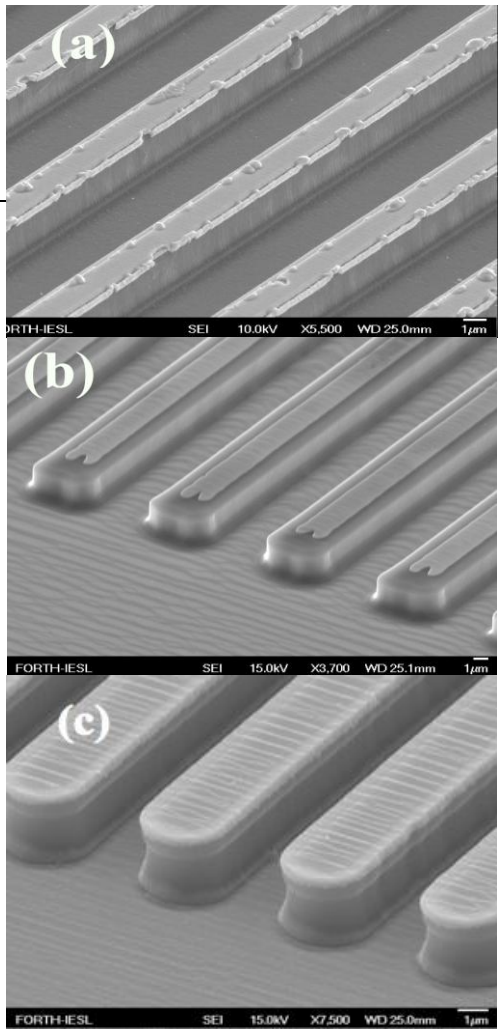


Figure 3. Source pillars after metallization deposition in the case of non-optimized self-aligned (a) conventional-contact-lithography (b) and optimized self-aligned (c) processes.

Although, the technology of 4H-SiC JFETs is simpler than that of MOSFETs or BJTs its main difficulty lies with the small width (~1μm) of the source pillars requiring the use of advanced photolithography equipment (steppers, e-beam lithography) or self-aligned approach in the case of contact lithography. Indeed, using a more conventional approach based on different lithographic steps for source and gate metal contacts was possible only for source widths higher than 3 μm (Fig.3(b)). The main issue in the case of the self-aligned process is related to the metal tears and wings, which should be avoided in order to have a large gate-source breakdown. In the case of Fig. 3(a) these features are not excessive but a study, relative to the use of different photoresist, allowed eliminating them completely (Fig. 3(c)). Fig. 3(c) shows the technology of the optimized metallizations formed by a "salicidation-like" process [10], which allows removing the metal from the areas close to the source finger edges. The contact annealing has been performed in two steps (750ºC and 1000ºC) in vacuum and the morphology of the annealed contacts is shown in Fig.4a.

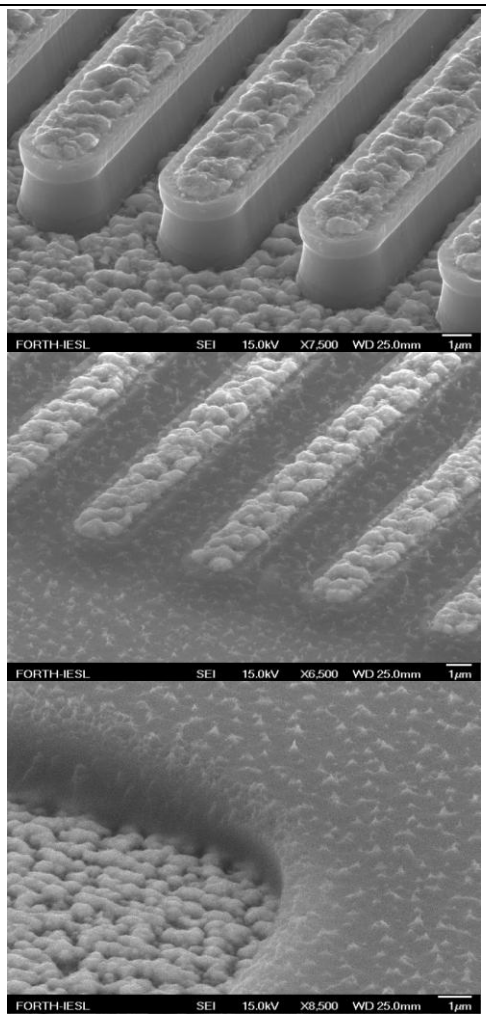


Figure 4. SEM images taken (top) after RTA at 1000ºC, (middle) after BCB deposition and etch-back from the source fingers and (bottom) after 2nd etch-back on the gate pad.

The next process step was the application of a trench filling dielectric (cyclotene[c]), its curing and etching-back to expose the mesa-structure tops with source contacts. The usefulness of this step is two fold. First, to planarize the source pillar tops for interconnecting them by a metal deposition. Second, to avoid any short between the source and the gate. Benzocyclobutene (BCB or simply cyclotene) has been employed for this task as it has excellent dielectric and planarization properties in comparison to other dielectrics such as the polyimide. The BCB film was deposited all-over the surface by spin coating and it is much thicker than the height of the source pillars. It was etched-back down to the source finger tops (Fig. 4b) with reactive-ion-etching (RIE) in pure SF_6.

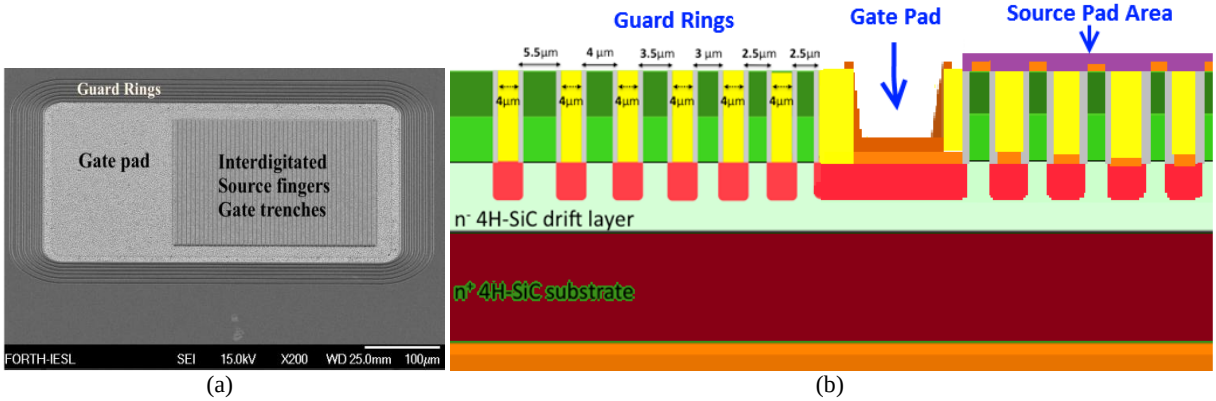
Then, the third lithography step was performed followed by RIE to open the gate pad contacts (Fig. 4c).

Finally, the final fourth lithographic step was employed for depositing and patterning the common source and gate pad Ni/Au metal overlay (Fig. 5). The edge termination was provided by a self-aligned multiple floating-guard-ring structure shown in Fig.5.

The "real" channel widths and guard rings trenches widths can be determined from SEM observations of the completed devices cross-section similar to that shown in Fig. 2 (hereby mentioned "SEM_1") but also from the surface plane views similar to that shown in Figs 3-4 (hereby mentioned "SEM_2"). It has been observed that the short channel devices exhibit a constant augmentation of about 1μm while for the long channel devices despite of the use of the same mask layout, the formatted channel widths seem to be equal to the nominal ones due to the implantation straggling effect which has been observed.

3 Device characterization and results

The fabricated devices were characterized on-wafer level up to 200V by using a Keithley 4200 semiconductor parameter analyzer. For the high voltage (>200V) characterization, a curve tracer Tektronix 370A was utilized. The measurements were performed in DC mode, except of the forward conduction characteristics where pulsed mode was utilized in order to avoid the self-heating effect and evalu-



(a) (b)

Figure 5. (a) SEM of the completed device, (b) Schematic of the device cross-section (Dark red:Substrate high n-type SiC, Dark and light green:high and low n-type SiC, red:p-type SiC, yellow:cyclotene, grey:SiO_2, light orange:Ni contact, purple:Au overlay.

ate the maximum current conduction capability of the device. The results are reported for both short and long channel devices, by mentioning the "nominal" values of channel width as determined by the lithography masks and not the "real" ones (see discussion above).

3.1 Transfer I-V characteristics

Figure 6 shows the transfer I-V characteristics of the fabricated devices with different channel widths for both short and long channel devices. During the measurement, the drain voltage was kept constant at 0.1V.

As the channel width increases, more negative gate voltage values are necessary to pinch off the channel and consequently pass to the off state of the device. We also

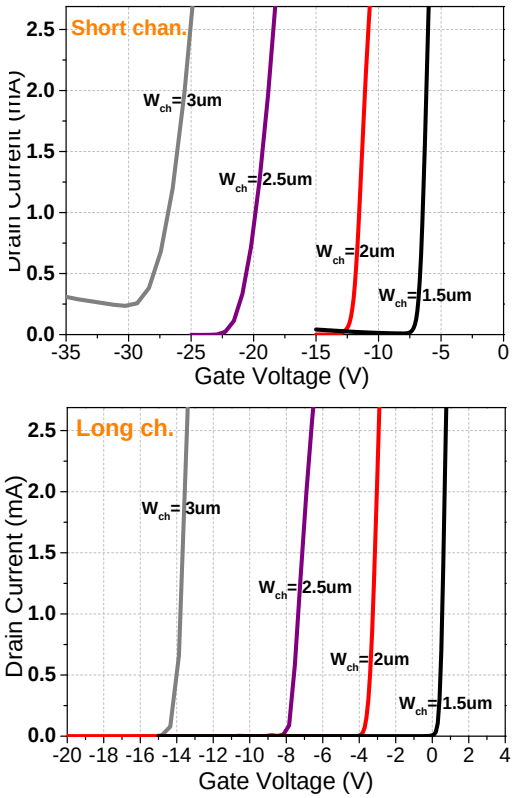


Figure 6. Transfer characteristics at V_{DS}=0.1V of the different channel widths for both short (top) and long (bottom) channel devices.

observe the existence of leakage problem for the short channel devices. The fabrication of normally on or normally-off devices can be achieved by manipulating the channel width. Notice that the desired normally-off behavior is achieved for the narrowest channel width (1.5um) of the long devices.

Figure 7 shows the extracted V_{th} values from the measurements and the theoretically expected curves. More than one theoretical curve are shown trying different doping profiles and channel widths in order to figure out which one is closer to the measured curve. The curves indicated by "SEM" correspond to the above mentioned values "SEM_2". It is worthwhile to mention that the threshold voltage value should not depend on the L_G according to the theory. However, due to the important strangling in the case of deep ion implantation, the effective channel width is reduced in the long channel devices and there is a shift

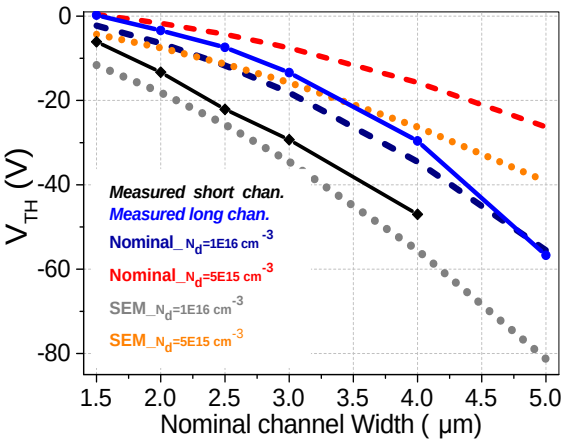


Figure 7. Threshold voltage dependence on channel width.

of the corresponding curve to smaller in absolute value threshold voltage.

3.2 Forward conduction.

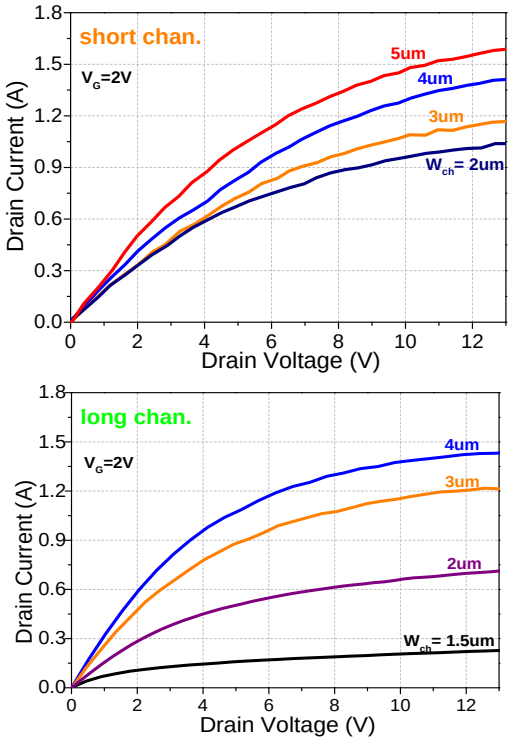


Figure 8. On state I-V characteristics of the different channel width devices (V_{GS}=2V).

Figure 8 shows the output I–V characteristics of the fabricated devices with different channel widths for both short and long channels. The gate has been biased at 2 V

(lower than the built-in potential) to minimise the space charge region of the gate p-n junction and achieve consequently the as wide as possible channel which serves the higher current conduction.

Figure 9 shows the on-state I-V characteristics of transistors of W_{ch}=3 um at different gate voltages ranging from

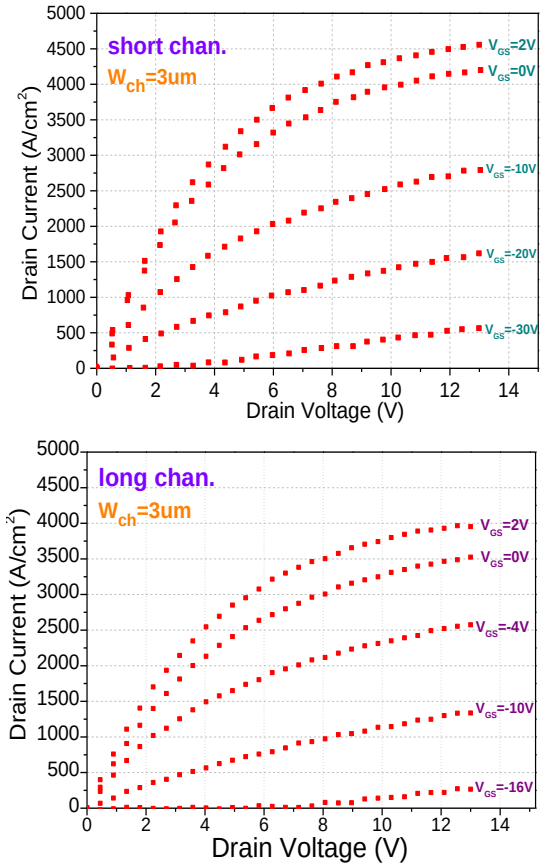


Figure 9. On state I-V characteristics (W_{ch}=3um).

2 V down to threshold voltage value. The satisfactorily high drain current density that is achieved is noticeable. The measurements were performed in pulsed mode to avoid self-heating of the transistors.

We observe that as the L_G increases, the effect of the W_{ch} on the amount of the conducted current becomes greater, namely the control of the current conduction by the V_{GS} is easier. Moreover, it is obvious that the short channel devices can pass greater values of current. This is attributed to the lower channel resistance of them in comparison with the respective long channel ones. Particularly for the narrowest short channel devices, the R_{on} is equal to 6.3mΩ·cm^2 while for the respective long channel ones, it equals to 11.3 mΩ·cm^2.

3.3 Reverse blocking

The reverse blocking test was performed with a curve tracer. The fabricated devices were immersed in Fluorinert™ dielectric liquid to prevent air breakdown.

We observed a clear triode regime of operation due to a static induction voltage-blocking capability induced by short-channel-effects (SCE) often called "Drain Induced Barrier Lowering (DIBL) [**Erreur ! Signet non défini.**].

The good blocking behavior of the long channel devices with low leakage currents, can be in part attributed to the reliable gate-to-source junction. Indeed, measurements of the GS characteristics of the long channel transistors, revealed that the leakage current is kept small at reverse voltages up to 40V, which is enough to pinch off the channel even for the devices with 4 μm channel width. This indicates that the fabricated devices have robust gate junctions and a negative gate voltage can be applied to obtain a high blocking voltage. Note also that these are the devices with the shorter mesa height showing that this parameter is not crucial for having low leakage between gate and source.

Nevertheless, the voltage capability for these VJFETs exhibiting the static-induction effect in the reverse blocking regime depends mainly on the L_G/W_{ch} ratio [**Erreur ! Signet non défini.**]. Higher values of this ratio, as in the case of our long devices, result in higher blocking voltage

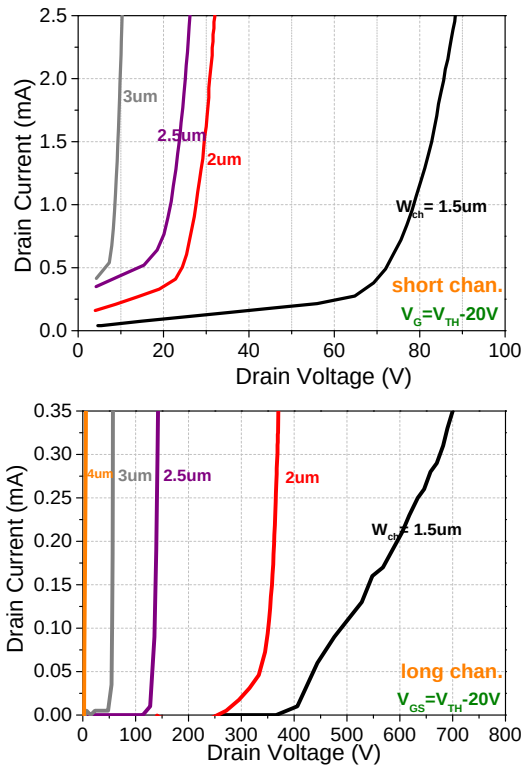


Figure 10. Reverse blocking characteristics of the different channel width devices

capability or in other words higher voltage gain values.

In the case of VJFETs exhibiting the static-induction effect, the parameter quantifying this gain control between the voltage across the device (V_{DS}) and the gate bias (V_{GS}) is called the "voltage gain" or "blocking voltage gain" or "AC voltage gain" or "differential voltage gain", but is al-

so sometimes referred to as "voltage amplification factor". The highest voltage gain values were reported for the narrowest transistors, which exhibited the best blocking behavior. Particularly for the W_{ch}=1.5um "long" and "short" channel transistors the voltage gain was found equal to 51 and 9.5 respectively. Fig. 11 shows the voltage gain (μ) dependence on the increase of channel width and on the L_G/W_{ch} ratio. A decreasing tense is observed with an abrupt inflection when passing from 1.5μm channel width devices to that with 2μm channel width.

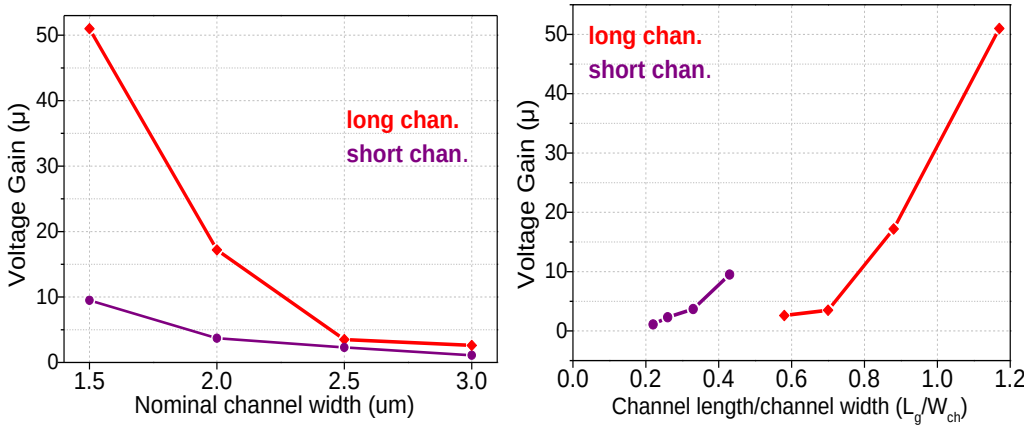


Figure 11. Voltage gain (μ) values.

The blocking voltage capability depends also on the device drift region thickness. The fabricated samples feature drift layer of 8μm and a maximum blocking voltage higher than 1000 V was expected. However, to reach this voltage, the VJFET has to be characterized by a high voltage gain (>40) with a simultaneous capability of high gate voltage (>25V for a gain of 40). In the case of our devices, this condition was met only for the smaller channel width long device. The fact that the maximum voltage blocking was only 500 V is attributed to the edge termination and more precisely to the fact that the top n^+ layer has not been removed from the floating guard rings.

4 Conclusions

This paper presents the design consideration, fabrication and electrical characterization of 4H-SiC TI-VJFETs with different channel lengths and widths. The electrical characteristics showed that the longer (i.e. deeper Al implantation) gate transistors exhibit higher on-resistance values and lower leakage currents as expected. The threshold voltage and gate-source characteristics were similar for the two types (long and short channel) of transistors. The blocking characteristics were triode-like and consequently the rated voltage class are determined by a static induction effect and therefore rather from the channel geometry than from the drift layer doping and thickness. The advantage of the hereby proposed technology is its robustness and simplicity as only four self-aligned photolithography steps have been employed.

A major conclusion of this study is that a high L_G/W_{ch} ratio (higher than 1.2) is necessary for good blocking purposes (e.g. high blocking voltage with small gate bias).

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