Real-Time Impedance Characterization Method for RFID-Type Backscatter Communication Devices

Benoit Couraud, Thibaut Deleruyelle, Edith Kussener, Remy Vauche

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B. Couraud *Student Member IEEE*, T. Deleruyelle *Member IEEE*, E. Kussener *Member IEEE*, R. Vauché, *Member IEEE*

***Abstract*— This paper presents a Radio Frequency measurement method that allows to determine electrical characteristics like scattering parameters or impedance of contactless passive chips, using common measurement devices as oscilloscope, personal computer and directional coupler. The measurements obtained using this method are as accurate as those obtained with vector network analyzer (VNA) measurements, while providing several improvements. First, the method makes it possible to measure a chip's impedance in activation state, which requires large input power, not compatible with VNA measurements. Secondly, this method realizes a real time measurement, which consists in impedance measurement as a function of time. Therefore, this real-time measurement makes possible to detect and measure the impedance changes of an actual contactless smart card's integrated circuit during a load modulation communication at different powers. Finally, this real time impedance measurement gives important information on chips electrical characteristics that can be used to optimize NFC (Near Field Communication) devices design in order to reduce the power losses within an RFID (Radio Frequency Identification) tag.**

***Index Terms*— Radio Frequency Identification, Near Field Communication, Impedance measurement, scattering parameters, modulation**

I. INTRODUCTION

RFID (Radio Frequency Identification) consists in communication between a reader device, and an object as a smart card, positioned at some distance away from the reader. The RFID technology is used in many applications such as electronic payment or electronic passport. For 13.56 MHz applications, the reading device is composed of a controller, a Radio Frequency (RF) circuit, and an inductive antenna, which sends a modulated RF signal to the card. The card, also called tag, is composed of a chip (integrated circuit (IC)) and an inductive antenna. In the present paper, we will focus on passive cards, which are remotely powered by the reader. The power is carried by the modulated RF wave sent to the card by the reader as depicted in Fig. 1. Throughout this paper, the frequency of the carrier will be 13.56MHz, which is the Near Field Communication (NFC) operating frequency. However, the measurement setup described here, can be generalized to other frequencies, depending on the acquisition speed of the electronic test instrument.

NFC technology has experienced a strong development in the last few years, mainly consisting in an increase of the data rate from 106 kb/s and 424kb/s to 6.78Mb/s, called Very High Bit Rate (VHBR) communication [1].

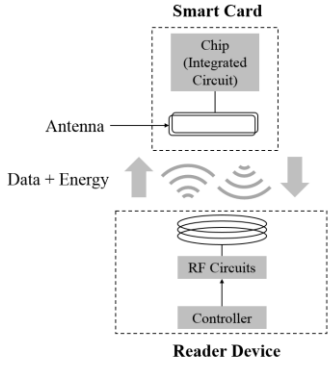

Fig. 1. Principles of Contactless Smart Card Operation. Power is provided by the reader, and harvested by the antenna of the tag. Data is exchanged in both directions (upward and downward).

This increase in the data rate involves a wider bandwidth for communication signals and a reduction of the quality factor for readers electronic circuits (filters, matching circuits), reducing the power transfer capability between the reader and the tag's IC. Thus, it becomes necessary to reduce power losses inside a PICC (Proximity Integrated Circuit Card) by optimizing the power transfer between the tag's antenna and its IC. One way to reduce these losses is to perfectly match the impedance of the antenna to the impedance of the chip (the antenna's impedance has to be as close as possible to the conjugate of the chip's impedance).

Therefore, when it comes to card manufacturing, an accurate measurement of the impedance of the chip is important in order to optimize the antenna design for power transfer. Unfortunately, the impedance of a card's chip is highly dependent on the power received by the card from the reader, as shown in [2]–[4]. These impedance changes are due to the different states in which the input power put the chip (Power on, Reset, Read, Write, cryptographic computation…). Moreover, in order to comply with proximity cards standards (like ISO 14 443, NFC Forum or EMVCo), a smart card manufacturer must ensure that the load modulation tested

B. Couraud (e-mail: benoit.couraud@isen.fr), T. Deleruyelle (e-mail: thibaut.deleruyelle@isen.fr) and E. Kussener (e-mail: edith.kussener@isen.fr) are with the Electronics and Numerical technologies Institute (ISEN) based in Toulon, France. With R. Vauché (e-mail: remy.vauche@im2np.fr), they are all members of the Institut Matériaux Microélectronique Nonosciences de Provence (IM2NP), University of Aix Marseille

according to ISO/IEC methods achieves the required voltage load modulation amplitude. This amplitude is directly dependent on the chip impedance changes during a communication, for which no measurement setup have been designed yet. Indeed, these measurements cannot be achieved with standard VNA as standard VNA cannot deliver the needed power to activate the card's chip, and cannot measure the impedance changes because of the very short time steps for load modulation impedance changes. Indeed, as it will be shown in this paper, the accepted power by a chip is above 10 dBm for activation of the chip, and above 25 dBm for the highest state of security mode (clamp state), which correspond to a larger 50Ω signal generator output power, depending on the chip impedance variation, according to (1). Indeed, the power accepted by a chip supplied by a signal generator can be expressed as a function of the incident power from the signal generator of impedance Z_0:

$$P_{accepted} = P_{Generator_{50\Omega}}\left[1 - \left|\frac{Z_{chip}(\omega) - Z_0}{Z_{chip}(\omega) + Z_0}\right|^2\right] \quad (1)$$

In the case of this paper, Z_0 is real and equal to 50Ω. Moreover, the IC load modulation changes during a communication with a reader occur in a very short time (between 10µs and 0.2µs depending on the data rate from 106 kb/s to 6.78 Mb/s). Works presented in [5]–[7] either do not allow measurement with such power, or are not suitable for the considered RFID frequencies. Hence, alternative impedance characterization techniques have been proposed in [4], [8]–[10], that can be used to determine PICC chips' impedance, but not for different input power, nor during a communication.

In the present paper, these measurement techniques have been enhanced to measure chips' impedance from the switched off state (very low voltage sent to the chip) up to the destruction level, and more importantly during a communication at any ISO 14443 data rate.

Section II presents the chip impedance measurement technique for real time measurements, while section III describes how this method is currently used by industrials to assess their chips characteristics, and then to optimize the antenna parameters for actual smart card devices.

II. Impedance Characterization Setup for Proximity Integrated Circuit Cards (PICC)

This section presents the tag IC impedance measurement setup. As it has been explained above, in order to optimize the power transfer between a PICC antenna and its chip, it is necessary to match the antenna to the IC, which can only be done if one knows the chip's impedance at operating voltage. Hence, measuring this impedance is the main goal of the proposed measurement setup.

A. Chip Impedance Model

First, it is necessary to define what chip's characteristics are measured. As introduced in [4], a PICC electrical model can be used as shown in Fig. 2, with the antenna (*Ra*, *La*, *Ca*), the assembly (*R*, *C*) and the chip (*Rc*, *Cc*). The aim of a chip's impedance characterization technique is to estimate the equivalent circuit constituted by R_c and C_c.

The capacitance *C* helps the antenna designer to tune the system at the desired frequency, whereas the resistance *Rc* is inversely proportional to the power consumed by the chip. In common applications, resistances *R* and capacitance C_a can be neglected. As presented in [11], the admittance of the chip can be expressed as a function of the reflection coefficient of the chip and the corresponding characteristic impedance, as shown below.

$$Yc = \frac{1}{Zo} \cdot \frac{1 - S_{11}}{1 + S_{11}} \quad (2)$$

where Z_0 is the characteristic impedance generally equal to 50Ω and S_{11}, the S parameter of the chip, in this case equal to the reflection coefficient.

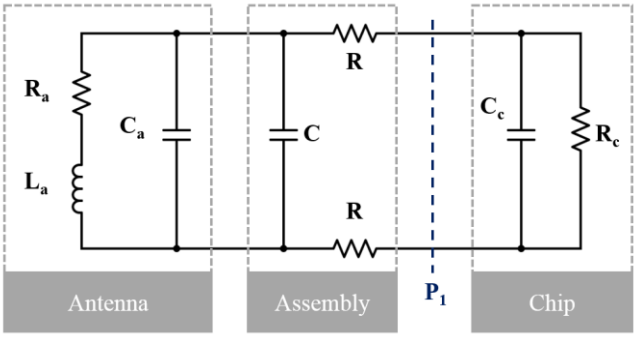

Fig. 2. Electrical Model of a PICC

The aim of the proposed method is to determine *Yc* from a one-port S parameter measurement using (2). Then, *Rc* and *Cc* can be expressed as follows:

$$\frac{1}{Rc} = \mathrm{Re}\left[\frac{1}{Zo} \cdot \frac{1 - S_{11}}{1 + S_{11}}\right] \quad (3)$$

$$Cc = \frac{1}{2\pi f} \cdot \mathrm{Im}\left[\frac{1}{Zo} \cdot \frac{1 - S_{11}}{1 + S_{11}}\right] \quad (4)$$

where f is the input signal frequency for the S_{11} measurement.

B. Chip Characterization Setup

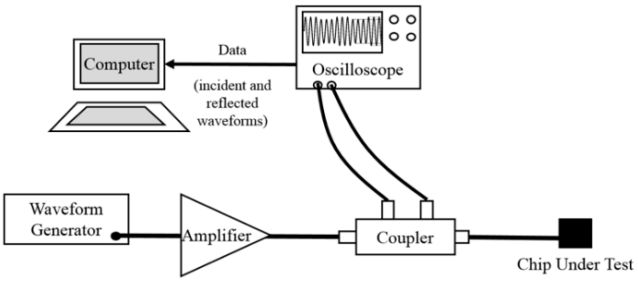

Fig. 3. Setup for Chips Impedance Measurements

The method proposed in this paper consists in measuring

the impedance of the device under test (DUT), without a VNA (which power limits and long measurement time have been emphasized) but with a directional coupler, an acquisition device (as an oscilloscope) and a Personal Computer linked to the acquisition device, as shown in Fig. 3.

The chips under test used in this paper are actual industrial chips used for electronic passport, and capable of communicating at VHBR (Very High Bit Rates). The measurements throughout this paper are realized at ambient temperature (23°C).

In this setup, a waveform generator is used to generate a 13.56 MHz carrier. It can be a common waveform generator, but it can also be any NFC reader device, as it will be shown later. Incident and reflected waves are extracted by the bi-directional coupler and sent to the oscilloscope. The directional coupler and the oscilloscope act as the coupler and the coherent receiver of an actual VNA, with the advantage that the oscilloscope has a large bandwidth of acquisition. Thus, the oscilloscope acts as an acquisition device that will send the recorded incident and reflected voltages to a computer so it can process them. Any other high sampling rate acquisition device can replace the oscilloscope. In order to make this measurement, it is necessary to connect the chip (tag IC) to the bi-directional coupler. This can be done by mounting the chip on a PCB in a standalone configuration, as shown on Fig. 4. a, where PICC chips are soldered to the PCB at their two antenna connectors, and the PCB adopts a single Coplanar Waveguide with Lower Ground Plane architecture, where no differential input is required as one port is taken as the reference.

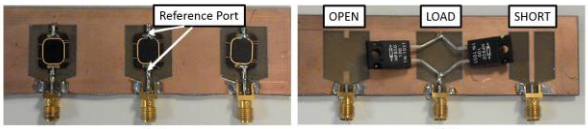

Fig. 4. PICC chips mounted in a PCB for characterization (a) and custom calibration kit (b)

Then, to extract *Rc* and *Cc*, a classical de-embedding technique [12] associated to the one-port S parameter measurement is used, which consists in determining the reflection coefficient of the chip from the incident and reflected wave records. The aim of the proposed algorithm is to realize this computation for every quarter of a 13.56 MHz carrier period (chosen arbitrarily, any measurement time step will suit), in order to obtain the chip impedance evolution during each step of a communication, without decreasing the accuracy of the measurement. First of all, the definition of the S-parameter of a device is expressed as follows [13]:

$$\underline{S_{11}} = \frac{\underline{b_1}}{\underline{a_1}} \tag{5}$$

where b_1 is the reflected wave and a_1 the incident wave, that are recorded from the two outputs of the coupler.

However, dividing the reflected voltage by the incident wave voltage will not give accurate results for the Measured reflection coefficient (Γ_M) [5]: indeed, it is necessary to calibrate the measurement set up. Three kinds of errors may arise in the measurement of the incident and reflected wave: a directivity error, a tracking error, and a port match error. Fig. 5 displays a one-port device flowgraph that represents all possible signal paths and the errors due to these multiple paths.

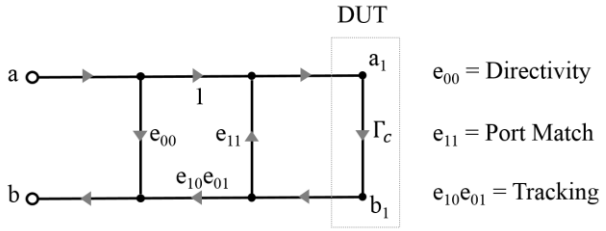

Fig. 5. Flow Graph of a One Port Device

In this simplified model, errors due to the directional coupler, the cables, connectors, and the acquisition device can be considered as due to a fictitious component placed between the coupler and the Device Under test (DUT), that modifies the incident and reflected waves amplitude and phase. Thus the Measured reflection coefficient Γ_M includes these error sources, and has to be corrected in order to determine the Chip's real reflection coefficient Γ_c. One can determine the equation that links the Measured (and thus incorrect) reflection coefficient Γ_M and the chip's real reflection coefficient Γ_c as shown in [14]:

$$S_{11\,M} = \Gamma_M = \frac{b}{a} = \frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} = \frac{e_{00} - \Delta_e \Gamma_c}{1 - e_{11}\Gamma_c} \tag{6}$$

Where A_r and φ_r are the reflected wave amplitude and phase respectively, and A_i and φ_i the incident wave characteristics. Thus,

$$\Gamma_c = \frac{\Gamma_M - e_{00}}{\Gamma_M e_{11} - \Delta_e} = \frac{\frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} - e_{00}}{\frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} e_{11} - \Delta_e} \tag{7}$$

with

$$\Delta_e = e_{00} e_{11} - e_{10} e_{01} \tag{8}$$

In order to determine the three unknown quantities e_{00}, e_{11} and Δ_e, the method consists in measuring the reflection coefficient Γ_M of three well-known loads whose real reflection coefficient (Γ_i) is known, and to solve the following system for the unknown error coefficients listed above:

$$\begin{cases} e_{00} + \Gamma_1 \Gamma_{M1} e_{11} - \Gamma_1 \Delta_e = \Gamma_{M1} \\ e_{00} + \Gamma_2 \Gamma_{M2} e_{11} - \Gamma_2 \Delta_e = \Gamma_{M2} \\ e_{00} + \Gamma_3 \Gamma_{M3} e_{11} - \Gamma_3 \Delta_e = \Gamma_{M3} \end{cases} \tag{9}$$

The three loads chosen for this measurement method are the ones shown in Fig. 4. b. One could use standard calibration kit if they can sustain the large input power, but custom kits will take into account the connection and the line between the chip and the coupler, and accept larger incident power. Thus, the self- designed calibration kit example consists of a custom Short Open Load (SOL) calibration kit which has the same footprint as the PCB for the chips, displayed in Fig. 4. a. The

Load termination consists in two parallel 100Ω ±1% resistances integrated in TO-220 packages, which allow a precise 50Ω load to be obtained and to be used up to 50dBm which is sufficient if 13.56MHz RFID power level is considered. This arrangement leads to a measure of the reflection coefficient seen from the closest plane to the chip (P1 on Fig. 2). Hence, for this known calibration kit, the real reflection coefficients must be: $\Gamma_{OPEN} = 1$, $\Gamma_{SHORT} = -1$ and $\Gamma_{50\Omega} = 0$. Once the measurements of Γ_{M_OPEN}, Γ_{M_SHORT} and $\Gamma_{M\_50\Omega}$ have been done, it is possible to solve (9) for e_{00}, e_{11} and Δ_e. Then, computing the real reflection coefficient of a given chip from the measure of incident and reflected voltages can be done using (7), where the reflected wave ($A_r e^{j(\varphi_r)}$) and the incident wave ($A_i e^{j(\varphi_i)}$) still need to be determined, as shown below.

The amplitude A_x and phase φ_x of a signal x can be computed from the voltage data recorded by the acquisition device. The proposed method consists of a Goertzel algorithm [15] implemented within the processing device (PC) or the acquisition device, that computes the amplitudes and phases of the two voltages (incident and reflected) at every quarter of a carrier period, depending on the sampling rate of the acquisition device. According to [15], the amplitude and phase of a signal can be computed using a very limited number of operations which makes it ideal for fast computations, and preferred to the Hilbert transform or even a Radix-2 FFT. Furthermore, it requires very few data points to provide an accurate computation of the two signal characteristics. The amplitude A_x^N of a signal x and φ_x^N its phase are given below, with N the block size to achieve a certain frequency resolution:

$$A_x^N = \sqrt{\left[Q_1^N - Q_2^N.\cos\left(\frac{2k\pi}{N}\right)\right]^2 + \left[Q_2^N.sin\left(\frac{2k\pi}{N}\right)\right]^2} \quad (10)$$

$$\varphi_x^N = atan\left[\frac{Q_2^N.sin\left(\frac{2k\pi}{N}\right)}{Q_1^N - Q_2^N.\cos\left(\frac{2k\pi}{N}\right)}\right] \quad (11)$$

where :

$$k \in \mathbb{N}, \qquad i \in [0, N]$$

$$\mathrm{N} = \frac{k.Sample\ Rate}{13.56.10^6} \quad (12)$$

$$Q_1^i = Q_0^{i-1} \quad (13)$$

$$Q_2^i = Q_0^{i-2} \quad (14)$$

$$Q_0^i = 2\cos\left(\frac{2k\pi}{N}\right).Q_1^i - Q_2^i + x(i) \quad (15)$$

with *x(i)* the incident or reflected voltage sample at time *i*, which has been windowed numerically using Blackman windowing. *k* is the size of the required acquisition sample expressed in number of periods of the carrier (if it is needed to acquire 2 periods of data, then *k = 2*). The computation of the $Q_{0,1,2}^i$ coefficients is done for every time sample (*i*), until $Q_{0,1,2}^N$ can be computed to determine the amplitude A_x^N and phase φ_x^N of the considered signal x. Thus, every *N* samples, the ratio between the incident and reflected signals is computed. The higher the number of sample per period ($\frac{N}{k}$) is, the more accurate the result will be. The amplitude and phase of incident and reflected waves are computed for each element of the SOL calibration kit so the three error coefficients can be computed using (6) and (9). Then, (7), (3) and (4) are used to determine the impedance of the Chip Under Test, every quarter of carrier period for example.

The setup displayed in Fig. 3 has been implemented using a National Instrument PXI (Peripheral component interconnect eXtensions for Instrumentation) hosting a custom-made transmitter and a receiver, constituted by an FPGA that drives a Digital to Analog Converter for the transmitter, and an Analog to Digital Converter for the receiver. In order to measure the impedance at every quarter of the carrier period, it is necessary to use an acquisition device with a FPGA or to use a high sample rate oscilloscope in order to achieve enough measurements per carrier period. In the 13.56 MHz NFC domain, this requires acquisition devices with acquisition speed above 300 MSample per second to achieve a measurement error below 1%. However, this sampling requirement can be lowered thanks to Goertzel algorithm. Indeed, the Goertzel algorithm gives very accurate results for the amplitude and phase of a signal in the two following cases: either the acquisition device proposes a high acquisition speed, in which case there are enough samples per carrier period to achieve an accuracy below 1%. Either the acquisition rate is close to a multiple of the carrier frequency, while still respecting Shannon criteria. In the 13.56 MHz RFID case, one could consider an acquisition device with a sampling rate of 40 MS/s. This acquisition speed is close to 3 times the carrier frequency, and would lead to 3 samples per carrier period. This would give a measurement error below 5%. Furthermore, the vertical resolution used in this implementation was 12 bits per sample, with a -3dB bandwidth of 2.27 GHz, but could be reduced without affecting the accuracy of the measurement.

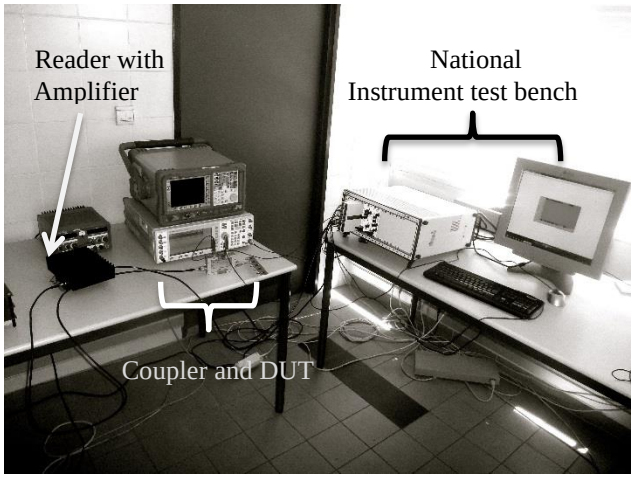

Fig. 6. Measurement Environment

Finally, the ISO/IEC 14443 Standards have been implemented in order to communicate with PICCs [16], as it

will be shown later. The setup is displayed in Fig. 6.

In order to validate this measurement setup, passive loads impedance have been measured using a VNA and using the measurement protocol described above. TABLE 1 shows the comparison of the obtained impedance at a single input power, where the accuracy is computed as follows:

$$Module\ error = \frac{\left|\,|Z_{from\ VNA}| - |Z_{new\ method}|\,\right|}{|Z_{from\ VNA}|} \quad (16)$$

TABLE 1. Real Impedance and Measurements Comparison

Impedance from VNA method (Ω)	Impedance from new method (Ω)	Module error (%)	Phase error (%)
99.96 + j0.3	99.86 + j0.3	0.1	3.4
0.46 + j22.1	0.12 + j22.7	2.7	1.0
0.9 – j458	2.1 – j449	1.9	0.2

One can see that these measurements match the impedance measured by the VNA, as the error is comparable to the measurement errors from the VNA. The validation of this method has also been done on 12 real smart cards chips. Then, the same measurements as those obtained in [4] using a VNA and an amplifier have been realized. Fig. 7 shows a Smith Chart display of a chip impedance measurement when the input power varies. The curves correspond to a measurement realized with the method described in [4], that uses a VNA and an amplifier, and the measurement as described above. These measurements demonstrate the ability of the proposed method to realize impedance measurements with large power sweep.

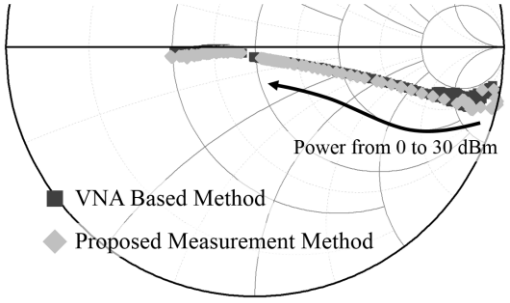

Fig. 7. Comparison between Chip Impedance Measurements by the two methods for a large range of input power (0 to 30 dBm)

In this section, a measurement setup has been proposed for measuring 13.56 MHz PICC's IC impedance. The advantages of such a method are that it can measure a chip impedance at any power, and thus in any state of the chip. Also, as it will be presented in the next section, the other advantage of this method compared to other methods already existing is that it has a very small measurement time step, and can be used to detect chip impedance changes even during a communication. Section III will describe the possible characterization of PICC ICs that can be used to assess the design of ICs.

III. PROXIMITY INTEGRATED CIRCUIT CARDS CHARACTERIZATION

This section presents the different characteristics of a PICC chip that can be assessed with the proposed measurement setup.

A. Chip Impedance as a Function of Input Power

As it has been shown in [2], [5], [6] a tag's IC impedance highly depends on the supply power. As an example, a measure of a chip's parallel resistance and capacitance as a function of the input power has been realized, and results are shown in Fig. 8. Measurements were validated by comparing them to the values obtained using the measurement setup described in [4].

This measurement makes it possible for industrials to determine the impedance of their chip at different states of operation, and thus to determine the impedance to which the antenna of the final tag will have to be tuned. A good choice is to match the antenna to the chip impedance measured at the lowest input power at which the chip is able to reply to a reader request. One can notice that in this case, the antenna will be matched to the impedance of the chip at one particular power. In real life application, that power will correspond to the power received by the chip when the card is at a particular distance from a reader. However, in these real life applications, a smart card is in motion during a communication. By choosing to design the antenna at the lowest power at which the IC responds, all cases will be covered as the need for matching or tuning is smaller when the smart card comes closer to the reader (which corresponds to larger input power). Finally, the orientation between the reader and a card has also an impact on the input power, but is not covered in this work.

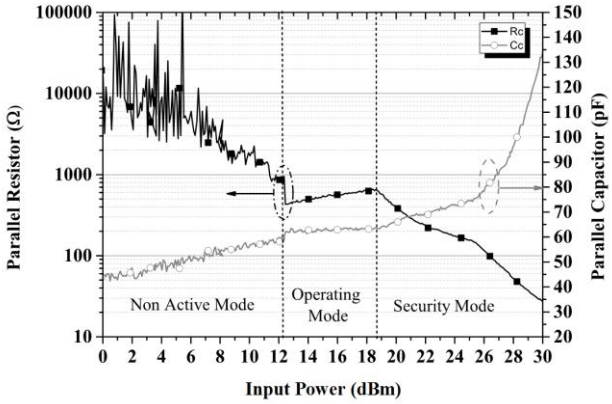

Fig. 8. Chip impedance as a function of the input power (50 Ω)

In addition, these impedance measurements can be done to determine the optimal design for the chip itself, as shown in the following example. The tested chip for this example is a particular chip that operates in a loop mode, at different Integrated Circuit (IC)-clock frequencies. The jitter deviation level defines these clock frequencies. The larger the jitter is, the lower the operating clock frequency will be (and the performance), and thus, the lower the consumed power will be. Measurements have been done for a large range of input power;

and for every power level used, the chip's impedance was measured. These measurements are displayed in Fig. 9. This figure presents the evolution of the impedance (R_c and C_c) as a function of input power and of the operating clock frequency of the chip. Since the power consumed by the chip decreases when the parallel resistance increases, Fig. 9 demonstrates the advantages of implementing a lower clock frequency for the chip in terms of power consumption. As mentioned above, it also makes it possible for the manufacturer to know precisely the impedance of the chip for different operating states. Fig. 9 shows also that the parallel resistance of the given chip is close to constant until the clock frequency falls below 80%. This allows the chip software designers to know that a clock frequency between 80 and 100% will consume the same amount of power, meaning that for a low power mode, the clock rate will have to be decreased below 80%.

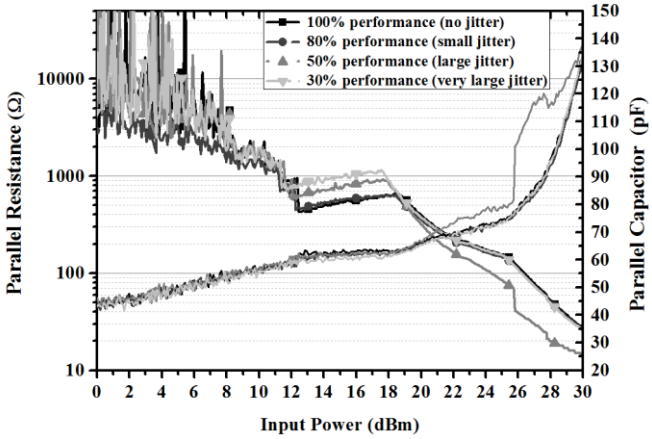

Fig. 9. Chip Impedance measurement as a Function of the input power (50 Ω) and the Clock Frequency

Finally, the setup has also been applied to assess the uniformity of chips impedance produced by a production line, so the manufacturer can assess the reliability of its production line and detect failures before integrating the chips into a tag. One can see on Fig. 10 that one sample behaves differently from the others, and thus has been rejected. The other chips present a good uniformity, which is important as the same antenna will be used for every chip.

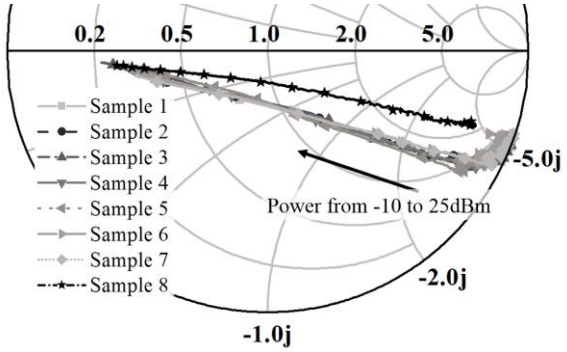

Fig. 10. Comparison of ICs impedance from the same Production Line of industrials manufacturers as a function of input power (50 Ω) from -10 to 25 dBm (low power range as requested by the manufacturer to not stress the ICs)

Up to this point, the measurements shown have been realized by sending only a single frequency signal at 13.56 MHz on the chip under test, and do not give any information about the behavior of a chip when a reader device sends a request, nor what is the exact power at which the chip begins to respond to a request. The next part will describe how the measurement method proposed in section II allows chip designers to measure the impedance of their chip during a communication, which gives useful information on the chip's power consumption, and on its ability to communicate when integrated into a tag.

B. Chip Impedance during a Communication

1) Measurement Setup

To realize the measurements of the PICC IC impedance changes during a communication and especially during the load modulation phase, the waveform generator displayed in Fig. 3 has been replaced with a NFC reader. Using this updated measurement setup, the NFC reader's output power is increased until a communication is established with the chip under test through the directional coupler. This communication can be at any data rate, low or VHBR, which requires a negotiation phase. As presented above, the algorithm used computes the impedance at every quarter of carrier period, which makes it suitable to measure a chip impedance even during the load modulation phase at a data rate of 6.78 Mb/s.

Thus, using a high sample rate acquisition device, the incident and reflected waves available at the outputs of the directional coupler were recorded from the beginning of the transmitter (NFC reader) request at 1.7Mb/s, until after the end of the chip answer at 3.39Mb/s. The recorded incident and reflected waves are displayed in Fig. 11.

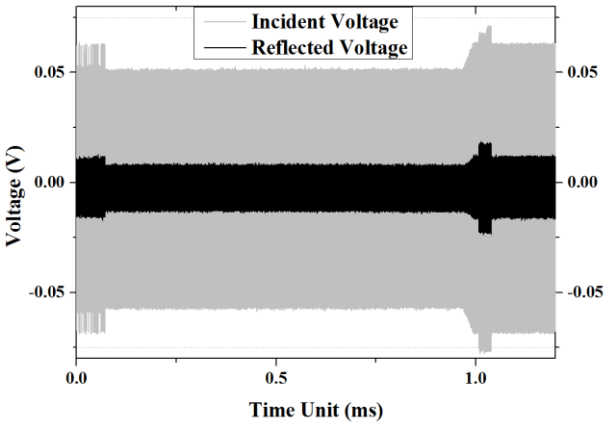

Fig. 11. Incident and Reflected Waves during a VHBR Communication

With these two incident and reflected waves, one is now able to compute the chip impedance at every quarter of a period, as presented in section II.

2) Impedance Changes during Load Modulation

The results of the impedance computation as a function of time are displayed in Fig. 12. One can see the chip's impedance variations during the reader request phase (due to different input power, as amplitude modulation is used), during the processing phase, and also during the backscattering load modulation

phase. During the processing time, the PICC is still harvesting energy, but is also consuming more power, as the parallel resistance is low. Indeed, the parallel resistance, in black in Fig. 13 and 14, represents the consumption of the chip during the communication. Moreover, the parallel capacitance follows the resistance changes in order to maintain a stable power supply of the chip.

Finally, determining this resistance at the lowest communication power allows antennas manufacturers to define the optimized parameters for good power transfer.

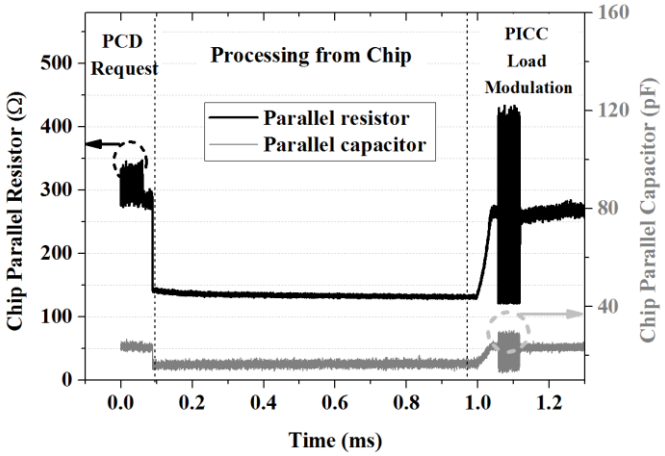

Fig. 12. Chip Impedance Evolution (parallel resistance R_p and capacitance C_p) during a VHBR Communication with Reader Request at 1.7 Mb/s and Load Modulation at 3.3Mb/s

Fig. 13 also displays the same impedance measurement, but with a load modulation bit rate of 106kb/s. One can confirm that the impedances are the same for the two different data rates, as long as the input power is the same.

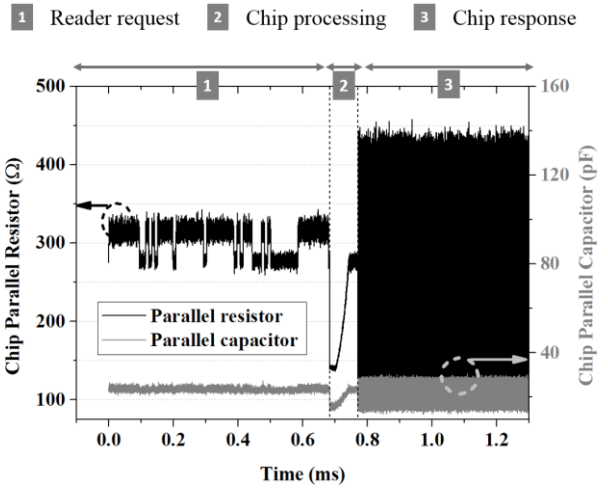

Fig. 13. Chip Impedance Evolution during a VHBR Communication with Load Modulation at 106kb/s. In black, parallel resistance evolution during time, in gray the parallel capacitance

Fig. 13 and 14 display very useful information for manufacturers, as they make it possible to assess the chip's impedance during each step of a communication, including processing and load modulation. With such information, manufacturers can consider the coupling between a reader antenna and the tag antenna to determine in advance the load modulation amplitude that will be achieved by the integrated smart card [17] (required for ISO 14 443).

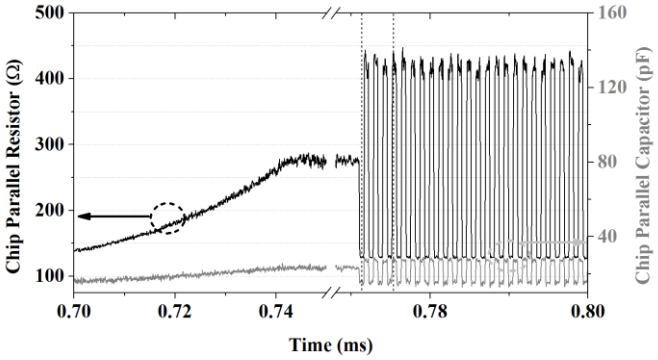

Fig. 14. Zoom on the Chip Impedance evolution during the processing and at the beginning of the chip response

Hence, the impedance variation in the load modulation phase of the communication can be measured accurately, and can reveal useful information about the ability of the smart card to comply with ISO/IEC 14443 PICC signal transmission requirements for example.

3) Non Linear Characterization

Up to this point, only the carrier frequency was considered to compute the chip's impedance. However, [18] shows that due to the presence of the rectifier circuit, an UHF RFID chip has a nonlinear behavior, that affects the response of a tag by reflecting not only the carrier frequency, but also its odd harmonics, and especially the 3rd one. The same applies to 13.56 MHz RFID systems and can be assessed by taking the power spectral density of the tag response recorded by the acquisition device, which is realized in Fig. 15. One can see the presence of the 3rd and 5th harmonics due to the RF to DC conversion, that constitute a power loss at the fundamental frequency, as presented in [6].

Finally, according to [6], changing the matching between the antenna and the chip could optimize the reflection of odd harmonics of the carrier, and thus increase the efficiency of the system.

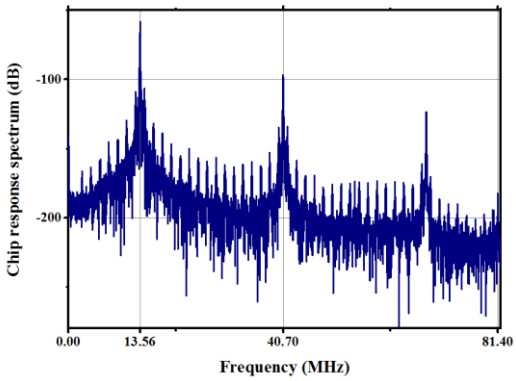

Fig. 15. Power Spectral Density of the Reflected Response of the Tag

4) Smart Card Electro-Magnetic Security

Finally, the last useful information given by this measurement method consists in a very useful security information. Indeed, as one can see in Fig. 12, the chip's impedance during processing (between the reader request and the chip load modulation phase) stays constant, and does not give any information about the ongoing computations of the chip. This characteristic is needed for robustness to hacking situations, in which hackers could determine the chip calculations by decrypting the electrical characteristics during the processing state, as shown in [19].

IV. Conclusion

The method proposed in this article allows most of laboratories to realize their own smart card's IC impedance measurements during a communication with a reader, with common and inexpensive measurement devices. The frequency range of this measurement set up is only restricted by cables quality, distortion of power amplifier and by the sampling frequency of the acquisition device. The results of this method are as accurate as those provided by VNA based setups. Besides, compared to VNA, it also allows designers to measure a chip's impedance at required powers, at very short time steps, and even during a communication. With VHBR evolution, engineers will need to measure accurately chips' impedance in order to optimize the power transfer between antenna and IC in Smart Cards applications (impedance matching). As presented above, this method provides the necessary information to realize this matching, in addition to information about robustness of smart cards IC to power analysis attacks, or about backscattering impedance, that can be used by designers to assess if their chip will comply with load modulation standard requirements. This is why this method of Real Time impedance measurement during communication and over a large power range is a necessary tool that is used to optimize the design of NFC devices.

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