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A 9pJ/Pulse 1.42V_{pp} OOK CMOS UWB Pulse Generator for the 3.1-10.6 GHz FCC Band

S. Bourdel, Y. Bachelet, J. Gaubert, *Member, IEEE*, R. Vauché, O. Fourquin, N. Dehaese, and H. Barthelemy, *Member, IEEE*

Abstract—This paper presents the design of a fully integrated ultra-wideband (UWB) pulse generator for the FCC 3.1-10.6 GHz band. This generator is reserved for medium rate applications and achieves unipolar pulses for OOK, PPM or PIM modulations. This UWB transmitter is based on the impulse response filter method which uses an edge combiner in order to excite an integrated bandpass filter. The circuit has been integrated in a ST-Microelectronics CMOS 0.13 μ m technology with 1.2V supply voltage and the die size is 0.54mm². The pulse generator power consumption is 9pJ per pulse and achieves a peak to peak magnitude of 1.42V. The pulse is FCC compliant and the generator can be used with a rate up to 38Mbps⁻¹ with a OOK modulation. Based on the FCC power spectrum density (PSD) limitation, a sizing method is also presented.

Index Terms— Pulse generation, FCC, Transmitters, Impulse Radio, Ultra-wideband (UWB), Pulse shaping circuit.

I. INTRODUCTION

Since the FCC has authorized communication in the 3.1 GHz to 10.6 GHz frequency band, several technologies have been developed to satisfy the communication market. These technologies are more or less suited to the numerous applications generally encountered. Typically, Orthogonal Frequency Division Multiplexing (OFDM) technique appears to be good candidates for high speed data communication whereas Impulse Radio (IR) is a good solution for low cost systems or positioning systems. In the case of IR systems, due to the applications, the most limiting characteristics of the system are the circuit cost production, the power consumption and the operating range. For the emission stage, those constraints mean that the transmitter must be designed using low cost technologies such as CMOS and must consume a small amount of power while generating pulses having large magnitude.

UWB impulse radio designs often use baseband pulse generator. Those baseband pulses are then used to produce

more complex pulses to match regulation frequency masks. A first technique to generate baseband pulse consists in using reflections in a transmission line (or a stub) to produce a pulse from a step function. It is difficult to integrate those generators in a CMOS technology due to the use of transmission lines or due to the need of discrete components such as SRD diode [1][2]. Currently, delayed edge combination is a good candidate to achieve baseband pulse and is well suited for UWB systems since it can be fully integrated in CMOS [3][4] and consumes a small amount of power.

Different methods have been presented to generate FCC pulses from one or several baseband pulses. A first technique is to use transversal filters achieved by artificial coupled transmission lines [5]. The baseband pulse propagates along the artificial line and is recombined at the output to achieve a more complex pulse. The artificial line is synthesized with lumped elements which results in the use of a large number of inductors and limits the integration. A second method is to transpose a baseband signal in the frequency band of operation using a mixer and a Local Oscillator (LO). This method is attractive since it uses few inductors and it performs well when it is implemented using LO switching. In spite of LO leakage problems [6], this technique currently appears to achieve the best performances in terms of consumption and pulse peak magnitude [7] [8]. Other methods based on elementary pulse combination have been presented with good potential for the pulse tuning and for achieving biphasic pulses [9][10]. Today, those techniques achieve pulse magnitude around 1V_{pp} but their power consumption dramatically grows with the pulse duration and it exceeds the consumption of LO switching topologies [11] [12]. Another way to produce FCC compliant pulses is to use filtered combined edge [13] [14]. This method is very attractive for its low power consumption potentiality but is penalized by the filter implementation. However, due to the large width of the FCC frequency mask, the order needed for the shape filter is low which leads to acceptable loss (around 3dB), in standard CMOS technologies [15].

The generation method presented is derived from filtered combined edge technique and consists on simply exciting an integrated bandpass filter using a baseband pulse to generate its impulse response. The filter excitation is achieved using a digital edge combiner coupled with a current driver and appears to be well suited for low cost and low power systems. To demonstrate the efficiency of this generation method, an

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UWB FCC pulse generator is designed in a 0.13 μm CMOS technology for medium rate applications around 36Mbs⁻¹. The power consumption is 3.84mW@100MHz Pulse Repetition Frequency (PRF) and the energy consumption is 9pJ per pulse. The pulse generator produces FCC compliant pulses having a measured voltage magnitude of 1.42Vpp. The digital edge combiner used in the design is able to generate pulses with less than 50ps width. It is designed with differential delay cell and high speed logical gate. The bandpass filter is a third order Bessel filter with less than 3dB loss and the whole die size is 0.54 mm². Using a sizing method based on Power Spectrum Density (PSD) analysis, the generator is designed regarding the application needs. This generator achieves unipolar pulses and can be used in On Off Keying (OOK) modulation, Pulse Position Modulation (PPM) or Pulse Interval Modulation (PIM). In OOK mode, the generator can operate up to 38Mbs⁻¹ to cover a large variety of applications including video streaming.

The paper is organized as follows. Section II deals with the theoretical concept of impulse response generation needed to compute the main parameters of the generator. This analysis is made for the FCC standard taking into account the impact of the modulation type and the impact of the bit rate on the design. The design of the pulse generator is presented in Section III. The on-chip filter and the buffer which consist in a current driver are first described. Then, the design of digital edge combiner is detailed. Simulation and measurement are presented and commented in Section IV.

II. PULSE GENERATOR SIZING

A. Pulse generation Principle

The method of pulse generation is depicted in Fig. 1. It consists in applying a short pulse at the input of a filter to generate its impulse response ($h(t)$). If we consider that, instead of a dirac, the filter is excited by a square function $\pi_\tau(t)$ having a magnitude A and a width τ , the output ($g(t)$) and its Fourier transform are given by :

$$g(t) = \frac{A}{\sqrt{l}} \pi_\tau(t) * h_e(t) \quad (1)$$

$$G(f) = \frac{A\tau \text{sinc}(\pi\tau f) \cdot H_e(f)}{\sqrt{l}} \quad (2)$$

where l represents the power loss of the filter and $H_e(f)$ the normalized function transfer of the filter. Computing $G(f)$ allows the determination of τ and $H_e(f)$ which leads to FCC compliant pulses. But, knowing $G(f)$ is not sufficient to size the baseband pulse magnitude (A) and the emitted pulse peak to peak magnitude (g_0). Because these parameters impact the range of the transmission, they must be taken into account in the sizing of the generator. It is then necessary to evaluate the average and peak PSD to size A and g_0 and other characteristics such as modulation type and bit rate must also be taken into consideration.

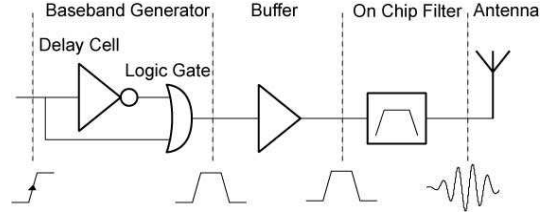


Fig. 1. Principle of pulse generation

B. Average PSD

The Fourier transform $G(f)$ is necessary to calculate the average PSD of the emitted signal. In the case of linear modulation such as OOK or BPSK, the emitted signal is given by (3) :

$$s(t) = \sum_{k=0}^N a_k \cdot g(t - k \cdot T_s) \quad (3)$$

where T_s is the symbol time and $\{a_k\}$ is the sequence of the transmitted symbols. In the case of OOK the value of a_k is simply 0 or 1. If the symbols of the sequence $\{a_k\}$ are independent the PSD is given by :

$$PSD_s(f) = \frac{|G(f)|^2}{T_s} \left(\sigma_a^2 + \frac{\mu_a^2}{T_s} \sum_{i=-\infty}^{\infty} \delta\left(f - \frac{i}{T_s}\right) \right) \quad (4)$$

where μ_a and σ_a^2 are respectively the mean and the variance of the sequence data $\{a_k\}$. For BPSK modulation, $\mu_a=0$ and $\sigma_a^2=1$. The PSD is then composed by a continuous spectrum given in V²/Hz. For OOK modulation, $\mu_a=0.5$ and $\sigma_a^2=0.25$. The PSD is then composed of a continuous spectrum and a discrete spectrum where the magnitude of the lines is directly given in V². Because $T_s \ll 1$, the spectral lines are much higher than the continuous spectrum and the ratio (η given in (5)) between the spectral line level and the continuous spectrum increases with the symbol rate ($D_s=1/T_s$). These spectral lines reduce the capability of the generator to achieve large pulse at high rate because the only way to decrease the PSD (for a given pulse and a given rate) is to reduce the magnitude of the pulse. In the case of FCC regulation [16], the PSD is measured in a Resolution Band Width (RBW_{av}) equal to 1MHz which reduces η and so reduces the impact of the spectral lines on the maximum pulse magnitude allowed by the standard.

$$\eta_{RBW=1MHz} = \frac{\mu_a^2}{\sigma_a^2 \cdot T_s \cdot RBW_{av}} \quad (5)$$

With (2) and (4), we can express the PSD as a function of the main parameters of the pulse generator (A , τ , l , Z_0 the output impedance, D_s , $H_e(f)$, μ_a , σ_a) and taking into account the measurement method imposed by FCC.

$$\begin{aligned} PSD_s^+(f) &= 2 \frac{|G(f)|^2}{Z_0} D_s \left\{ RBW_{av} \cdot \sigma_a^2 + D_s \mu_a^2 \sum_{i=-\infty}^{\infty} \delta\left(f - \frac{i}{T_s}\right) \right\} \\ &= 2 \frac{(A\tau \text{sinc}(\pi\tau f) \cdot H_e(f))^2}{Z_0 \cdot l} D_s \left\{ RBW_{av} \cdot \sigma_a^2 + D_s \mu_a^2 \sum_{i=-\infty}^{\infty} \delta\left(f - \frac{i}{T_s}\right) \right\} \end{aligned} \quad (6)$$

Equation (6) gives the unilateral PSD as it would be displayed by a spectrum analyser with its RWB set to 1MHz. The

continuous spectrum is given in W/MHz and the discrete spectrum in W.

Moreover, it appears that for a given filter and a given baseband width, the maximum value of the PSD (PSD_{max}), which is fixed to -41.3dBm/MHz by the FCC, linearly depends on A and D_s . If the frequency for which the PSD is maximum (f_0) is close to the frequency for which $H_e(f)$ is maximum, the maximum value of A allowed by FCC (A_{max}), can be approximated by using (6) in the case of BPSK ($\mu_a=0$ and $\sigma_a^2=1$) and OOK ($\mu_a=0.5$ and $\sigma_a^2=0.25$) as follows :

$$A_{max} = \min \left\{ \left(\frac{lZ_0 \cdot PSD_{max}}{2D_s^2 \tau^2 \text{sinc}^2(\pi f_0 T_s) RBW_{av} \sigma_a^2} \right)^{1/2}, \left(\frac{lZ_0 \cdot PSD_{max}}{2D_s^2 \tau^2 \text{sinc}^2(\pi f_0 T_s) \mu_a^2} \right)^{1/2} \right\} \quad (7)$$

In these conditions, A_{max} mainly depends on D_s and is independent of the filter transfer function.

From A_{max} it is then possible to compute the maximum pulse magnitude (g_{0max}) imposed by the average PSD limitation for a given symbol rate. Because g_0 depends on the filter used ($h_e(t)$) and the baseband pulse ($\pi_r(t)$) it linearly varies with A and can easily be evaluated as follows :

$$g_0 = \frac{A}{\sqrt{l}} \frac{\pi_r(t) * h(t)}{g_{norm}(t)} = \alpha \frac{A}{\sqrt{l}} \quad (8)$$

where $g_{norm}(t)$ is $g(t)$ normalized to g_0 . The α coefficient represents the magnitude efficiency of the filter response to a square function of width τ .

However, to avoid excessive peak magnitude, the FCC also limits the peak power. It is then recommended to verify the FCC compliance of the peak power of the generated pulse.

C. Peak Power Limit

The peak power limitation is specified by the FCC as follows: "there is a limit on the peak level of the emissions contained within 50MHz bandwidth centered on the frequency at which the highest radiated emission occurs, f_0 . It is 0 dBm EIRP." The FCC recommends the use of a spectrum analyzer with a 50MHz RBW and a peak power detector. For rates lower than 50MHz, this measurement corresponds to the peak power of the emitted pulse filtered by the RBW filter. Under this condition, if the pulse spectrum is flat in the RBW and if the RBW filter is supposed to be ideal, the magnitude of the pulse at the RBW filter output for which the spectrum ($G_{pk}(f)$) and its reverse Fourier transform ($g_{pk}(t)$) are :

$$G_{pk}(f) = G_0 \left[\pi_{RBW_{pk}}(f - f_0) + \pi_{RBW_{pk}}(f + f_0) \right] \quad (9)$$

$$g_{pk}(t) = 2G_0 \cdot RBW_{pk} \cdot \text{sinc}(\pi RBW_{pk} t) \cdot \cos(2\pi f_0 t) \quad (10)$$

where G_0 is the magnitude of $G(f)$, $\pi_{RBW_{pk}}(f)$ is a square function having a width equal to the spectrum analyser RBW (RBW_{pk}). The peak power is then given by the level of $g_{pk}(t)$ as follows :

$$P_{pk} = \frac{4 \cdot G_0^2 \cdot RBW_{pk}^2}{Z_0} \quad (11)$$

If the frequency for which the PSD is maximum (f_0) is close to the frequency for which $H_e(f)$ is maximum G_0 is given by:

$$G_0 = \frac{A \tau \text{sinc}(\pi f_0 \tau)}{\sqrt{l}} \quad (12)$$

By using (6), the PSD_{max} can be expressed as in (13) as a function of G_0 . This enables the evaluation of the peak power, as in (14), as a function of the symbol rate in the case where the average PSD complies with the FCC mask for BPSK ($\mu_a=0$ and $\sigma_a^2=1$) and OOK ($\mu_a=0.5$ and $\sigma_a^2=0.25$) modulations.

$$PSD_{max} = \max \left\{ \frac{D_s^2 G_0^2 \mu_a^2}{Z_0}, \frac{D_s G_0^2 RBW_{av} \sigma_a^2}{Z_0} \right\} \quad (13)$$

$$P_{pk} = \max \left\{ \frac{4 \cdot PSD_{max} \cdot RBW_{pk}^2}{D_s^2 \mu_a^2}, \frac{4 \cdot PSD_{max} \cdot RBW_{pk}^2}{D_s \sigma_a^2 \cdot RBW_{av}} \right\} \quad (14)$$

Equation (14) is only valid for rates lower than 50MHz for which the RBW filter only responds to one pulse. Moreover, in the case where the rate is decreased to maximise the pulse magnitude, (14) gives the minimum rate below which further increasing the magnitude is prohibited.

D. Generator Sizing

First, the filter and the width of the baseband pulse must be dimensioned by using (2) or directly by computing the average PSD given by (6). A large variety of filters can be used to be compliant with the FCC standard if their bandwidth and center frequency are tuned to match the FCC mask as shown on Fig. 2. Moreover, whatever the $H(f)$ considered, a 3rd order is sufficient to achieve FCC compliant pulse due to the large width of the frequency mask. This limits the loss in the filter and enables integration in CMOS technologies. The choice of the filter relies on a complex compromise. First, the designer must bear in mind that this choice can be reoriented by the filter design presented later on, especially if the value of the filter components can not be achieved in the targeted technology. To choose the filter, it is relevant to consider the value of τ needed and the magnitude efficiency represented by α . As shown in Fig. 2, where only 3rd order filters are considered, the pulse2 achieves almost the same efficiency (α) as pulse3 with a wider baseband pulse which relieves the constraint on the edge combiner design. Also, for similar

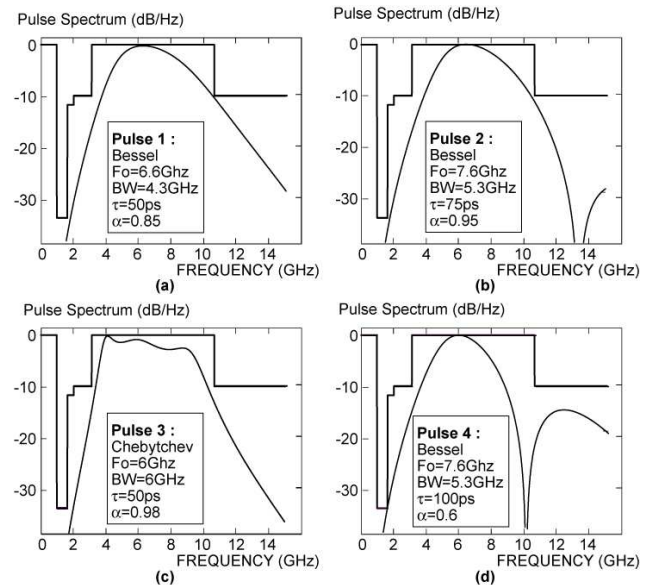


Fig. 2. Relative pulse spectrum ($|G(f)|^2$) comparison for different filters and baseband pulses.

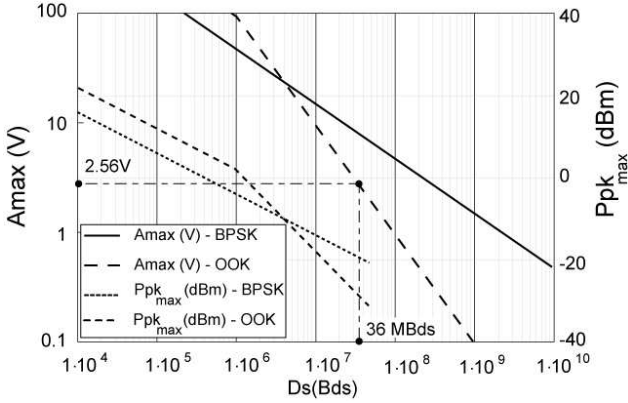


Fig. 3. Maximum baseband pulse magnitude (A_{max}) and peak power limit as a function of D_s for OOK and BPSK

filters (pulse2 and pulse1) lowering τ decreases α and increases the design constraint which is not helpful. Moreover, the pulse4 shows that using large baseband pulses increases the sinus cardinal function influence which degrades the pulse spectrum and also α .

Once the pulse ($g(t)$) chosen, it is then possible to compute with (7) the maximum pulse magnitude allowed by the average PSD, regarding the modulation type and the rate. Fig. 3 reports A_{max} as a function of D_s for OOK and BPSK modulations. Fig. 3 is plotted for pulse2 with 3dB filter power loss.

In the case of OOK modulation, for high rates, the maximum value of PSD is given by the discrete spectrum. When D_s is lower than $D_{s_{lim}} = RBW_{av} \cdot (\sigma_d / \mu_a)^2$, discrete spectrum is lower than the continuous spectrum and the maximum value of PSD is fixed by the continuous spectrum. In our case study, a rate of 36Mbs^{-1} is targeted. Such a rate can be achieved with OOK modulation if the baseband pulse magnitude does not exceed 2.56V, which leads to a $g_0 = 1.73\text{V}$ due to the 3dB filter power loss and due to $\alpha = 0.95$. Moreover, depending on the application needs, the computation of A_{max} can be used in a different way. For a given pulse magnitude fixed by the budget link, the maximum rate can be evaluated for OOK or BPSK modulation.

Lastly, for a RBW equal to 50MHz in the case where A is set to A_{max} the peak power given by (14) is plotted in Fig. 3.

Under this condition, the peak power limit is reached for OOK at $D_s = 1.23 \text{Mbs}^{-1}$ and it is not possible to reduce further the symbol rate to increase g_0 . For BPSK, the limitation is reached for $D_s = 380 \text{kbs}^{-1}$ but it leads to the same value of g_0 . For our case study where $g_0 = 1.73\text{V}$, the peak power is -29dBm .

E. Generator specifications

This theoretical section presents the specification of the main parameters of a pulse generator that uses filter impulse response technique in the case of linear modulation. It shows that a generator can be achieved with a low order filter. A 3rd order Bessel filter is chosen here, especially because it has a good response in terms of magnitude ($\alpha = 0.95$) to a baseband pulse that has a width equal to 75ps. This lowers the constraint on the design in a $0.13 \mu\text{m}$ CMOS technology. Moreover, to reach 36Mbs^{-1} rate, OOK modulation can be used with a pulse magnitude of 1.73V leading to a good detection [17]. To achieve $g_0 = 1.73\text{V}$ with 3dB loss and $\tau = 75\text{ps}$, A_{max} must be equal to 2.56V. Such a value can not be directly obtained in the technology targeted because $A_{max} > 1.2 = V_{dd}$. As a consequence the filter must be driven in current mode as shown in the next section. Last of all, there is no limitation due to the peak power in RBW_{pk} for OOK modulation having $g_0 = 1.73\text{V}$.

III. PULSE GENERATOR DESIGN

Fig. 4 shows the entire topology of the proposed pulse generator. The generator consists in a edge combiner that uses varying differential delay cells and a fast logic gate. A transistor is then used to drive the filter in current mode to produce the magnitude needed ($A_{max} = 2.56\text{V}$) at the filter input.

A. On Chip Filter Design

The design of the pulse generator is mainly determined by the performance of the passive devices of the technology used and especially the inductors. Due to the metal thickness and the substrate loss, CMOS technology provides inductors with low Q factor. The low order needed to achieve a FCC

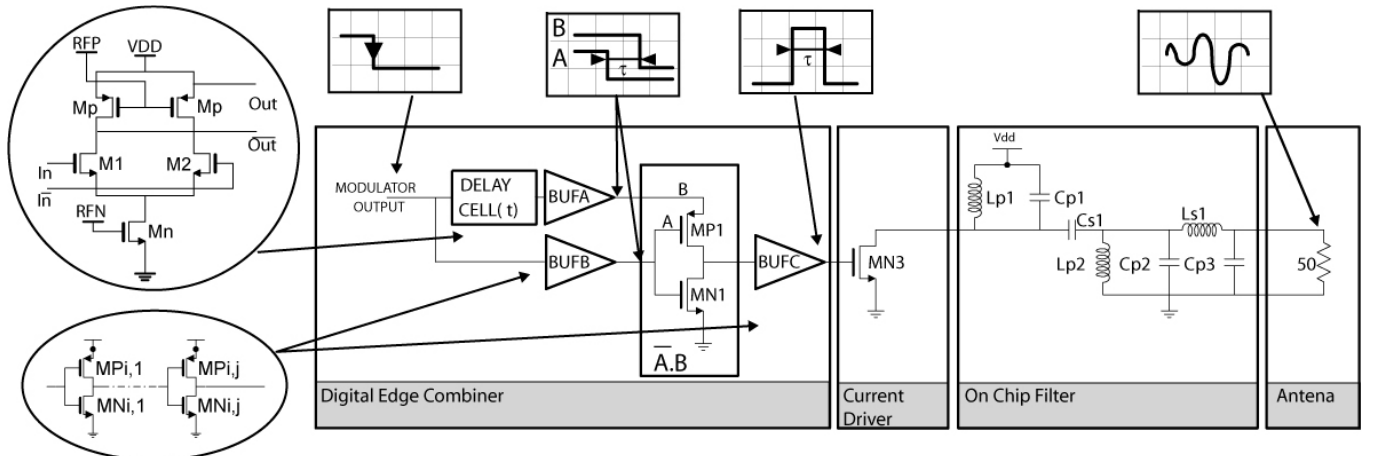


Fig. 4. Pulse generator architecture

compliant pulse is a great advantage for the design of a filter with low Q devices because it limits the power loss (<3dB). Moreover, the values of the Q factor and of the Self Frequency Resonance (SFR) vary with L. It is then necessary to evaluate the technology to determine which values of inductors achieve admissible Q factor (around 10) in the overall bandwidth. This means that the range of inductor values to be used is limited. For the 0.13 μm CMOS technology used for this design, the range is around 400pH<L<1.5nH. Lower values of inductors leads to inductor with Q<10 and higher values of inductors leads to SFR lower than 15GHz. Due to the large relative bandwidth of the FCC mask, the dispersion on the inductor values needed to implement a FCC compliant filter is low and filters can be achieved with such a narrow range. For the 3rd order Bessel considered in this design, the values are listed in TABLE 1 and are in the range. Moreover, different filter structures can be evaluated to find the best inductor values. In our design, as shown in Fig. 4, the filter topology used is a modified ladder structure.

B. Filter Driver Design and Matching

In our case study, the magnitude of the baseband pulse needed exceeds the voltage supply. Obviously, the filter is driven in current mode. The sizing of MN3 depends on the filter input impedance and A. In the case where g(t) is a square function with magnitude equal to V_{DD} , the current given by MN3 to the load during the time τ can be approximated using the MOS current law $I_D(V_{GS})$ with $V_{GS}=V_{DD}$. Under this assumption the width of MN3 can be expressed as follows:

$$W = \frac{LA}{R_{IN} \cdot \mu_0 \cdot C_{ox} (V_{DD} - V_t)^2} \quad (15)$$

where R_{IN} is the filter input impedance and is equal to the load impedance in most of the passive filter if the loss is ignored. The current needed to drive the 50 Ω impedance is then $I_0=(A_{max})/50=51\text{mA}$ which implies a large transistor. The output of such a wide transistor influences the filter transfer function and can involve matching loss. During the conduction time (τ) of MN3, the output (R_{ds} and C_{ds}) can be approximated using small signal hypothesis leading to the electric scheme in Fig. 5. To match the driver to the filter, MN3 must be sized to have R_{ds} equal to R_{IN} . Because both R_{ds} and I_0 depend on MN3 width (W_{MN3}), it is not possible, with such a simple topology, to size MN3 to have $I_0=51\text{mA}$ and, at the same time, $R_{ds}=R_{IN}$. It is then necessary to make a trade-off between the driving current (I_0), the matching (R_{ds}), and the power consumption (W_{MN3}). For the considered design the width of the transistor is set to 100 μm which leads to the intrinsic characteristics given in TABLE 2. Due to the mismatch ($R_{ds}=122\Omega$ instead of 50 Ω), the value of I_0 is increased to 58mA (instead of 51mA) in order to ensure that $g_0=1.73V$ as shown in Fig. 10. A wider transistor would

TABLE 1 : FILTER'S COMPONENT VALUES

Lp1 (nH)	Cp1 (pF) (ideal)	Cp1 (pF) (Real)	Cs1 (fF)	Ls1 (nH)	Lp2 (nH)	Cp2 (fF)	C3 (fF)
460	1.43	0.5	677	1.15	1.08	420	260

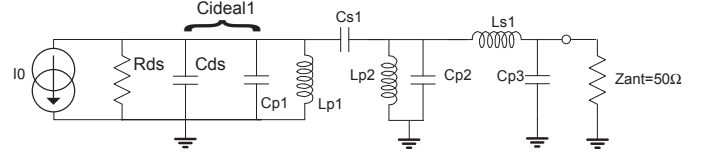


Fig. 5. Electrical scheme of the driver and the filter.

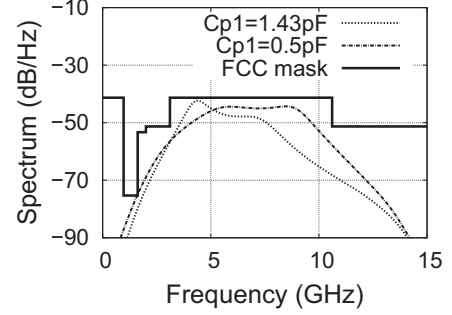


Fig. 6. Compensation effect on the output pulse spectrum .

have a lower R_{ds} and would better match the filter but would increase the power consumption.

To avoid transfer function distortion, the effects of C_{ds} can be easily cancelled by taking C_{p1} equal to its ideal value minus C_{ds} . As shown in Fig. 6 the main effect of C_{ds} on the filter transfer function is to reduce the 10dB bandwidth.

The drain of MN3 is biased using the first filter resonator to avoid the use of additional inductor. The gate is not biased to operate in C class. As a result, the filter does not consume DC power while no pulse is transmitted resulting in good power consumption performances.

C. Digital Edge Combiner Design

The technique used in the baseband pulse generator consists in propagating an edge through a delay cell. The pulse is then obtained by combining the input and the output of the delay cell using a logic function. Generation of accurate delay requires a phase locked loop and is not suitable for low cost systems. The delay variation mainly impacts α which is equivalent to additional loss. However, a small variation does not impact the output magnitude very much and only tunable delay cells are used in this design principally to compensate process variation. The delay cell used is the modified differential MOS Current Mode Logic inverter [18] depicted in Fig. 4. The control voltage (V_{ctrl}) and V_{DD} are respectively applied to RFP and RFN pins. In this configuration Mp and Mn act like resistors and no additional capacitor is needed. The width of Mp and Mn is set to 0.5 μm . The output voltages are : $V_{OL}=0.3V$ and $V_{OH}=1.2V$ and the delay achieved by the cell varies from 17ps to 300ps which gives to the cell a large tuning capability.

TABLE 2 : VALUES OF THE EXTRACTED NMOS TRANSISTOR HAVING 100 μm WIDTH, 0.13 μm LENGTH AND BIASED TO $V_{GS}=1.2V$ AND $V_{DS}=1.2V$

I_{dson}	58 mA
G_{ds}	7.59 mS
C_{ds}	240 fF

The combination of the two edges can be achieved by a large variety of logic gate. The speed of the gate is very important to generate short pulses having sufficient magnitude. The logic function used here needs only 2 transistors to operate, allowing high speed transition. The cell achieves A and not B, which generates pulses only on negative edges.

Due to the difference between the transistor size of the delay cell and of the filter driver, buffers are needed to ensure the signal integrity. The buffers consist in serial inverters sized with the fan out law to make a smooth transition between the delay cell and the driver transistor sizes.

IV. MEASUREMENT AND SIMULATION RESULTS

The pulse generator has been designed with a 0.13μm standard CMOS technology from ST Microelectronics. The die is shown in Fig. 7 and its area is 0.54mm².

A. Digital Edge Combiner Results

The performances of the triangular pulse generator depend on the load of the filter driver MN3 and accurate measurement is difficult to achieve. Simulations using the design kit and post layout extraction are presented here. The impulse output signal of the gate and its Fourier transform are depicted in Fig. 8 and Fig. 9 for different values of the delay cell control voltage. The gate is able to generate impulse with a minimal width of 46ps having 1.2V voltage magnitude. For a 0.4V control voltage, the pulse width is 75ps and the Fourier transform is almost flat in the FCC band which denotes good spectral efficiency and good pulse quality.

B. UWB Pulse Measurement

Measurement achieved with a 12GHz real time oscilloscope (Agilent DSO81204B) and simulations concord well as shown in Fig. 10. Taking into account the cable loss, the peak to peak magnitude is 1.42V instead of 1.73V. This results in a lower detection but increases the rate capability up to 43.8Mbs⁻¹. The width of the pulse is 460ps, and its 10dB bandwidth is 6.8GHz. As shown in Fig. 11, the compliance with FCC mask is good and the bandwidth of the pulse is very large. Due to this very large bandwidth, the PSD of the modulated signal (s(t)) must be lower than the PDS_{max} imposed by FCC to avoid emission in the forbidden frequency band around 1GHz. This limits the rate and finally, the maximum value is 38Mbs⁻¹. As shown in Fig. 12 the spectrum of a 36Mbs⁻¹ OOK modulated signal complies with the FCC mask.

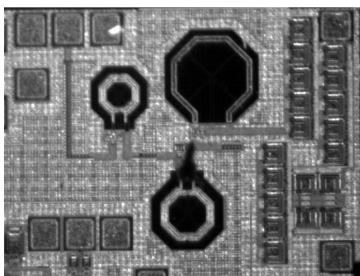


Fig. 7. Die Photographe.

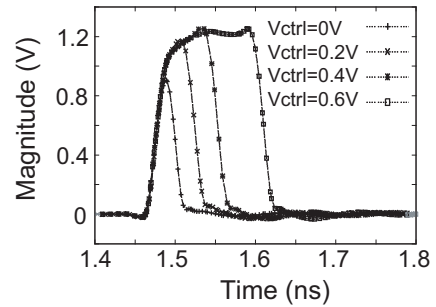


Fig. 8. Time simulation of the Baseband pulse for different control voltages.

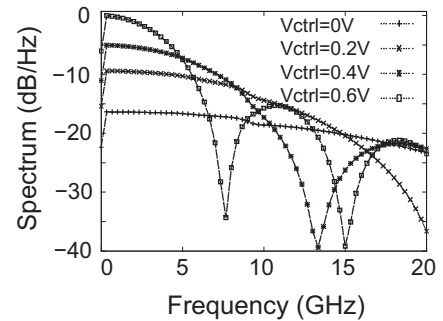


Fig. 9. Comparison of the Fourier transform of the baseband pulse for different control voltages

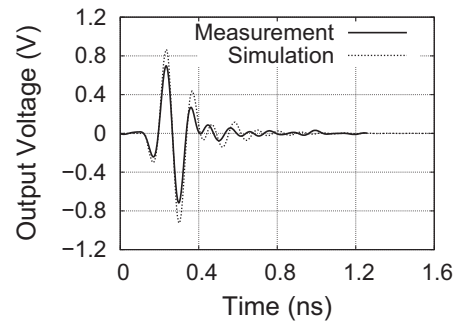


Fig. 10. Time simulation and measurement of the pulse generator output

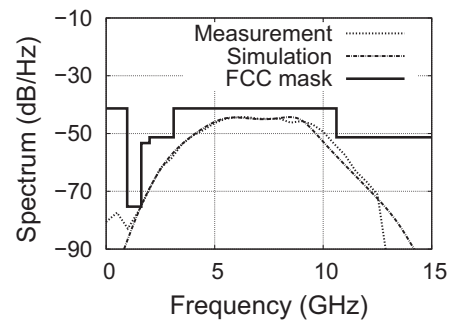


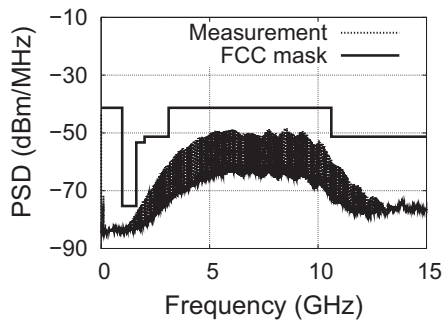
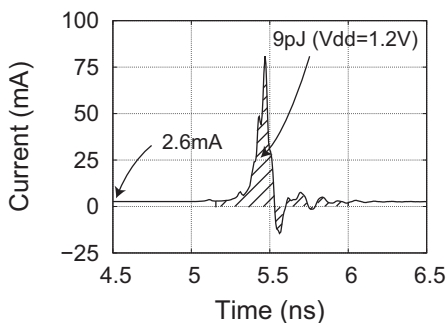
Fig. 11. Simulated and measured output spectrum

TABLE 3 : PERFORMANCE SUMMARY OF PROPOSED GENERATOR AND COMPARISON WITH PREVIOUS WORKS

Ref.	V _{pp} (V)	V _{dd} (V)	Width (ns)	BW (-10dB)	CMOS (μm)	Power Cons.	E _p (/pulse)	η (pJ/p/V)	Area (mm ²)	Technique	Modulation
[19]	1,24	2,2	1,75	1,4GHz	0,18	29,7mW@36MHz	nc	nc	0,4(core)	Digital Pulse Combining	DBPSK
[20]	0,18	1,5	3,5	500MHz	0,18	1,82mW@100MHz	18pJ	100	0,39(die)	OL switching	OOK
[21]	0,9	1,8	2,5	1,2GHz	0,18	1,8mW@10Mp/s	180pJ	200	1,21(die) / 0,57(core)	OL switching	BPSK
[10]	0,65	1	3	550MHz	0,09	nc	47pJ	72.3	0,08(core)	Digital Pulse Combining	DBPSK
[8]	0,16	1,5	3,5	520MHz	0,18	1,68mW@100MHz	16,8pJ	105	0,3(core)	OL switching	OOK
[7]	0,673	1,8	500ps	4,5GHz	0,18	nc	27pJ	41,5	0,11(die)	OL switching	OOK
[13]	0,35 to 0,45	1,2	0,6 to 0,8	2-4GHz	0,13	10mW@160MHz	nc	nc	1,56 (die)	Filtered Edge Combination	PPM/BPSK
This work	1,42	1,2	0,46	6,8GHz	0,13	3,84mW@100MHz	9pJ	6.4	0,54(die)	Filtered Edge Combination	OOK

C. Power and Energy Consumption

The major interest of the presented structure is its very small amount of energy needed to generate large pulses. The energy consumed by pulse is estimated to be 9pJ, as represented in Fig. 13, which is a very good performance regarding literature. This very good performance relies on two aspects. First, the pulse generated has a very wide spectrum which leads to a very short duration and limits the time conduction of the transistors. Second, the filter driver which consumes the major amount of power, operates in C class mode and has no DC power consumption. The DC consumption is 3.2mW and is mainly due to the differential delay cell. The total power consumption is 3.84mW@100Mhz and is linearly dependent on the rate. Moreover, the DC power can easily be decreased to zero by using classic CMOS logic gate in the edge combiner especially for very low power applications like RFID or sensor network.

Fig. 12. PSD of a 36Mbps⁻¹ OOK modulation using the proposed generatorFig. 13. Simulation of the current consumption with V_{dd}=1.2V

For low cost systems that use energy detectors, an important criteria is the energy by pulses relative to the pulse magnitude :

$$\eta = \frac{E_p}{g_0} \quad (16)$$

When the consumed energy is compared to the pulse magnitude, the presented generator also performs well since it achieves 6.4pJ/Pulses/V.

V. CONCLUSION

The design of a low power and high voltage pulse generator has been presented. It uses a bandpass filter excitation technique for which a sizing method, based on the average PSD, has been presented. The generator is fully integrated in a 0.13μm CMOS technology on 0.54mm². It consumes 9pJ by pulses and generates a 1.42V_{pp} pulse. It can be used in the FCC band with OOK modulation and rates up to 38Mbps⁻¹. Regarding its performances, this generator appears to be very well suited for low cost and low power applications.

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