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# Transimpedance instrumentation amplifier based on current inversion

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**Abstract** — this paper presents a novel instrumentation amplifier operating a differential current measurement from a resistive bridge. The proposed transimpedance instrumentation amplifier is constructed with two voltage opamps. One opamp is used to realize the current inversion and the second as a single input transimpedance amplifier. The resistive bridge is biased by a DC current and that it differs from the traditional voltage Wheatstone bridge. Simulation results by PSpice from a full custom 0.35μm CMOS opamp (BSIM transistor models) and the commercially LT1097 from linear technology (macro-model) show well performances of the proposed topology and confirm the validity of the circuit. Under ±2V opamps supply voltages, the CMOS full custom configuration consume 273μW per MHz and provides a linear sensitivity of 5mV/Ω.

## I. INTRODUCTION

Instrumentation amplifier (IA) is one of the most important building blocks in the design of analog front-end dedicated to sensor networks and measurement systems [1-4]. Measurement could be made from a single or multiple impedance variations from pressure gauges for example [1-4]. The strain gauges permit to provide impedance-variations which depend on the pressure, i.e.  $R+\Delta R$  or  $R-\Delta R$  in case of resistive variations. A current measurement technic that employs a current-mode Wheatstone bridge and voltage operational amplifiers has been introduced in [1] and some additional implementations in [6-9]. The goal of this paper is to present a new versatile solution using a current type resistive bridge. The main modification consists to add a current negative impedance converter (INIC) in order to cancel the input current offset before to apply the amplification [9]. The topology proposed in this paper is based on two voltage opamps which offers wide precision and the possibility to be implemented in full custom or by using commercial devices.

**Traditional voltage mode Wheatstone bridge (VWB):** Fig.1a and Fig.1b shows the traditional voltage mode Wheatstone bridge (VWB) [1]. Here, the differential voltage amplifier of gain  $A_D$  must provide an infinite input impedance at node  $in+$  and node  $in-$ . The VWB concerns typical applications based two possible sensor variations. Considering  $R_A=R_{A0}+\Delta R_A$ ,  $R_B=R_{B0}+\Delta R_B$ ,  $R_D=R_{D0}$  and  $R_C=R_{C0}$  with  $R_{A0}=R_{B0}=R_{D0}=R_{C0}=R$ , this two typical cases are: i)  $R_A=R+\Delta R$ ,  $R_B=R-\Delta R$  and ii)  $R_A=R+\Delta R$ ,  $R_B=R$ . The study presented in this paper will consider the first case, but could easily be extended to the second case when  $\Delta R \ll R$ . Then from Fig.1, considering  $R_A=R+\Delta R$ ,  $R_B=R-\Delta R$ ,  $R_{D0}=R_{C0}=R$ , for  $V_{DD}=-V_{SS}=V_0$ , we have for an ideal instrumentation amplifier of gain  $A_D$ :

$$V_{out} = A_D(V_A - V_B) = \left[ \frac{A_D V_0}{R} \right] \Delta R = S \Delta R \quad (1)$$

where  $S$  is the IA sensitivity. In non-ideal case, the IA exhibits an output voltage offset and (1) becomes:

$$V_{out} = S \Delta R + V_{OFF} \quad (2)$$

Theoretically, the output offset  $V_{OFF}$  exists due to the common mode gain ( $A_{CM}$ ) of a real IA and imprecise set of resistances or supply voltages, both for the bridge and the IA.

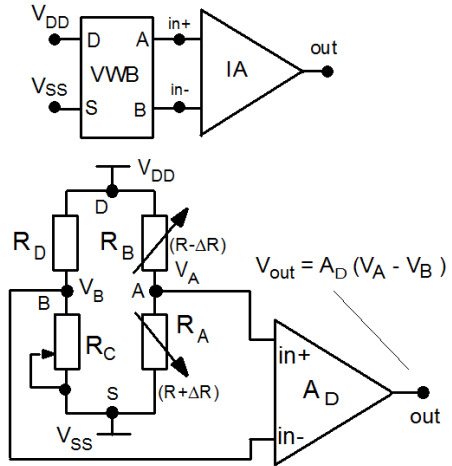


Fig.1: Typical voltage mode Wheatstone bridge (VWB) followed by a differential voltage instrumentation amplifier,  $R_C$  is use here for offset compensation.

Note that an Instrumentation amplifier with high *common mode rejection ration* (CMRR) will considerably reduce the amplification of the common mode voltage  $V_{A0}+V_{B0}$  were  $V_{A0}$  and  $V_{B0}$  are the effective DC voltages at node A and B. Unfortunately the necessary and inherent differential gain  $A_D$  will drastically amplify the differential input offset  $V_{AB0}=V_{A0}-V_{B0}$ . In summary, to reduce the output offset  $V_{OFF}$ :

- The CMRR must be high
- The differential DC voltage between node A and B must be as close as possible.

The CMRR of the VWB is described by:

$$V_{out} = A_D(V_A - V_B) + \frac{A_{CM}}{2}(V_A + V_B) \quad (3)$$

$$\text{with } CMRR = 20 \cdot \log \frac{A_D}{A_{CM}} \quad (4,5)$$

A simple manner to reduce the differential offset consist in setting  $R_C$  (see Fig.1) or  $R_D$ .

**Equivalent current mode resistive bridge (CRB):** Azhari and Kaabi proposed in [5] a versatile measurement technic using an equivalent “current-mode” resistive bridge (CRB) also called current mode Wheatstone bridge (CMWB). The corresponding topology is shown in Fig.2a and Fig.2b. Note that the differential current amplifier must, ideally, provides a zero input impedance at node  $in+$  and node  $in-$ .

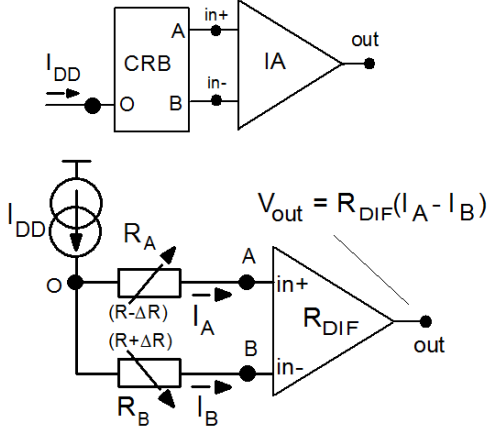


Fig.2: Current mode resistive bridge (CRB) followed by a differential transimpedance instrumentation amplifier [5].

Considering the same type of variations of  $R_A$  and  $R_B$  than the VWB previously discussed we have, when  $R_A=R+\Delta R$ ,  $R_B=R-\Delta R$  and for  $I_{DD}=I_0$ :

$$V_{out} \cong \left[ \frac{R_{DIF} I_0}{R} \right] \Delta R + V_{OFF} = S \cdot \Delta R + V_{OFF} \quad (6)$$

where  $S$  is the sensitivity in  $V/\Omega$  and  $V_{OFF}$  the DC output voltage offset; considering the common mode transimpedance, we also have:

$$V_{out} = R_{DIF} (I_A - I_B) + \frac{R_{CM}}{2} (I_A + I_B) \quad (7)$$

$$\text{with } CMRR = 20 \cdot \log \frac{R_{DIF}}{R_{CM}} \quad (8,9)$$

where  $R_{DIF}$  is the differential transimpedance and  $R_{CM}$  the common mode transimpedance of the instrumentation amplifier (current inputs, voltage output). A low differential offset is obtain for quasi zero input impedance at node  $in+$  and  $in-$  in conjunction of a good matching between  $R_{A0}$  and  $R_{B0}$ . The circuit proposed in this paper offer a simple and versatile solution to cancel the output offset  $V_{OFF}$  from a single resistance and to provide a low input differential offset when  $R_{A0}$  is close to  $R_{B0}$ . Moreover the proposed configuration will not need high CMRR because the offset will be compensate before amplification [6].

In section II, the proposed current-inputs voltage-output instrumentation amplifier based a resistive bridge is presented and a theoretical analysis is given. Simulation results and discussions are proposed in section III. In section III two configurations are simulated and discussed 1) a full custom integration based on a CMOS 0.35 $\mu m$  typical process [10] and 2) a configuration based on two commercially opamps: the

LT1097 from Linear Technology [11]. These two configurations were simulated with PSpice using the BSIM 3V3 transistor models for the CMOS full custom design and using the LT1097 macro-model from Linear Technology.

## II. PROPOSED TRANSIMPEDANCE INSTRUMENTATION AMPLIFIER

Fig.3 shows the synopsis of the instrumentation amplifier [9] and Fig.4 the proposed novel implementation based on two voltage opamps. The circuit is composed by a I(current) negative impedance converter (INIC) and followed by a transimpedance amplifier having a transimpedance equal to  $-R_F$ . This output amplifier amplify the current difference  $I_E = I_B - I_A$  “only” by  $V_{out} = R_F (I_A - I_B)$ ; in this ideal case  $R_{DIF} = R_F$  and  $R_{CM} = 0$  (see Fig.2). Considering a typical voltage instrumentation amplifier, one goal is to obtain a very low common gain (high CMRR) in order to cancel the common input offset voltage. Here the interest of having a low CMRR is not justified if the compensation offset of  $I_E$  ( $I_{OFF}$ ) is done from the INIC by introducing a current gain  $\alpha$  between the INIC output and input. This approach is then less different than a general view which consider the amplification (difference) of two input currents  $I_A$  and  $I_B$  at nodes  $in+$  and  $in-$ , because here  $I_E$  is the only one input current that will be amplify. This means that in order to cancel the output offset voltage  $V_{OFF}$ , we only need to compensate  $I_{EOFF}$ . We will shows that compensate the  $I_{EOFF}$  leads to an overall gain of  $R_{DIF} = (1 + \alpha) R_F$ . Then playing on  $R_F$  will permit to calibrate the sensitivity and playing on  $\alpha$  will permit to cancel the output voltage offset  $V_{OFF}$ .

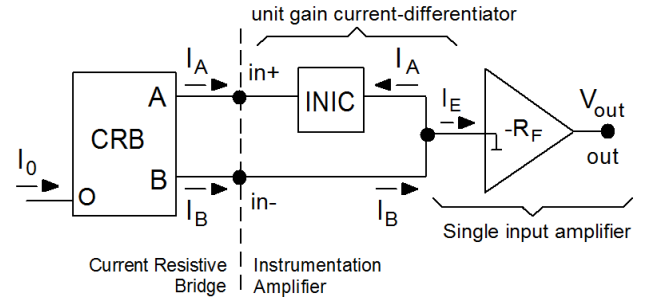


Fig.3: Synopsis of the Instrumentation Amplifier [9].

Fig.4 shows the current resistive bridge biased with the DC current  $I_0$  and the proposed instrumentation amplifier using two operational voltage feedback opamps OA1 and OA2.

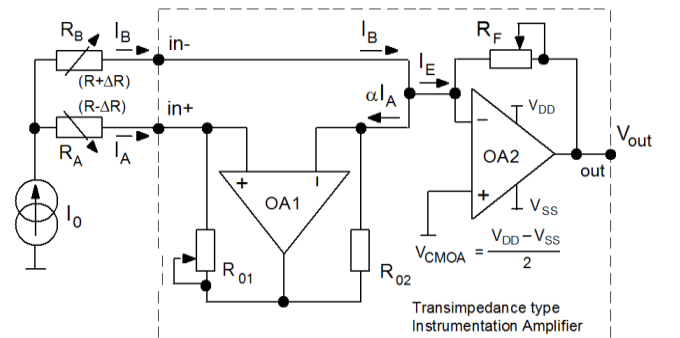


Fig. 4: Proposed transimpedance instrumentation amplifier.

Considering  $\alpha=1$ , compared to Fig.2, the amplifier OA2 amplify the input current  $I_E = I_B - I_A$  by a factor of  $-R_F$ . The voltage amplifier OA2 permits to provide an ideal zero loading inputs impedance at the node  $in+$  and the node  $in-$ . The part of the circuit composed by the opamp OA1,  $R_{01}$  and  $R_{02}$  simulate

the negative impedance converter shown in Fig. 3. Here the INIC convert a zero loading impedance. Operation of OA1 (INIC) gives  $R_{01}I_A = \alpha R_{02}I_A$  or:

$$\alpha = R_{01} / R_{02} \quad (10)$$

The output amplifier OA2 and the feedback resistance  $R_F$  realize a transimpedance amplification, we have:

$$V_{out} = R_F(\alpha I_A - I_B) \quad (11)$$

And from (11) we found:

$$R_{DIF} = \frac{1+\alpha}{2} R_F ; \quad R_{CM} = (\alpha-1)R_F \quad (12,13)$$

Then the sensitivity in  $V/\Omega$  is given by:

$$S = \left[ \frac{(1+\alpha)R_F}{2R} I_0 \right] \quad (14)$$

Playing on  $\alpha$  allows to directly acting on the output offset voltage. Effectively, considering  $I_{A0}$  and  $I_{B0}$  the DC current through  $R_A$  and  $R_B$  respectively, when  $\Delta R=0$ , we have:

$$V_{OFF} = R_F(\alpha I_{A0} - I_{B0}) = R_F \left( \frac{R_{01}}{R_{02}} I_{A0} - I_{B0} \right) \quad (15)$$

with :

$$I_A = \frac{R_{B0}}{R_{B0} + R_{A0}} I_0 ; \quad I_{B0} = \frac{R_{A0}}{R_{A0} + R_{B0}} I_0 \quad (16,17)$$

Because the transimpedance amplifier OA2 receives the difference between  $I_{B0}$  and  $\alpha I_{A0}$  only, high CMRR [6] is not a necessary condition to reduce  $V_{OFF}$ . Then in our case, degradation of the CMRR could be done in order to cancel the output offset voltage  $V_{OFF}$ . In real case a non-ideal output transimpedance amplifier (Fig.3) provides, when  $V_{OUT}=0$ , an inherent input current offset  $I_E(@V_{OUT}=0)=I_{OFF}$ . Considering this additional offset, a zero output voltage ( $V_{OFF}=0$ ) is obtained for:

$$\alpha I_{A0} - I_{B0} = I_{OFF} \quad (18)$$

and (15) must be rewritten as follows:

$$V_{OFF} = R_F(\alpha I_{A0} - I_{B0} - I_{OFF}) \quad (19)$$

Concerning an output offset voltage control of  $V_{OFF}$  from  $R_{01}$ , we have:

$$\Delta V_{OFF} / \Delta R_{01} = R_F I_0 / 2R_{01}. \quad (20)$$

### III. SIMULATION AND DISCUSSION

All simulations have been performed using PSpice simulator. Simulations are done using two types of voltage opamps: *i*) using the PSpice macro-model of the commercially LT1097 [11] and *ii*) using a two identical full custom two stages CMOS voltage opamps simulated with a BSIM 3V3 typical transistor models from AMS [10]. Transistor Level description of the CMOS design is shown in Fig. 5 were  $I_B$  is the CMOS opamp DC bias current. Table I resume the transistor sizes and post-layout estimated drain and source areas and perimeters in order to compute the junction capacitances.

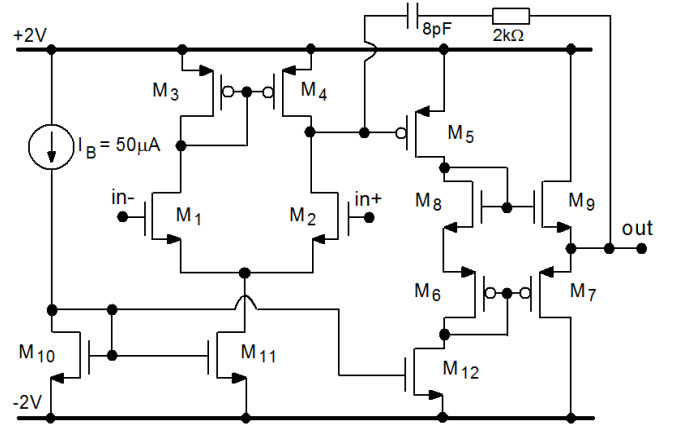


Fig. 5: Typical CMOS 0.35μm two stages voltage opamp.

**TABLE I**  
TRANSISTORS SIZES AND EQUIVALENT DRAIN AND SOURCE AREAS  
(AD, AS) AND PERIMETERS (PD, PS)

transistors	W (μm)	L (μm)	AD=AS (m <sup>2</sup> )	PD=PS (m)
M <sub>1</sub> , M <sub>2</sub>	150	0.5	131E-12	135E-6
M <sub>3</sub> , M <sub>4</sub> , M <sub>5</sub> , M <sub>6</sub> , M <sub>7</sub>	60	0.5	76E-12	63E-6
M <sub>8</sub> , M <sub>9</sub> , M <sub>10</sub> , M <sub>12</sub>	30	0.5	38E-12	33E-6
M <sub>11</sub>	60	0.5	76E-12	63E-6

Fig.6 shows the simulated variation of  $V_{OFF}$  and  $\alpha$  versus  $R_{01}$  for the CMOS configuration. A quasi-offset cancellation is obtained for  $R_{01}=10104\Omega$  ( $\alpha=1.00948$ ). The corresponding sensitivity is shown in Fig.7. The value of  $R_{01}=10104\Omega$  does not correspond to an optimum CMRR, however this clearly cancel the output offset and does not impact the linearity of the sensitivity  $S$  defined by the equation (14). For the LT1097 configuration, the offset cancellation is obtained for  $R_{01}=10006\Omega$  ( $\alpha=1.0006$ ) and the corresponding sensitivity is also shown in Fig.7.

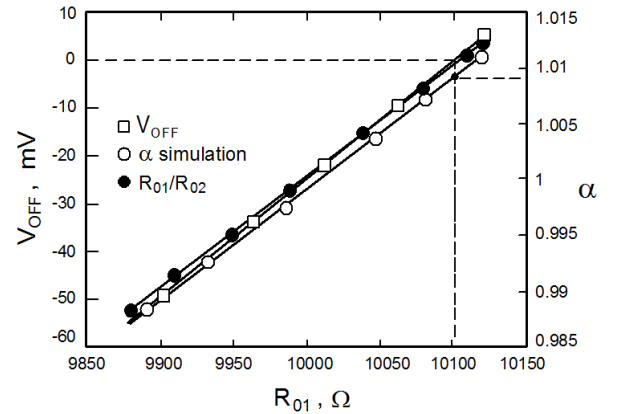


Fig.6: Offset cancellation of the CMOS configuration from  $R_{01}$  ( $R_{A0}=R_{B0}$ ).

In Fig.6, the accuracy of the control of the output offset voltage  $V_{OFF}$  is  $250\mu V/\Omega$ ; which match with the equation (20). Table II resumes the mains simulated performances for the two configurations. Table II is given for  $R_{A0}=R_{B0}=1k\Omega$  and a quasi-zero output offset voltage obtained with  $R_{01}=10104\Omega$  and  $R_{01}=10006\Omega$  for the CMOS and LT1097 configurations respectively. In case of  $R_{A0}=1k\Omega$  and  $R_{B0}=1010\Omega$ , the values of  $R_{01}$  that permits to obtain  $V_{OFF}=0$  are respectively for the CMOS and LT1097 configurations  $R_{01}=10000\Omega$  ( $V_{OFF}=20\mu V$ ) and  $R_{01}=9905\Omega$  ( $V_{OFF}=73\mu V$ ). This also demonstrates the capability to compensate the deviation between  $R_{A0}$  and  $R_{B0}$  from  $\alpha$  by acting on  $R_{01}$ .

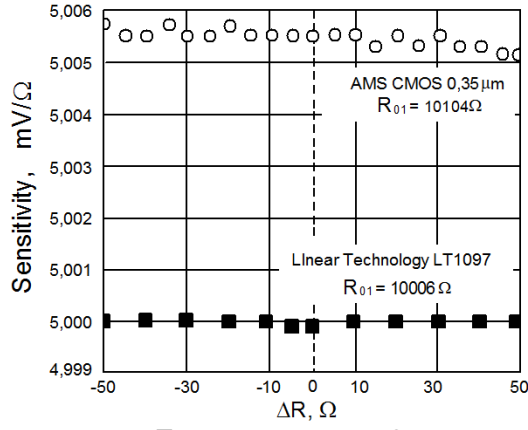


Fig.7: Output sensitivity: ■ LT1097 (macro-model) ○ CMOS Full custom (BSIM3V3).

In Table II the total power consumption of the CMOS configuration is about  $273\mu\text{W}$  per MHz; this mean that in case of low bandwidth sensor variation of few Hz, an ultra-low power CMOS design of the opamp could be considered. Here the GBW (*gain bandwidth product*) of the CMOS configuration ( $I_B=50\mu\text{A}$  in Fig. 5) is 13MHz and the opamp consumes 1mW (13MHz/1mW); for example this become 2.8MHz/112μW when  $I_B=15\mu\text{A}$ .

TABLE II

MAIN SIMULATED PERFORMANCES FOR  $R_F=100k\Omega$  AND  $I_0=50\mu\text{A}$ ,  
 $R_{A0}=R_{B0}=1k\Omega$ ,  $V_{DD}=-V_{SS}=2\text{V}$ ,  $I_B=50\mu\text{A}$

Parameters	CMOS 0.35μm	LT1097 Linear Technology	
$R_{01}$	10 104	10 006	[Ω]
$R_{02}$	10 000	10 000	[Ω]
$I_{A0}$	24.886	24.995	[μA]
$I_{B0}$	25.114	25.005	[μA]
$I_{OFF}$	7.57	-4.31	[nA]
$V_{OFF}^{(1)}$	830	447	[μV]
$\alpha-1$	0.00948	0.0006	-
Sensitivity (S)	5.0056	5	[mV/Ω]
S-Deviation	±40	±20	[ppm]
Power consumption	2.19	3.14	[mW]
Bandwidth <sup>(2)</sup>	8 (-3dB)	0.1 (+3dB)	[MHz]

(1) The precision is  $250\mu\text{V}/\Omega$  and match with equation (20).

(2) Done with AC input currents @ in+ and in- (Fig.8, Fig.9).

In case of the simulation conditions of table II, Fig.11 and Fig.12 show the evolution of  $R_{DIF}$  and  $R_{CM}$  versus the frequency variation of  $I_A$  and  $I_B$  for the CMOS and the LT1097 configurations. As discussed before for the circuit discusses in this paper, reaching a low CMRR is not in our case a design objective for canceling the output voltage offset. In Fig.7, the sensitivities deviation are not higher than 40ppm for a resistive sensor(s) variation of 10% (i.e.  $\Delta R/R=0.1$ ).

#### IV. CONCLUSION

A novel instrumentation amplifier based on a current resistive bridge were introduced in this paper. The proposed voltage output instrumentation amplifier is based on two operational voltage opamps and 3 resistances only. It has been shown that the output offset voltage can be easily controlled from a single resistance. Simulation of a full custom CMOS design and using the commercially LT1098 have in both case demonstrated the circuit feasibility. This versatile topology could advantageously

replace topologies based on the traditional VWB, particularly when it is more convenient to have a bridge DC current supply instead of a DC supply voltage.

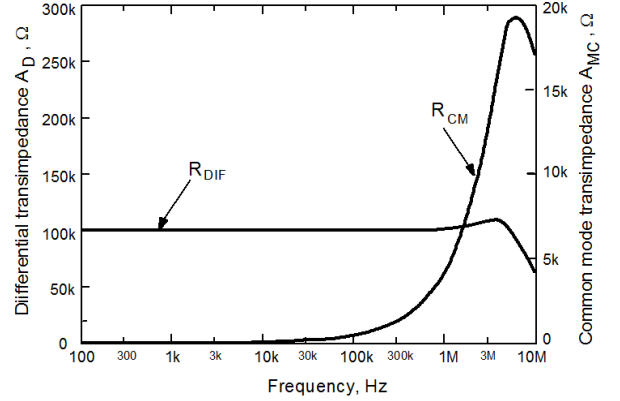


Fig.8: Frequency responses of the proposed CMOS instrumentation amplifier.

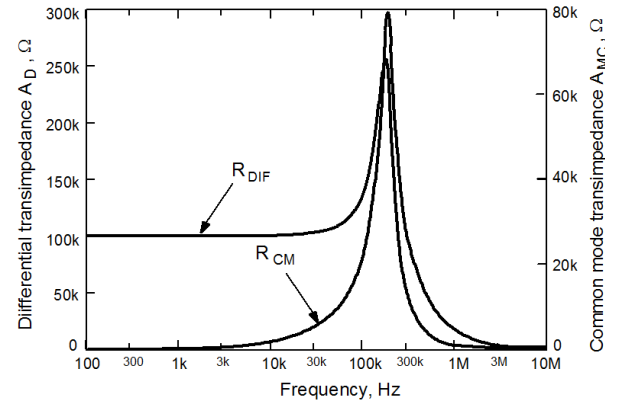


Fig.9: Frequency responses of the proposed instrumentation amplifier simulated with two LT1097.

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