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A Low Cost Impedance Measurement Method for Integrated Circuits

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Abstract: Impedance matching of a Radio Frequency (RF) device antenna with its integrated circuit chip is necessary to improve efficiency and RF communication quality. This matching can only be done if one knows the chip components impedances. This paper presents a new RF measurement method to determine electrical characteristics like s-parameters or impedance of smart cards integrated circuits or antennas, using common measurement devices as a computer, an oscilloscope or any voltage acquisition device, and a directional coupler. Achieved results are compared with vector network analyzer (VNA) measurements and the method is applied to real contactless integrated circuit proximity cards components.

Keywords: NFC, Impedance measurement, Proximity cards, S-parameters

1 Introduction

Passive contactless Proximity Integrated Circuit Card (PICC) consist in an integrated circuit (the chip), and an antenna connected to the chip in order to power it and allow the chip to communicate with a reader device, as shown in Fig. 1. These cards do not involve batteries, and are supplied directly by the reader that provide a time-varying magnetic field while communicating with the card. This technology has experienced a strong development recently, and especially cards communicating with readers by modulating a carrier of 13.56MHz. Indeed, several billions of these cards are on the market today, for identification in the transport, or in contactless payment applications.

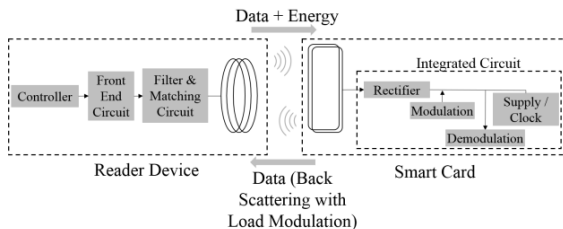


Figure 1 Principles of Contactless Smart Card Operation

In order to maximize the power transfer between the reader device and the chip, it is necessary to match the antenna of the card to its chip so the antenna impedance equals the conjugate of the chip's impedance. This design constraint becomes even more important as standards

evolve to Very High Bit Rate (VHBR) communications between the reader and the chip [1]. Indeed, as the data rate increases, the bandwidth of the communication signal increases, such that the quality factor of the antenna has to be lowered (from 128 to 1 or 2 when one wants to communicate up to 6.78Mb/s). Thus, it is of great importance for cards manufacturer to know perfectly the impedance of each component so the design optimizes the power transfer. However, it is difficult to measure this impedance with standard instruments since the operating voltage can exceed 2V_{rms}. This is why, a custom impedance characterization technique has been developed in [2] to determine PICC chips' impedance as a function of input power. The issue with such a method is that it requires expensive and special equipment as a vector network analyzer in order to measure chips' impedance.

In the present paper, this existing technique in [2] which uses particular equipment as a network analyzer has been adapted to allow PICC chip impedance measurements from common devices like oscilloscopes connected to a computer. It allows the user to measure chips' impedance from the switched off state (very low voltage sent to the chip) up to the destruction level, in order to characterize completely the chip behavior, and thus adapt the antenna impedance to the chip. Furthermore, it also makes it possible to determine the chip impedance during a communication at any data rate.

This paper is organized as follows. Section II deals with the existing chip impedance measurement technique, while section III presents the proposed novel algorithm implemented in a computer connected to an oscilloscope. This allows to determine the chip impedance in different states, including high operating voltages. Finally, section IV presents and comments measurement results obtained with the different techniques on real smart card chips.

2 Chip Characterization: Network Analyzer Based Method

The measurement of chips impedance using network analyzers implies the use of a bi-directional coupler, an amplifier, and an attenuator for instruments protection, as shown in Fig. 2.

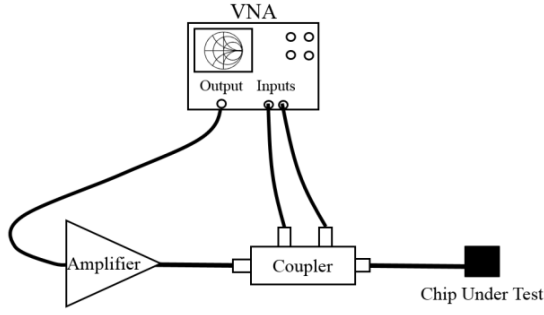


Figure 2 Set Up for Impedance Measurements using VNA

The way the network analyzer works in this set up is that it computes the reflection coefficient Γ_c at the connection of the chip by computing the ratio between the reflected and the incident waves voltages measured from the coupler device outputs. Then, from the reflection coefficient, one can determine the impedance of the considered chip by considering the equivalent chip admittance Y_c constituted by R_c in parallel with C_c . The aim of the method also presented in [2] is to determine Y_c from a one-port S parameter measurement using the following equation:

$$Y_c = \frac{1}{Z_o} \cdot \frac{1 - S_{11}}{1 + S_{11}} \quad (1)$$

where Z_o is the reference impedance generally equal to 50Ω and S_{11} , the S parameter of the chip, measured by the network analyzer.

A generic algorithm used to determine the reflection coefficient from the incident and reflected wave extracted by the coupler is now studied. First of all, it is necessary to recall the definition of the S-parameter of a device [3]. S-parameter can be defined as follows:

$$\underline{S_{11}} = \frac{b_1}{a_1} \quad (2)$$

Where b_1 is the reflected wave and a_1 the incident wave that are recorded from the two outputs of the coupler.

However, dividing the reflected voltage by the incident wave voltage will not give accurate results for the coefficient reflection [4]: indeed, it is necessary to calibrate the measurement set up. Three kinds of errors can arise in the measurement of the incident and reflected wave: a directivity error, a tracking error, and a port match error. Fig. 3 displays a one-port device flowgraph that represents all possible signal paths and the errors due to these multiple paths.

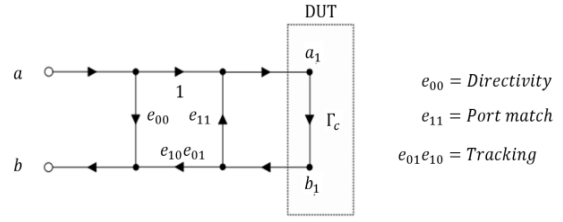


Figure 3 Flow Graph of a One Port Device

In this simplified model, errors due to the directional coupler, the cables, connectors, and the oscilloscope can be thought as due to a fictitious component placed between the coupler and the Device Under test (DUT), that modifies the incident and reflected waves amplitude and phase. Thus the measured reflection coefficient Γ_M includes these error sources, and has to be corrected in order to determine the chip's real reflection coefficient. One can determine the equation that links the measured (and thus incorrect) reflection coefficient Γ_M and the chip's real reflection coefficient Γ_c as shown in [4]:

$$S_{11M} = \Gamma_M = \frac{b}{a} = \frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} = \frac{e_{00} - \Delta_e \Gamma_c}{1 - e_{11} \Gamma_c} \quad (3)$$

Where A_r and φ_r are the reflected wave amplitude and phase respectively, and A_i and φ_i the incident wave characteristics. Thus,

$$\Gamma_c = \frac{\Gamma_M - e_{00}}{\Gamma_M e_{11} - \Delta_e} \quad (4)$$

with

$$\Delta_e = e_{00}e_{11} - e_{10}e_{01} \quad (5)$$

In order to determine the three unknown quantities e_{00} , e_{11} and Δ_e , the method consists in measuring the reflection coefficient Γ_M of three well-known loads whose real reflection coefficient (Γ_i) is known, and to solve the obtained system for the unknown error coefficients listed above.

Then, computing the real reflection coefficient of a given chip from the measurement of incident and reflected voltages can be done using (7). The last step for impedance computation is then achieved by using (2) and (3).

Thus, this straightforward method embedded within VNAs makes it possible to compute easily the impedance of a chip by determining its S-parameter. Now, an adaptation of this method will be studied in order to measure the chip's S-parameter without using a VNA, and even during a communication phase.

3 NOVEL CHIP CHARACTERIZATION TECHNIQUE

The method proposed in this article consists in replacing the network analyzer with an oscilloscope and a computer linked to the oscilloscope. Fig. 4 represents the setup for the measurement.

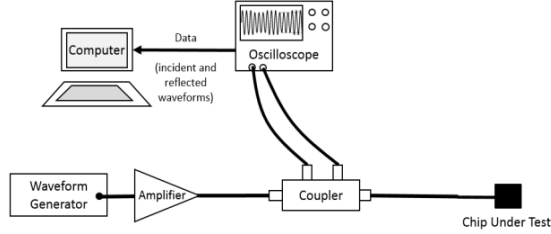


Figure 4 Low Cost Measurement Setup

In order to realize the measurement of the chip impedance, the proposed set up computes the reflection coefficient at the chip connection level. A waveform generator is used to generate the 13.56MHz carrier. It can be a common waveform generator, but can also be a reader device. Incident and reflected wave are then extracted by the bi-directional coupler and sent to the oscilloscope. The oscilloscope acts as an acquisition device that will then send the recorded incident and reflected voltages to the computer so it can process them. As explained above, it is necessary to first use a custom calibration kit to calibrate the setup, in order to take into account all the errors from the platform equipment. The algorithm used for computing the reflection coefficient from the two waveforms uses the same development as explained above. According to (4), the reflection coefficient can be computed as follows:

$$\Gamma_c = \frac{\Gamma_M - e_{00}}{\Gamma_M e_{11} - \Delta_e} = \frac{\frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} - e_{00}}{\frac{A_r}{A_i} e^{j(\varphi_r - \varphi_i)} e_{11} - \Delta_e} \quad (6)$$

Thus, it is necessary to determine A_k and φ_k from the incident and reflected voltages data recorded by the oscilloscope. The following processing is implemented within the computer: first, the amplitude can be determined by filtering numerically the signals to remove all noise and obtain the signal of interest that is the carrier at 13.56MHz.

$$x_{filtered}(l) = \frac{1}{N} \sum_{j=0}^{N-1} x(j) e^{\frac{-2i\pi[jk-lk]}{N}} \quad (7)$$

Where x is the incident (x_i) or reflected (x_r) wave signal, k is the index that corresponds to the 13.56MHz frequency, and N the number of points used in time domain. Then, amplitude of the signals A_r and A_i and corresponding phases can be determined by using Hilbert transform and analytical signals. Indeed, the amplitude of

a signal noted x can be computed using the following equation.

$$A_x = \text{median}(\|x_a(t)\|) = \text{median}_k(\|x(k) + j \cdot x_h(k)\|) \quad (8)$$

Where x_a is the analytical signal of x , $x_h(k)$ is the Discrete Hilbert Transform of the signal x , and can be determined as follows [5]:

$$x_h(k) = \frac{1}{N} \sum_{v=0}^{N-1} x(v) \left[1 - (-1)^{v-k} \cot\left(v - k\right) \frac{\pi}{N} \right] \quad (9)$$

Similarly, the phase difference between the incident and reflected signals can be computed as follows:

$$\Delta\varphi = \varphi_r - \varphi_i = \text{median}_k \left[\text{atan} \left(\frac{x_{r_h}(k)}{x_r(k)} \right) - \text{atan} \left(\frac{x_{i_h}(k)}{x_i(k)} \right) \right] \quad (10)$$

All these calculations are implemented within the computer, and allow A_x and $\Delta\varphi$ to be computed accurately with very few carrier periods, which means that the impedance of the chip can be computed with very low time steps, and even during the different phases of a communication.

4 CHIP IMPEDANCE MEASUREMENTS RESULTS

This method has been applied on different loads and chips in order to demonstrate its accuracy. First of all, a comparison with measurements done with vector network analyzer is presented, in order to validate the accuracy of the proposed method. Then tests in power have been done on real chips. To do the comparison with VNA measures, an impedance measurement of passive loads has been done twice, with two different measurement set up. First, loads were connected directly to a VNA, calibrated with its standard calibration kit. The other measurement set up was the one described in Fig. 4, where the DUT was replaced by the considering passive load. Three loads have been considered: a purely resistive load (100Ω), a standard calibration coil as described in [6] (inductive load), and finally a purely capacitive load. Results are displayed in Fig. 5 and Table 1.

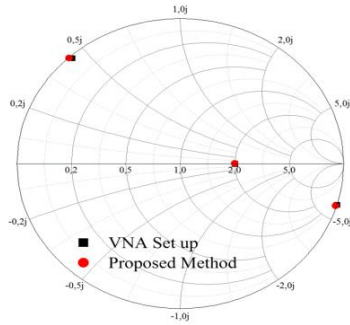


Figure 5 Impedance Measurement with VNA and low cost measurement set up

Table 1 Impedance Measurements and Comparison

| Impedance from VNA method (Ω) | Impedance from low cost method (Ω) | Real part error (%) | Imaginary part error (%) |
|--|---|---------------------|--------------------------|
| $99.96 + j0.3$ | $99.86 + j0.4$ | 0.1 | 0.7 |
| $0.46 + j22.1$ | $0.12 + j22.7$ | 1.5 | 1.8 |
| $0.6 - j346$ | $7.1 - j334$ | 2.08 | 3.46 |

The error being extremely low (comparable to the VNA measurement error), it is possible to validate this low cost measurement method, and to apply it for chip characterization at different states of operation.

Finally, the proposed method has been used to measure the impedance of a chip as a function of the incident power and thus as a function of the chip's state. Fig. 6 shows the impedance of the chip for a power ranging from -10 to 25 dBm measured with the method proposed in [2] and with the proposed low cost method. One can see that the measured impedance matches perfectly the VNA measurements.

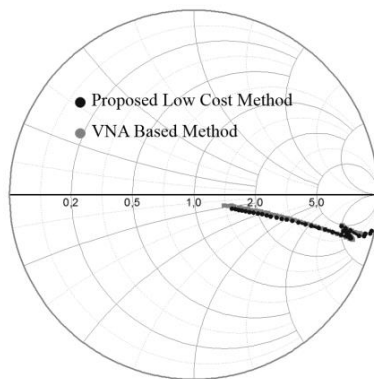


Figure 6 Chip Impedance Measurements Comparison

This validates the accuracy of this new chip impedance characterization method. In this section, it has been shown that an acquisition device and a computer for chip impedance characterization can replace a VNA, and provide accurate measurements with much smaller time steps. Furthermore, an other advantage of this method is that the waveform generator can be replaced by a reader device, in order to measure the chip impedance during a communication with a reader, which can be of great interest when designing a smart card.

5 Conclusions

With the increase of Near Field Communication products and evolutions such as VHBR, it is necessary to optimize the matching between chips and antennas. This matching has to be realized for specific operating states of the chips, and thus a method of impedance measurement over several power levels had to be provided. The proposed method in this article allows most of laboratories to realize their own impedance measurements with common measurement devices. Results of this method are comparable to results provided by VNA based measurement set-ups, which validates its performance. It has been used to measure a chip's impedance at different operating states in order to optimize the design of these chips depending on the application. Finally, as this method makes it possible to compute the chip's impedance at very short time steps, it will be applied to determine the impedance of a chip during a communication, and thus to measure the impedance changes during the different phases of load modulation

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