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A Fully Differential 7.2-8.5GHz LNA for a Self Synchronized and Duty-cycled UWB OOK Receiver

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Abstract—This paper presents a low power Impulse-Radio Ultra-WideBand (IR-UWB) receiver for low range and low data rates applications. The receiver adopts a non coherent detection with duty cycling that allows very low power consumption. The receiver operates in the high band of the UWB frequency band. It has been designed for the 7.2-8.5GHz bandwidth and covers channels 8, 9, 10, and 11 of the IEEE 802.15.4a standard. The receiver has been implemented in 130nm standard CMOS process and occupies an area of 1.5mm². Post-layout simulations of the fully differential Low Noise Amplifier (LNA) including parasitic effects of the package show 40 dB voltage gain and 4 dB noise figure. The LNA turn on time is less than 3 ns. When synchronized and duty cycled with an analog Clock and Data Recovery (CDR) with 23ns peak to peak jitter the receiver consumes 1.95mW at 1Mbps data rate.

Index Terms—UWB, impulse radio, IEEE 802.15.4a, Non-Coherent Detection, Low Power, High Voltage Gain.

I. INTRODUCTION

Many applications such as Body Area Networks, Radio-Frequency IDentification (RFID), Wireless Sensor Networks or Biomedical Networks need Ultra Low Power (ULP) transceivers for the short or medium communication ranges and for low data rates. In Impulse-Radio Ultra-WideBand (IR-UWB), due to the short time duration of IR-UWB pulses, the receiver can be turned off between two received pulses. In [1] authors show that UWB impulse radios with aggressive duty-cycling can strongly reduce the radio power consumption compared to Continuous Wave (CW) radios especially for low data rates and short communication ranges. Indeed many ULP Non Coherent UWB receivers have been published last years in the 3-5GHz low band of the UWB spectrum [1]-[5]. Recently, a self-synchronized and duty cycled UWB receiver implemented in a single chip for the 3-5 GHz UWB frequency band has been reported in [5].

In this paper we propose an ULP non coherent UWB receiver for the high band of the UWB spectrum. This paper focuses on the fully differential Low Noise Amplifier (LNA) of the receiver and its duty cycling ability. The transient response of the LNA including package parasitic effects is presented. The power consumption capabilities of the front-end receiver are analyzed in the particular case of a self synchronized and duty-cycled receiver working at 1Mbps data rate.

Section II presents the architecture of the high band self-synchronized and duty-cycled On-Off Keying (OOK) UWB receiver. In section III a fully differential LNA architecture is presented with its fast power switching implementation. Section IV presents the post layout simulation results in realistic environment including package parasitic effects. Finally, in section V, the power consumption performance of the receiver is compared to the state of the art duty cycled UWB receivers.

II. RECEIVER ARCHITECTURE

Fig. 1 shows the block diagram of the non coherent receiver architecture. This paper focuses on the front end receiver (blocks in grey in Fig.1). The 7.2-8.5 GHz fully differential LNA is duty-cycled by a power duty-cycling controller which provides the turn On/Off command (V_{ctrl}) of the LNA synchronized with the incoming UWB pulses. The symbol frequency of 1 MHz is recovered by an analog Clock and Data Recovery (CDR) based on the design presented in [6]. An asynchronous UWB pulse detector composed of a self mixing squarer, a low pass filter and a threshold detector directly follows the LNA output [7] and drives the CDR with a short duration 0- V_{DD} OOK 3ns RZ signal. It is worth noting that the proposed architecture does not need any external frequency reference.

After a searching mode cycle where a "111..." pulse sequence allows the CDR synchronization, the LNA is duty-cycled with a steady state turned-on duration T_{on} . T_{on} has to be set according to the peak to peak CDR jitter, the settling time of the LNA and the pulse duration. An overview of the ULP receiver signals and the power control signal during the steady state is presented in Fig. 2.

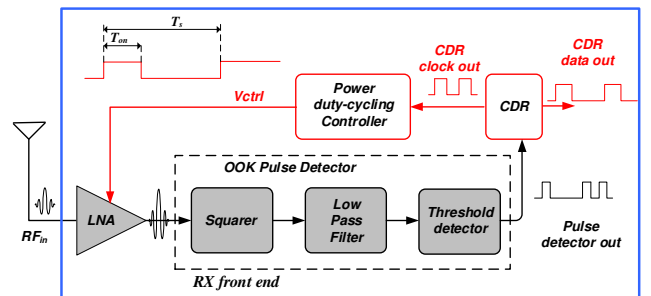


Fig. 1 Self synchronized and duty-cycled receiver architecture.

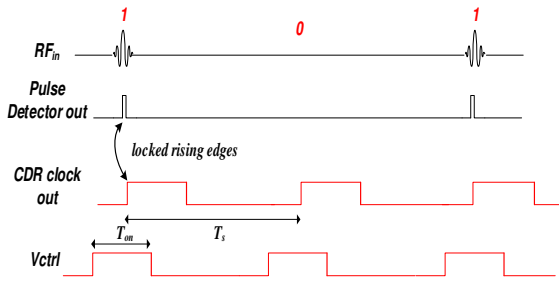


Fig. 2 Input and output receiver signals in the steady state duty-cycled mode.

III. LNA ARCHITECTURE AND POWER SWITCHING CIRCUIT IMPLEMENTATION

The fully differential LNA presented in Fig. 3 includes three stages: a LC matched input stage which achieves the wide band matching to the antenna and two gain stages which provides an additional amount of voltage gain. A fully differential topology is selected because the common mode parasitic signal generated by the turn On/Off process is rejected at the LNA differential output which allows the LNA to have a fast turn On/Off time and enables aggressive duty-cycling.

A. Differential input matching cell

The input matching cell of the LNA is deduced from a standard differential LC ladder filter. Since the fractional bandwidth of the 7.2-8.5GHz is low (less than 17%), we have used a LC ladder filter implemented by means of capacitive admittance inverters [8]. The differential ended input matching cell is given in Fig. 4.c. In Fig. 4.a and 4.c the values

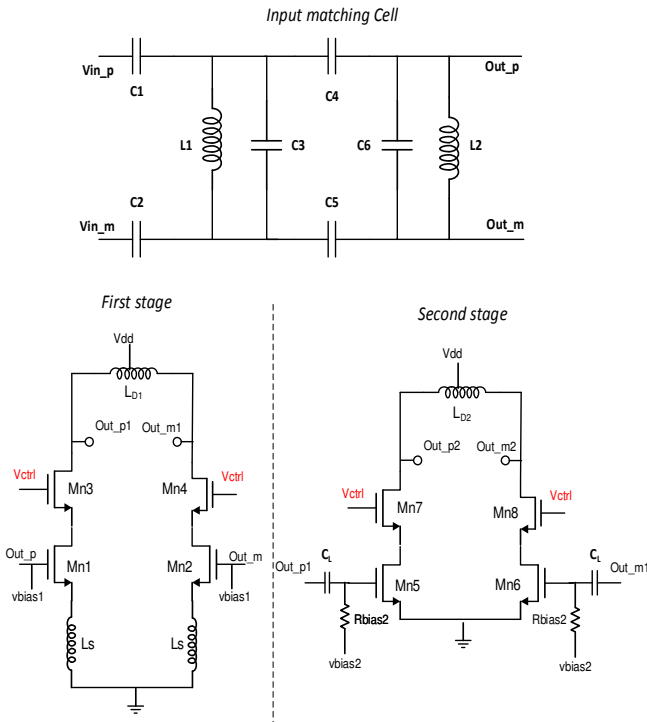


Fig. 3 LNA transistor level implementation.

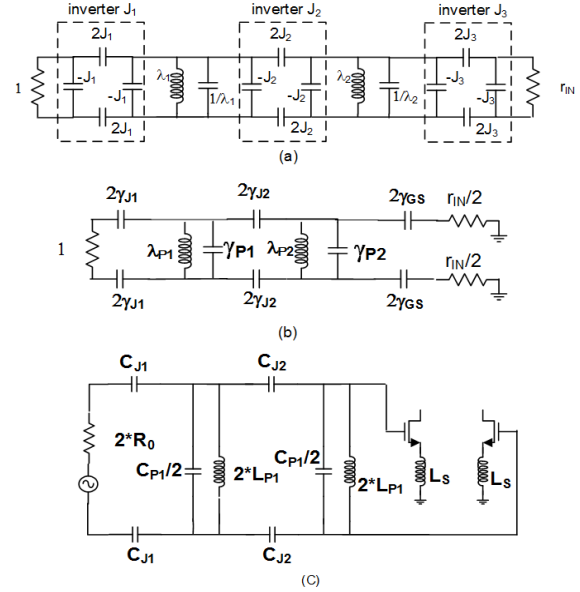


Fig. 4 Fully differential input matching cell: (a) Normalized (by $R_0=50\Omega$ and ω_0) differential LC ladder filter with capacitive admittance inverters, (b) Normalized input matching cell. (c) Input matching cell implementation.

are normalized by $R_0 = 50\Omega$ and by the middle frequency ω_0 of the LNA bandwidth. The capacitor and inductor values in Fig. 4.a are deduced from a normalized LC ladder filter. In this design we have used a second order Tchebycheff response with 0.5dB ripple. As detailed in [8] in the case of a single ended topology, the circuit of the normalized differential ended LC ladder filter using capacitive admittance inverters (Fig. 4.a) is first transformed into the circuit given in Fig. 4.b, in order to remove the negative values. Then the final circuit is given in Fig. 4.c where the resistive termination is provided by the inductive source degeneration of the input MOSFETs and the capacitors γ_{GS} are provided by the input MOSFETs capacitors.

This topology gives inductor values which can be integrated with a standard CMOS process and with high self frequency resonance (SFR) value and a high Q factor within the LNA operating bandwidth. Such LC filter input matching cell achieves the wide band matching to the antenna, a broadband response with constant group delay in the bandwidth, a noise equivalent bandwidth limitation and an out of band signal rejection.

B. LNA first stage

The first gain stage of the LNA is shown in Fig. 3. It is implemented using a differential cascode architecture with a resonant LC load and inductive source degeneration. The sizing methodology and the noise figure and the voltage gain optimization strategy, similar to the ones used for the single ended architecture presented in [8].

A fast turn On/Off capability is obtained by applying the control command (V_{ctrl}) at the gate of the cascode transistors

(Mn3) and (Mn4). By using this technique, only the biasing current of the stage is modulated during the turn-on process while the potential of the outputs (Outp1, Outm1) remains nearly unchanged.

C. LNA second stage

The second stage is implemented using a differential cascode amplifier with resonant load as shown in Fig.3. At the resonance frequency the voltage gain of the half circuit is given by (1) where g_{m5} , g_{m7} , g_{mb7} , r_{ds5} and R_p represent respectively the transconductance of Mn5, the transconductance of Mn7, the back-gate transconductance of Mn7, the drain-source resistance (Mn5) and the parasitic resistance of the inductance L_{D2} [9]. The gain expression shows that to obtain a high voltage gain, a large transistor should be used which increases considerably the power consumption of this stage. Nevertheless, the power consumption can be reduced with the implementation of the power management solution.

$$|G_v| = \frac{g_{m5}(g_{m7} + g_{mb7})r_{ds5}R_p}{1 + r_{ds5}(g_{m7} + g_{mb7})} \quad (1)$$

Similarly to the first stage the turn On/Off command (Vctrl) is applied at the gate of the cascode transistors (Mn7) and (Mn8). The second stage is AC coupled to the first stage but the voltage potential of the gates of the transistors (Mn5) and (Mn6) remains nearly unchanged during the turn On command, so the voltage at the terminals of the AC coupling capacitors is unchanged too. The inductive load allows the LNA to be DC-coupled to the pulse detector.

IV. POST LAYOUT SIMULATION RESULTS

The receiver has been implemented using a 130nm standard CMOS technology from ST-Microelectronics with a voltage supply of 1.2V. The circuit die, presented in Fig.5, occupies a silicon area of 1.5mm² including the bonding pads.

The transient response of the LNA is strongly influenced in the presence of the parasitic inductance given by the bond wires. In addition large on chip decoupling capacitor values have been used to avoid common mode coupling between the different blocks of the receiver. The package technology was carefully chosen to minimize the turn On/Off time. The receiver is implemented with multiple supply voltage and ground pins to minimize oscillations during the turn On/Off process.

Fig.6 presents the test chip used to evaluate the effect of parasitic elements given by the bond wires on the turn On/Off time. The value of the parasitic inductors on the supply voltage, the on-chip decoupling capacitors and the parasitic resistors are 3nH, 350pF and 1Ω respectively. The value of the parasitic inductor on the ground pins is 1nH. Fig.7 and Fig.8 show the results of AC (LNA loaded by detector) and S-parameters post-layout simulations. The frequency response of LNA stages is presented in Fig.7. The LNA achieves a voltage gain of 40 dB in 7.2-8.5 GHz frequency bandwidth within a minimum noise figure of 3.2dB. The return loss, S11, is low than -10 dB within all the bandwidth.

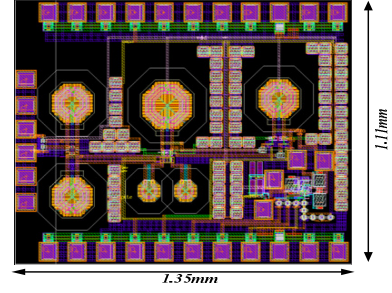


Fig. 5 Layout of the receiver in 130 nm CMOS Process.

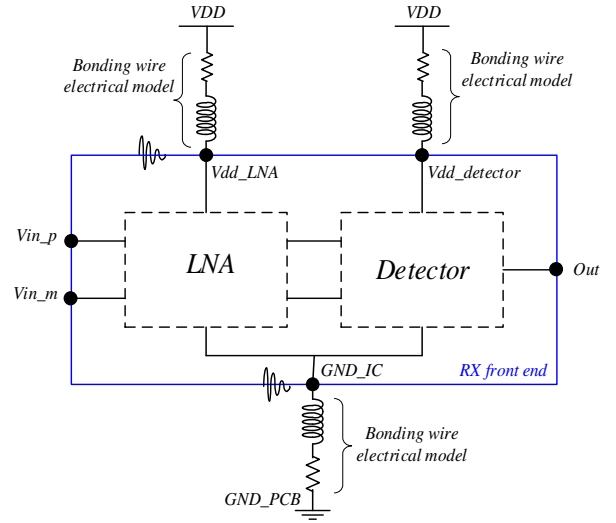


Fig. 6 Test chip used to evaluate the packaging influences on the turn On /Off time.

To evaluate the turn-On/Off time, the control command is applied while a continuous wave at the center frequency of the LNA bandwidth (7.9GHz) is applied to the LNA input. Fig.9 shows the control command signal of the LNA (Vctrl) generated at the power duty-cycling controller with the LNA differential output voltage. As shown in Fig.9. The LNA output voltage is settled within 3ns.

The whole receiver transient response has been simulated using the circuit environment described in Fig.6. The transient response of the receiver is presented in Fig.10. Fig.10 shows one period of the control command (Vctrl). A pulse signal with a peak amplitude of 400μV is applied at the LNA input. When the LNA is turned On and Off, glitches are generated at LNA outputs. The amplitude of the glitches is strongly reduced at the LNA differential output. Since the pulse detector is also sensitive to the common mode, these glitches lead to spurious detections that increase the on time duration Ton. In Fig. 10 the first response observed at the detector output is due to the turn On process of the LNA. Indeed, the UWB signal must be sent with a delay margin of 5ns to avoid false detections. A logical function has been implemented at receiver output (Out_RX) to eliminate these false detections.

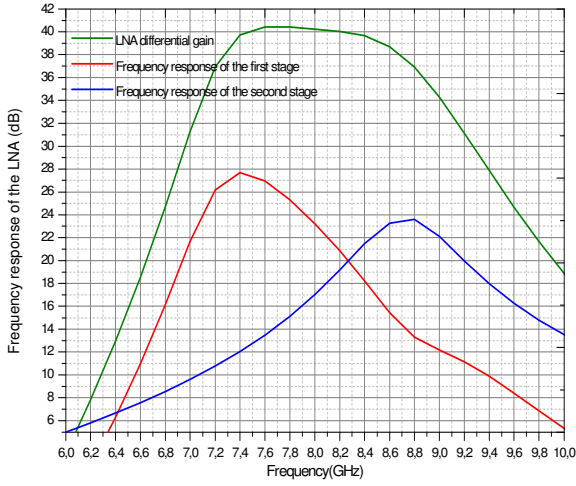


Fig. 7 LNA voltage gain with the frequency response of each stage.

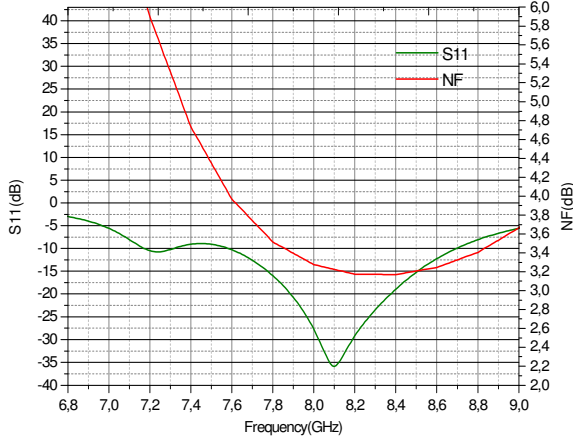


Fig. 8 The return loss S11 and the noise figure.

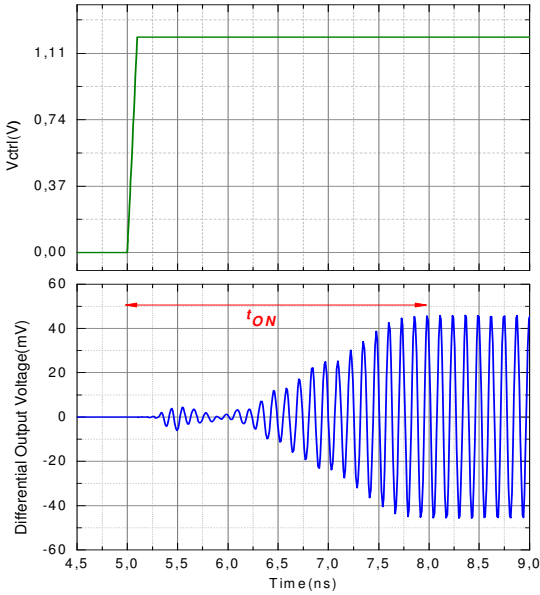


Fig. 9 Post layout simulated LNA differential output voltage.

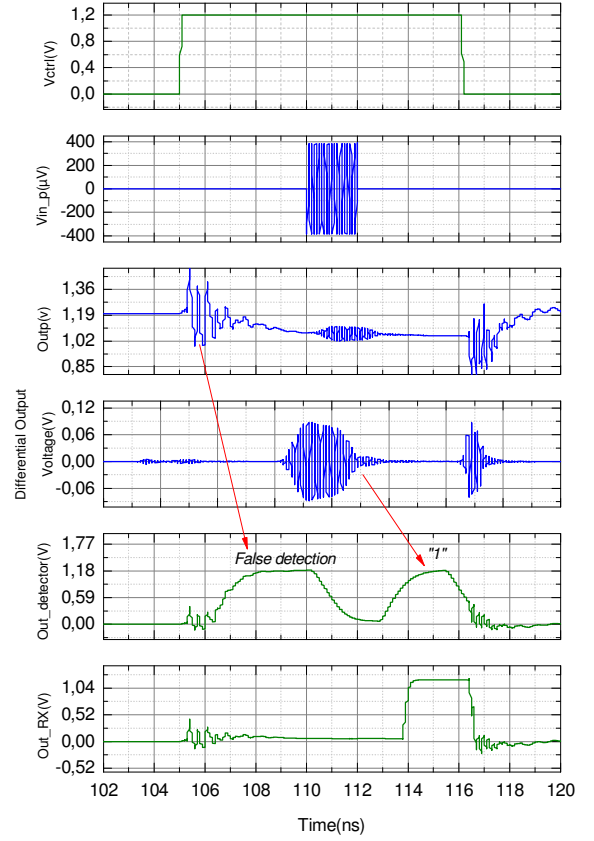


Fig. 10 Post layout simulated receiver waveforms.

V. POWER CONSUMPTION PERFORMANCE OF THE RECEIVER

The receiver power consumption P_{RX} is calculated according to equation (2). The turned-on time duration T_{ON} is given in (3) where $t_{ON-RFfunctions}$, τ and t_{synch} represent respectively the turn on time (equal to 5ns in our case), the pulse duration (~ 2 ns) and the synchronization uncertainty. The LNA is synchronized and duty-cycled with an analog CDR [6] which presents a 23ns peak to peak jitter. The static and leakage power of the LNA are respectively 49.2mW and 36 μ W. The low power detector and the CDR are always on and consume respectively 216 μ W and 16 μ W.

$$P_{RX} = \frac{T_{ON}}{T_s} \times P_{static} + P_{leakage} \quad (2)$$

$$T_{ON} = t_{ON-RFfunctions} + \tau + t_{out_detector} + t_{synch} \quad (3)$$

Table I compares the simulated performance of the proposed receiver with state of the art duty-cycled UWB receivers. The proposed receiver consumes 49.5 mW when continuously turned-on in the searching mode. Indeed, it is implemented to meet the needs of the UWB high band for IEEE 802.15.4a standard with 130 nm CMOS process. After synchronization, in the locked mode with self duty-cycling active, the RX consumes only 1.95 mW at 1 Mbps OOK data rate. Although operating in the high band, the power consumption performance of the proposed receiver in the duty

TABLE I. SUMMARY OF IR-UWB RECEIVER PERFORMANCES COMPARED TO OTHERS PUBLISHED WORKS.

<i>Parameter</i>	[2] ^b	[1] ^b	[4] ^b	[5] ^b	[this work] ^a
CMOS Technology	90nm	90nm	90nm	65nm	0.13 μ m
Frequency Bandwith(GHZ)	3-5	3-5	3.6-4.3	4.35	7.2-8.5
Gain(dB)	40	39	27	42	40
NF(dB)	8.6	N/A	6	4.5	4^c
RX Power consumption (mW)	35.8	10.5	2.9	11.66	49.5
RX Power consumption when duty-cycled	250 μ W@100kbps	14.3 μ W@100kbps	1.64mW@1Mps	750 μ W@2Mps	1.95mW@1Mps
RX Turn on time (ns)	2	3	5	15-20	5
Self-synchronized and duty-cycled	No	No	No	yes	yes
Active Area (mm ²)	2.2 (RX)	2.3 (TX+RX)	0.6(TX+RX)	0.53(TX+RX)	1.5 (RX)

a simulation results; b measured results; c average value of the noise figure

cycled mode is quite good, approaching the power consumption performance of low band receivers which are self-synchronized and duty cycled.

VI. CONCLUSION

In this paper a fully differential LNA for a self synchronized and duty-cycled receiver for the 7.2-8.5GHz bandwidth of the IEEE 802.15.4a standard is proposed. The LNA achieves a flat and high gain of about 40dB in the desired bandwidth. Post layout simulations taking into account the parasitic effects of the package show that the LNA output voltage is settled within 3ns. When synchronized and duty cycled with an analog CDR with 23ns peak to peak jitter the receiver consumes 1.95mW at 1Mbps data rate.

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