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Ultra-WideBand Voltage Controlled Oscillator with Commutable Phases for BPSK Implementation

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Abstract—An ultra-wideband Voltage Controlled Oscillator (VCO) is presented in this paper. The circuit achieves fast startups and stops which allow wideband pulses to be generated. In addition, the VCO allows bipolar modulations as Binary Phase Shift Keying to be implemented without the need of a shaping circuit as a mixer. The proposed VCO has been integrated on a silicon area of 0.003mm^2 in a 65nm CMOS technology operating with a supply voltage of 1.2V. The oscillator output provides large differential oscillations from 2.6GHz to 12.3GHz. Measurement has demonstrated the frequency agility of the proposed VCO which covers the mandatory channels of the low (resp. high) bands centered on 4492.8MHz (resp. 7987.2MHz) defined by the IEEE 802.15.4 standard. The VCO power consumption is about 3.2mW/GHz. By using Current Mode Logic (CML) gates, the power consumption can be reduced to 3.84uW only when the VCO is not running (switch off).

Keywords—BPSK; CML; Impulse Radio; Phase Switching; Power Gating; UWB; VCO

I. INTRODUCTION

Since 2002, the Federal Communications Commission (FCC) released the frequency band 3.1-10.6GHz called Ultra-Wide Band (UWB) [1], but did not specify communication mode. So, it is possible to take advantage of the UWB bandwidth by using Impulse Radio (IR) instead of conventional carrier modulations. This allows emitters with low power consumption to be designed and gives the possibility to power down most functions between the transmission of two pulses [2][3].

Following this, different standards using the UWB band have emerged as the IEEE 802.15.4 standard [4] which made the choice to cut the UWB into several channels whose bandwidth is between 500 MHz and 1.35GHz. However, two channels located around 4.5GHz and 8GHz must be covered to be compliant with this standard which implies a certain agility on behalf transmitters and receivers.

To implement modulations used by UWB-IR, three architectures of pulse generators are commonly integrated in emitters. The first uses pulse generators based on impulse filter response which has low power consumption but having quasi no tunable frequency responses [3]. The second uses pulse synthesizers which provide highly tunable frequency responses but are complex to implement [5]. Finally, the last uses switched oscillators which allows a limited number of IEEE 802.15.4 channels to be addressed by their available oscillation

frequency ranges [6][7]. Moreover, their startup and stop durations are not always short enough to make generated oscillations compliant with spectrum masks defined by the IEEE 802.15.4 standard. In this case, a mixer is required to shape the generated oscillations [8] since the width of frequency response is inversely proportional to the pulse duration. It allows an up-conversion of the baseband pulse; and the derivate UWB pulse-generator architecture is, similar to a classic modulator that permits the On-Off Keying (OOK) modulation or the Binary Phase Shift Keying (BPSK) modulation.

Furthermore, in UWB-IR communications, it is important to be able to implement bipolar modulations as BPSK or Randomly Alternate OOK (RA-OOK) [9]. Indeed, for this type of communications, the Power Spectrum Density (PSD) is composed of two parts proportional to the energy emitted per symbol which are named here continuous and discontinuous spectrum [9]. Since the discontinuous spectrum dominates the continuous spectrum for high bit rates, and since it is proportional to the mean value of emitted symbols, the use of bipolar modulations increases the maximum allowed bit rates compared to OOK modulation at the same energy emitted per symbol [9]. By contrast, it is possible to increase the energy emitted per symbol and also the communication range for a fixed bit rate.

A differential Voltage Controlled Oscillator (VCO) with a sufficient frequency range for IEEE 802.15.4 standard is presented in this paper. It achieves fast startups and stops and also does not require a mixer to shape oscillations. Moreover, the positive and the negative paths of its differential voltage output can be switched around and allows also bipolar modulations as BPSK to be implemented. Thus, it can be used for UWB-IR communications as well as conventional carried modulations. Finally, it can be powered down between the emissions of two consecutive pulses where it consumes only 3.84uW.

This paper is organized as follows. Section II deals with UWB-IR emitters based on switched oscillators. In this section, a pulse model is provided and allows the adequate pulse width to be computed as a function of the targeted spectrum mask. Section III presents the architecture of the proposed VCO designed with a 65nm design kit. In section IV, simulation results demonstrate its frequency agility while measurement results show its compliancy with the IEEE 802.15.4 standard.

II. UWB-IR EMITTERS BASED ON SWITCHED OSCILLATORS

A. Architecture of switched oscillators

As shown in Fig. 1, UWB-IR emitters based on switched oscillators use an oscillator whose duration τ_p (resp. the frequency f_M) of the gated oscillations determines the bandwidth (resp. the central frequency) of the emitted pulse in frequency domain. To allow the oscillator to be loaded by the antenna, a driver stage is necessary between the oscillator and the antenna. The design of the driver stage between the oscillator and the antenna is not discussed in this paper.

To obtain a compliant pulse with a given spectrum mask, a switched oscillator must have a frequency control, and a startup and stop command. In Fig. 1, the oscillation frequency f_M is selected by the control voltage VCTRL and the pulse duration τ_p is set by the time during which the ON signal is active.

Considering a Pulse Amplitude Modulation (PAM), the signal emitted by the antenna $s(t)$ can be written as a sequence of pulses as follows:

$$s(t) = \sum_{k=0}^{+\infty} d_k \cdot p(t - k \cdot T_s) \quad (1)$$

where d_k is the k^{th} emitted symbol, T_s is equal to the multiplicative inverse of the symbol rate, and $p(t)$ is the waveform of the generated pulse.

B. Model of pulse generated by switched oscillators

By supposing a sinusoidal switched oscillator, the pulse shape $p(t)$ can also be expressed as follows:

$$p(t) = A \cdot \sin(2\pi f_M t) \cdot \Pi_{\tau_p} \left(t - \frac{\tau_p}{2} \right) \quad (2)$$

which allows the duration τ_p to be estimated when a particular frequency mask is targeted. In (2), A is the peak voltage of generated pulse and $\Pi_{\tau}(t)$, the rectangular function equals to 1 within $[-\tau/2; \tau/2]$ interval and 0 outside. τ_p can also be written as a function of the frequency f_M by:

$$\tau_p = \frac{N}{2f_M} \quad (3)$$

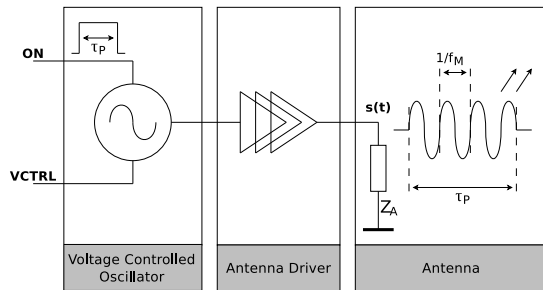


Fig. 1. Architecture of an UWB-IR emitter using a switched oscillator.

where N is the number of sinus half-periods of the generated pulse. Thus, the modulus value $|P(f)|$ of the $p(t)$ mono-lateral Fourier transform can be computed and is given by:

$$|P(f)| = \frac{A \cdot \tau_p}{\sqrt{2}} \left| \text{sinc} \left[\pi (f - f_M) \tau_p \right] \right| \quad (4)$$

For impulse modulations, by considering that the emitted power spectrum density is directly linked to the square of $|P(f)|$ [9], it is possible to compute the number N of half-periods as a function of the bandwidth BW_{-XdB} defined as follows:

$$XdB = 10 \log |P(f_M)|^2 - 10 \log \left| P \left(f_M + \frac{BW_{-XdB}}{2} \right) \right|^2 \quad (5)$$

This allows the minimum value of N to be estimated by solving:

$$XdB \leq -10 \log \left[\text{sinc}^2 \left(\frac{\pi BW_{-XdB} \tau_p}{2} \right) \right] \quad (6)$$

which gives:

$$N_{\min} = \alpha \frac{f_M}{BW_{-XdB}} \quad (7)$$

where α is a scalar equals to 1.8 (resp. 3 and 10.1) when an attenuation XdB equals to 3dB (resp. 10dB and 18dB) is considered.

From (3) and (7), the minimum value of the pulse duration τ_p , that is only BW_{-XdB} dependent, can also be computed by:

$$\tau_{p-\min} = \frac{\alpha}{2BW_{-XdB}} \quad (8)$$

and allows the energy emitted per pulse to be estimated by:

$$E_p = \frac{A^2 \tau_p}{2Z_A} \quad (9)$$

where Z_A is the antenna impedance.

III. ARCHITECTURE OF THE DESIGNED VCO

The proposed oscillator is based on a conventional ring oscillator for which one of its stage is replaced by a NAND logic gate as shown in Fig. 2. This allows the oscillation duration to be controlled by the ON signal applied to the free input introduced by the NAND gate. Thus, when ON is active, the NAND gate has the same logic equation as an inverter between the 120° input and the 0° output. This makes the system unstable and capable of oscillating. By contrast, when ON is inactive, the NAND gate imposes a logic state on its

output which is independent of the 120° signal. In this case, the system becomes stable and cannot oscillate.

Here, to avoid oscillations frequency shift when one of its outputs is loaded by an additional element as a mixer or an antenna, it is necessary to add an output buffer. Moreover, to ensure optimal oscillation conditions, each stage must have the same electrical characteristics; so it is necessary to add an identical buffer on the other outputs too.

A. Design of the three stages ring oscillator

The proposed 3-Stage VCO is shown in Fig.3. To obtain large oscillations with a frequency range wide enough to address the mandatory channels of the IEEE 802.15.4a standard, a Current Mode Logic (CML) is used for each stage of the proposed ring oscillator. In Fig. 3, VCTRL controls the oscillations frequency f_M , and the complementary ON input is used to fix the duration of oscillations τ_P . The complementary DATA input allows the positive and negative paths of the differential OUTVCO output to be commuted (OUTVCO+ becomes OUTVCO- and OUTVCO- becomes OUTVCO+). The EN input enables the standby mode (switch off) when it is reset.

B. Design of one stage used in the ring oscillator

One of the 3 identical stages of the proposed VCO in Fig.3 is shown in Fig.4. Each stage is constituted of two CML gates, a tunable delay cell (a) and an output buffer (b). These two gates are based on the same CML XOR gate which has the advantages to be strictly balanced and to be powered down when EN is inactive.

Considering the tunable delay cell (a), the input wiring has been modified compared to the classical XOR gate in order to have a similar logic function as the NAND gate shown on Fig. 2. Consequently, when S is active, the tunable delay cell works as an inverter and when S is inactive, complementary logic states are provided on its differential output. To obtain the designed ring oscillator, two stages (stages 2 and 3 according to Fig. 3) are used in inverter mode by keeping S active whereas the last stage (stage 1 according to Fig. 3) is able to be in the two modes according to the state of ON. Thus, even if each stage operates different logic equations, all the stages remain similar from an electrical point of view; consequently optimal oscillation conditions are reached.

Considering the buffer (b), the wiring has not been modified since the gate is used to implement bipolar modulations thanks to the logic equation of the XOR gate. Thus, according to the state of the complementary SB input, it is possible to logically connect OUT (resp. OUT\) to OUTB or OUTB\ (resp. OUTB\ or OUTB). It also works as an inverter or a follower and then allows bipolar modulations as BPSK to be implemented.

For the tunable delay cell (a) and the buffer (b), the VCTRL input modifies the biasing of active loads which allows the delay and also the oscillations frequency to be tuned (a), and sinusoidal waveform to be kept at the OUTVCO output of the oscillator (b).

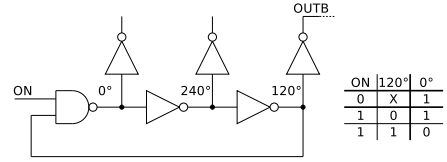


Fig. 2. Conventional three-stages ring oscillator for startup & stop control.

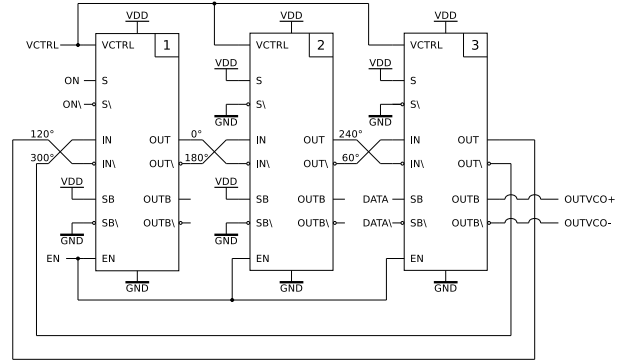


Fig. 3. Designed three-stages voltage controlled ring oscillator.

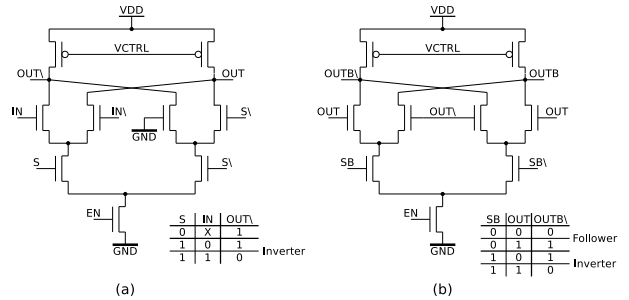


Fig. 4. Design of one CML stage: tunable delay cell (a) - XOR buffer (b).

IV. SIMULATION AND MEASUREMENT RESULTS

The proposed oscillator has been simulated and realized using the 65nm CMOS design kit from STMicroelectronics under a supply voltage of 1.2V. The VCO die area is about $35\mu\text{m}$ by $78\mu\text{m}$ and its layout is shown in Fig. 5. Here, all the connections have been made to ensure that each stage is similar to the others from an electrical point of view.

In Fig. 6, pulses, designed in frequency domain to have a bandwidth $BW_{-10\text{dB}}$ ($\alpha=3$) equals to 500MHz and centered on 4.5GHz (a) and 8GHz (b), have been generated in post-layout

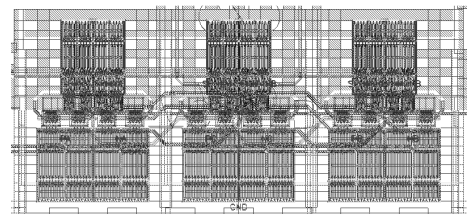


Fig. 5. Layout of the designed oscillator ($35\mu\text{m}$ by $78\mu\text{m}$).

simulations where the buffered differential output OUTVCO is loaded by the same equivalent input capacitance as the buffer (b) in Fig. 4. As predicted by (8), the ON input has been activated for 3ns. In time domain, according to Fig. 6, and the state of DATA, the differential OUTVCO voltages (obtained by subtracting OUTVCO- to OUTVCO+) are in phase opposition and consequently have the same response in frequency domain. Providing fully differential outputs as shown in Fig. 6, the circuit is able to implement bipolar modulations as BPSK modulation. Moreover, the quasi-instantaneous starts and stops give the advantage and the opportunity that any additional circuit to obtain a short duration pulse is not necessary.

From post-layout simulations, Fig. 7 shows the oscillations frequency and variation of the power consumption versus VCTRL in the same simulation conditions than Fig.6. The VCO total power consumption is about 3.2mW/GHz (resp. 3.84μW) when EN is active (resp. inactive). The VCO gain is about 14.8GHz/V. This result demonstrates the wide frequency range of operations which is compatible with the mandatory channels of the IEEE 802.15.4 standard, centered on 4492.8MHz and 7987.2MHz. This gain has been validated in measurement until 8.5GHz since the VCO has been integrated, currently, in a more complex system where VCO output signals cannot be directly observed by measurement.

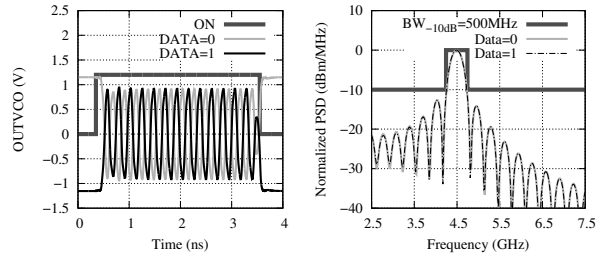
Always in the same simulation conditions than the Fig. 6, the differential OUTVCO output provides a minimum peak to peak voltage of 1.2V. Finally, the main characteristics of the proposed VCO are summarized in Table I.

V. CONCLUSION

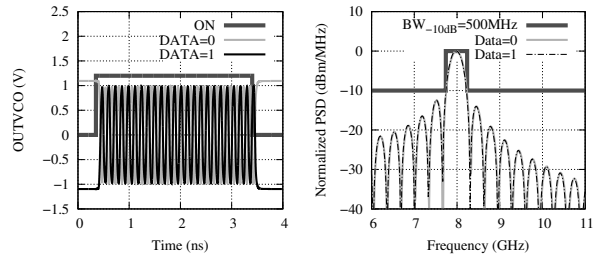
A VCO using fast CML gates has been presented in this paper. It demonstrates its capability in measurement to address the mandatory channels of the IEEE 802.15.4 standard. Moreover, it allows bipolar modulations as BPSK to be implemented without the need of a mixer or other shaping circuits. In the case of UWB-IR communications, this allows the range and/or the rate to be increased for a fixed power spectrum density compared to an OOK modulation. Finally, the circuits can advantageously be switched off between the emissions of two consecutives pulses where it consumes only 3.84μW only.

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(a)



(b)

Fig. 6. Simulated response of the differential OUTVCO voltage for a BW_{10dB} of 500MHz ($\tau_{p-min} = 3$ ns) centered on 4.5GHz (a) and 8GHz (b).

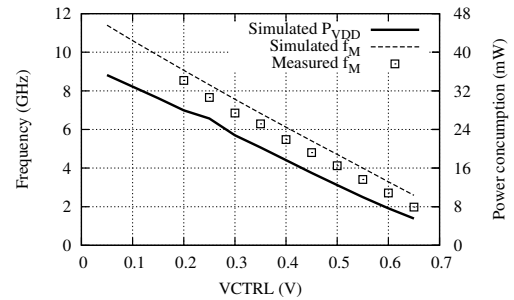


Fig. 7. Oscillation frequency and power consumption versus VCTRL.

TABLE I. SUMMARY OF VCO CHARACTERISTICS

Tech (nm)	Vdd (V)	Size (μm ²)	τ_p min	f_M (GHz)	Vpp (V)	Power Cons.	
						Running	Standby
65	1.2	2730	$1/f_M$	2.6–12.3 ^a 2.0–8.5 ^b	>1.2 ^a	3.2mW/GHz ^a	3.84μW ^a

^a Post-layout simulations of the full VCO with capacitive load (identical to buffer input capacitance).

^b Verified in measurement.

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