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A 4GHz CMOS 130nm IR-UWB dual front-end transceiver for IEEE802.15 standards

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Abstract—A single chip CMOS 130nm transceiver for UWB-IR communications was assembled and measured for further integration into a demonstrator aiming compatibility with the recently published IEEE802.15.6 standard for Body Area Networks. The transmitter achieves a 10.9 mA current consumption for the 15.6MHz pulse repetition frequency and 1.5V peak-to-peak voltage. The receiver is an innovative combination of a low current consumption non coherent envelop detector and of a high sensitivity coherent quadrature demodulator. Different compromises in sensitivity, current consumption and acquisition speed are made possible. This paper briefly describes the architecture and provides the chip measurement results.

Keywords—UWB, CMOS IC, Emitter, Receiver, Coherent, Non Coherent, BAN

I. INTRODUCTION

Over the last decade, the development of innovative architectures for the transmission and reception of UWB-IR signals benefitted from the publication of IEEE standards aiming different application areas. The IEEE802.15.4a [1] had first been published in 2007 to unify a specification based on the UWB impulse radio technology to cover the need for 1 Mbits/s class wireless systems offering sub-meter precision location at tens of meter range. Then, the emergence of devices in the smart phone eco-system for leisure and healthcare, but also in the medical area, called for the Body Area Network (BAN) and wearable devices concepts. It led to the development of the dedicated IEEE802.15.6 standard published in 2011 in which a UWB based specification is given with strong similarities with 15.4a but with simplifications aiming at reducing power consumption [2][3].

UWB-IR has significant advantages to address the large span of BAN applications in a disruptive manner compared to narrowband solutions in ISM bands. They are robustness to narrow band fades, protection against ISM bands interferers, bit rate scalability from 400 kbits/s to 12.6Mbits/s with the same hardware, reduced transmit power well below -10dBm, ultra-low power implementations especially at transmitter side at the milli-Watt scale, reduced antenna size, etc [4].

Being in 15.4a or 15.6, the specification enables the implementation of coherent and non-coherent approaches at the receiver side, thus giving opportunities for power consumption, performance and complexity tradeoffs. Purely non coherent front-ends based on threshold crossing or energy detection offer low power high-frequency-synthesis-free conversion to baseband at the expense of reduced sensitivity and lower robustness to blockers, whereas mixer-based quadrature down conversion front-ends propose the opposite compromise. Once in baseband, the conversion to the digital domain can be done at Nyquist rate over one several bits, enabling afterwards fast and parallel synchronization and channel estimation by the Digital Base Band (DBB). It may also be done at a lower rate, e.g. the Pulse Repetition Frequency (PRF), if prior processing is done in the analog domain with the aim to reduce ADCs consumption at the expense of serial search done by the DBB during synchronization.

This paper presents a smart combination of a non-coherent (NC-Rx) and a coherent receiver (C-Rx) front-end to offer several possible tradeoffs at once for the reception of 15.4a or 15.6 signals [5]. This dual-front-end receiver is assembled with a transmitter in a single CMOS chip called “RUBYLB” and operates in the 4-GHz band. Its architecture and design principles are presented in Section II. The measurement results are given in Section III and Section IV concludes the paper.

II. CHIP ARCHITECTURE AND DESIGN

A. Chip Architecture and dual-front-end concept

The RUBYLB chip architecture is shown on Fig. 1. On the receiver side, the output of the shared LNA feeds the remainder of the coherent Rx on the one side and the NC-Rx on the other side.

The C-Rx is made of a quadrature down conversion stage, an anti-aliasing and blocker rejection filter, a second quadrature down conversion stage and a bank of four integrators which will integrate the signal over 2ns windows. The position of the four windows is set by the DBB through a 125MHz Double Data Rate (DDR) parallel port at the PRF. It has as its corollary that a synchronization and channel estimation algorithm would

perform a serial-parallel search with 16 serial steps to reach 1ns resolution with half overlapping windows, thus needing at least 16 consecutive preamble symbols to complete it.

The NC-Rx is made of a rectifier followed by a detector which output feeds a LVDS converter to interface the digital baseband. Given the detector bandwidth, an equivalent 1bit 1GHz sampling is performed. Therefore the capture of a complete channel impulse response is ultimately possible within a single preamble symbol. In the case of IEEE802.15.6, preamble symbols are made of Kasami sequences of length 63 pulses. In [7] a thorough description of how the DBB would perform the preamble detection and synchronization in a few symbols can be found.

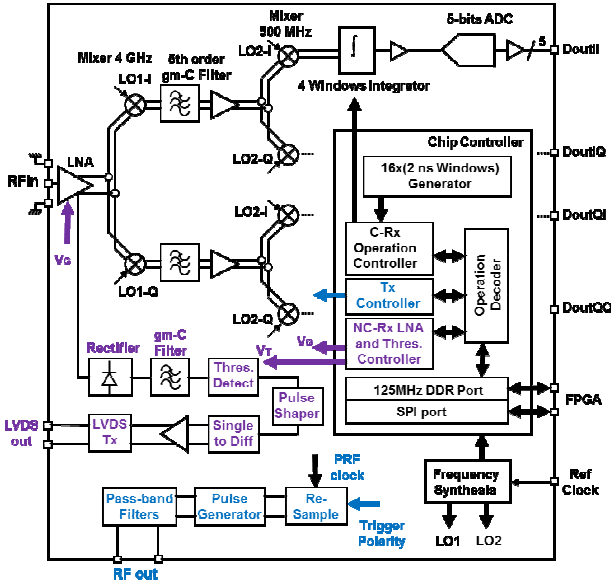


Fig. 1. RUBYLB Overall Architecture

The justification of the dual front-end receiver therefore lies in the capability of the system to perform preamble detection, synchronisation and initial channel estimation in a very short time with a low power receiver and then move to a higher sensitivity coherent receiver which will complete the channel estimation and perform symbol detection and demodulation, either in a coherent or non coherent manner.

B. Transmitter Design

The transmitter was originally designed to provide a non-tunable 2GHz bandwidth with maximal voltage swing [6] and not expected to be fully compatible with the standards spectrum masks, the objective being essentially a successful integration for further use in a demonstrator. It is based on an UWB pulse generator followed by a band-pass filter as shown on Fig. 1. The baseband pulse generator generates two τ -delayed excitations and then, when the trigger is reset (resp. set), a positive (resp. negative) pulse is generated on the clock rising edge thanks to the balanced output “RF out”.

C. Non Coherent Receiver Design

The Non-Coherent Receiver architecture is described in Fig. 1. The receiver consists of a high gain wideband LC filter

LNA [8] followed by a non coherent pulse detector and a CMOS to LVDS converter which provides received data to the digital base band (DBB). The non-coherent pulse detection is performed by rectifying the RF signal and low pass filtering instead of squaring the RF signal. The threshold detection is achieved with biased CMOS inverters [9]. A 1ns 0- V_{DD} square signal is obtained at the detector output for each incoming UWB pulse. A CMOS to LVDS converter is used to drive this wideband digital signal to the Digital Base Band input. The pulse detection principle is depicted in Fig. 2. The rectifier is composed of a cascade of an odd number of CMOS biased inverters. Consecutive inverters are biased alternatively at V_P and V_N values (see Fig. 2.b) in order to achieve a strong non linear response which amplifies the positive half cycle of the incoming signal and saturates the negative half cycle (see Fig. 2.c). V_P and V_N bias values are set by the DBB and strongly impact the receiver sensitivity. As we can see in Fig. 2.c this detector architecture provides an additional gain.

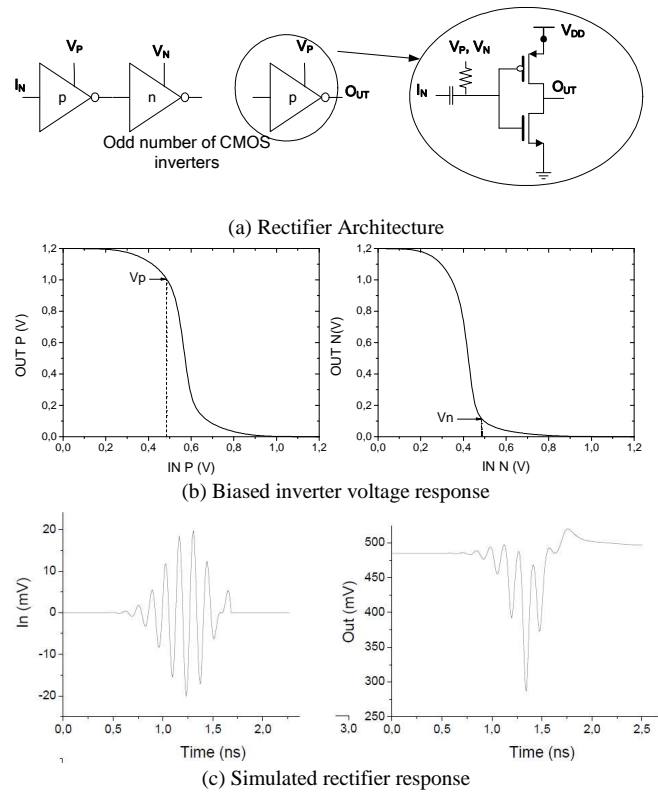


Fig. 2. Rectifier architecture and pulse detection principle

D. Coherent Receiver Design

The coherent receiver original principle is exposed in [10] and its architecture, design details and key performances are detailed in [11]. In the implementation presented in this paper, the main modifications concern the LNA, the operating frequencies to comply with the IEEE802.15.4a/6 band plans and PRFs, and the interface with an external DBB.

E. Chip Layout

The RUBYLB chip was designed in CMOS130nm from STmicroelectronics. Its overall size is 20mm² with an active

part size of 12mm². Its layout is shown on Fig. 3. It was assembled in a QFN88 package.

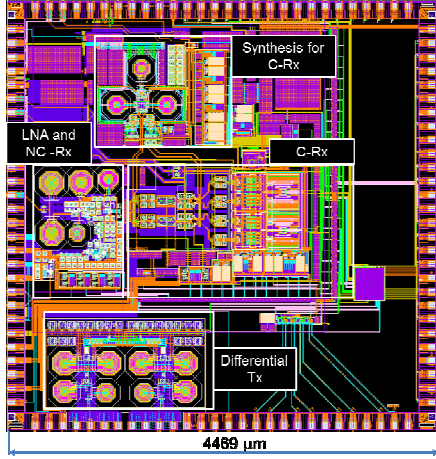


Fig. 3. Chip Layout

III. MEASUREMENT RESULTS

A. Transmitter Measurements

The transmitted pulse was acquired with an Agilent Series 90000 40Gps Digital Sampling Oscilloscope (DSO) and then post-processed with MatlabTM to calculate its time and frequency domains characteristics (Fig. 4). The transmitter produces 1.52V peak to peak pulses with 4 GHz center frequency and 2.1GHz 10dB bandwidth.

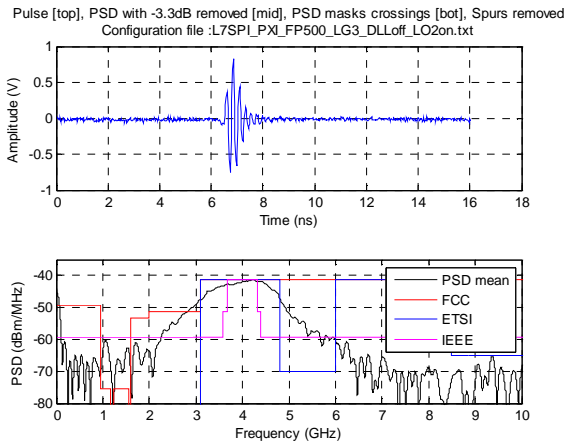


Fig. 4. Tx Pulse Shape in Time and Frequency Domains with spectrum masks for FCC, ECC (ETSI) and IEEE802.15.4a/6

It is noted that the receiver performances presented in next sections were measured using an Anritsu MP1800A generator configured to produce a pulse shape with 15.6MHz PRF very close to the actual transmitter one. To further calculate the sensitivity, a Gaussian pulse with 10dB bandwidth of 2000MHz adequately approximates the transmitted pulse.

B. Non Coherent Rx Measurements

The sensitivity of the NC-Rx was measured using an oscilloscope triggered on the pulses emissions. An extraction of the statistics at the expected LVDS output pulse position provides a measurement of the detection and miss-detection rates, whereas the integral of LVDS high level crossings at all other positions provides the false alarm rate.

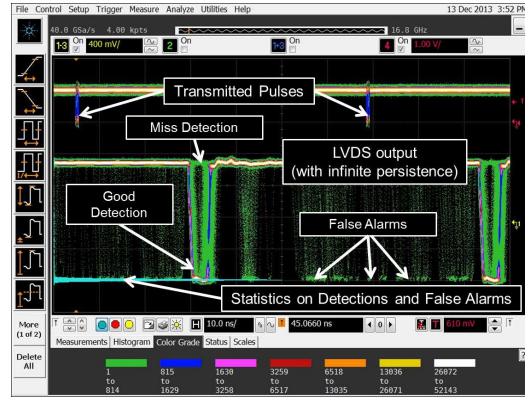


Fig. 5. LVDS Output for the Non Coherent Rx

The settings of the NC-Rx (V_G , V_T then V_P and V_N) are adjusted so as to set the probability of false alarm near to 0% and the probability of good detection near to 100% with 0.1% tolerance. The voltage supply of the LNA was raised to 1.35V to achieve the expected gain and noise figure performances obtained in simulation. Once the other blocks of the receiver are activated, and especially the frequency synthesis, the level of internal noise due to clock couplings is a little degraded. The settings have been revisited accordingly but an acceptable penalty of 2dB on the receiver pulse detection sensitivity remains. The best settings together with the best obtained sensitivity are reported in TABLE I.

TABLE I. NC-RX PULSE DETECTION SENSITIVITY

	Nominal Settings @ 1.2V	Best settings @ 1.35V	Best settings with all blocks active @ 1.35V
V_T (mV)	724.7	757	743
V_N (mV)	635.3	640	649
V_P (mV)	343.5	339	334
V_G (mV)	400	400	649
Sensitivity (dBm)	-66	-72	-70

C. Coherent Rx Measurements

In the C-Rx, the frequency synthesis is composed of an 8GHz VCO which through a PLL and a quadrature divider-by-2 delivers the 4GHz LO to the first stage mixer and a 500MHz reference clock for the analog baseband, ADCs, external DBB and transmitter.

TABLE II. FREQUENCY SYNTHESIS PHASE NOISE AT 8GHZ

Phase Noise (dBc/Hz)	@ 10kHz	@ 100kHz	@ 1MHz	@ 10MHz
Expected	-74	-67	-87	-115
Measured	-70	-67	-85	-104

The phase noise specification complies with the coherent reception at the lowest symbol rates in the IEEE802.15.6 standard. The supply voltage was raised to 1.3V to optimize the phase noise performance reported in TABLE II. .

Next, the transfer function of the C-Rx was measured to characterize the receiver gain and bandwidth. The maximum in-band gain is tunable from 54dB to 66dB with around 4dB steps. Measurement of the gain in pulse mode gives 61dB with a ~600MHz 10dB bandwidth pulse compliant with IEEE802.15.6 and 57dB with a 2000MHz 10dB bandwidth pulse close to the transmitter one.

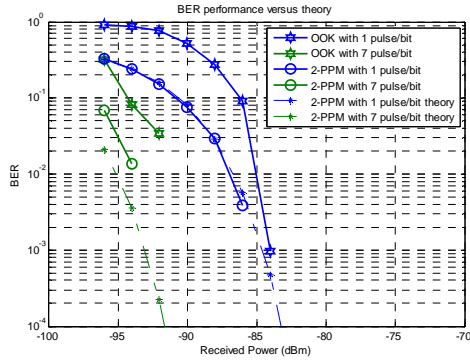


Fig. 6. C-Rx BER curves for IEEE802.15.6 2-PPM and OOK modulations under perfect synchronisation

Finally, the sensitivity was measured in pulse mode supposing perfect synchronization for the receiver and a BER target of 10^{-3} for the 2-ary pulse position modulation (2-PPM) as used in IEEE802.15.4a/6 at the highest uncoded bit rate of 15.6Mbits/s. Fig. 6 shows the BER curves for a transmitter compliant with channel 2 of the standard. The processing gain obtained with a coherent integration over 7 pulses is about 8dB, close to the theoretical value of 8.5dB. The sensitivity measurements for the C-Rx are summarized in TABLE III.

TABLE III. C-RX BIT DEMODULATION SENSITIVITY

Bit rate	RUBYLB Tx bandwidth	1100 MHz bandwidth	IEEE802.15.6 channels bandwidth
15.6 Mbits/s	-82 dBm	-84 dBm	-84 dBm
2.23 Mbits/s	-89 dBm	-91 dBm	-92 dBm

D. Current Consumption

TABLE IV. provides the current consumption measured on the different supplies available on the test board. Expectations are met for the different blocks, except for the transmitter for which the trigger signal did not have the expected duty cycling (50% instead of a few %). The NC-Rx total consumption is about half the C-Rx one, which also justifies the choice for the dual front-end combination, providing fast bloc-level power up and power down is possible during frame reception.

IV. CONCLUSIONS AND FUTURE WORK

A fully functional dual front-end CMOS130nm transceiver aiming partial compliance with IEEE802.15.4a/6 standards was assembled and measured. The pulse detection sensitivity for

the non-coherent receiver is -72dBm for a 33mA current consumption whereas the bit demodulation sensitivity of the coherent front-end is -84dBm at 15.6Mbits/s with 61.9mA drawn from the supply. Future works aim at interfacing the chip with the DBB in an FPGA and work on the acquisition speed, sensitivity, consumption tradeoffs.

TABLE IV. RUBYLB CURRENT CONSUMPTION

Regulator	Expected consumption (@1.2V)(mA)	Measured consumption (@1.2V) (mA)
LNA and NC Det.	28.1 (20.1 for LNA)	28.0 (@ 1.35V)
Mixer, Integrators	17.1	14.4
Digital, DIOs, Ring	6.7 (DIOs off)	8.5 (DIOs off)
LVDS	6.0	5.0
Frequ. Synthesis	16.2	17.9 (@ 1.3V)
VCO	0.9	1.1
TOTAL for full RX	75.0	74.9
Total for NC-RX	34.1	33.0
Total for C-RX	61.0	61.9
TOTAL for TX (without PRF clock)	3.0 (@15.6MHz)	0.06 (no trig) 10.9 (continuous trig)

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