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A Remotely UHF Powered UWB Transmitter for High Precision Localization of RFID Tag

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Abstract—The design of a remotely UHF powered UWB transmitter is presented in 0.13 μm CMOS standard process. Power harvesting unit is based on a Dickson voltage multiplier and UWB pulse generator uses filtered combined edge method. Multi-Vt technique and CMOS logic allows pulse generator power consumption between two consecutive pulses to be reduced enough to be remotely powered. It achieves FCC compliant pulses having 1.82Vpp and a PRF of 15kHz at 10m thanks to the power harvesting unit.

Power Harvesting; Pulse Generator; Remotely Powered; RFID; Tag Localization; UWB;

I. INTRODUCTION

Due to its rapid adoption in industry, RFID technology is facing new application demands. Especially, accurate Real Time Location (RTL), robust, and secure identification and management of large Tag number are needed to address new purposes, and new markets. Such a demand is all the more difficult to satisfy since the Tag cost must be lower than few tens of cents. Consequently the tag must be fabricated using, low cost technologies: a single CMOS chip in a low cost technology with no external devices such as crystals or filter and moreover the chip must be remotely powered to avoid the use of costly cells or battery.

Since UHF RFID technology uses narrowband continuous waves around 900MHz, it is intrinsically limited for high resolution location, sensitive to multipath cancellation and affected by multi-users interference. Even if improvements can still be achieved on UHF RFID systems, a technological breakthrough is needed to overcome all those limitations. According to recent works, UWB-IR is a promising technique for the next generation of RFID systems [1]. The very short time duration of the emitted pulse enables (i) accurate localization with TOA or TDOA techniques [1], (ii) efficient power gating which allows power consumption to be reduced, (iii) high multipath resolution which allows coverage area to be increased, (iv) efficient multiple access and interference mitigation which allow the number of Tags to be increased [2][3][4][5][6].

Several communication techniques can be implemented to achieve the uplink in a Remotely Powered UWB Tag. A first solution is to use UWB backscatter propagation [7]. Backscattering is very well suited to passive Tag because it consumes a very small amount of power since it consists in

varying the input impedance of the circuit. Unfortunately, the backscatter signal has very low energy which degrades the localization accuracy [4]. Another solution is to use an ultra low power UWB pulse generator remotely powered by an UHF downlink [8]. Indeed UWB pulse generators are known to consume a very small amount of energy for a pulse emission. In [9] we demonstrated an energy consumption of 9pJ per pulse with 10dBm pulse peak power. Such low energy per pulse consumption enables ultra low power consumption at low data rate (few tens of microwatt for 1Mbs⁻¹ bit rate) which can be supplied by a standard UHF energy harvesting unit.

Recent works showed the feasibility of UHF/UWB hybrid RFID Tags [8][10]. It appears that achieving high energy pulse with a very small power budget is a bottleneck which finally limits the localization accuracy and the range. To improve the energy efficiency of the pulse generator, high energy pulse must be used [1]. But in the same time, energy consumed per pulse must be minimized. Especially, reducing the power consumed between the emissions of two consecutive pulses is highly required to reach ultra low power consumption at medium or low rate. Moreover, efficiency of the energy harvesting unit must also be maximized to increase the available power and so, the localization accuracy and the tag reader range.

In this paper, we present a remotely powered UHF/UWB transmitter for a passive RFID Tag for high precision localization. As shown in Fig. 1, the Tag consists of an UWB ultra low power pulse generator powered by an UHF energy harvesting unit. The tag, which can be power supplied by conventional UHF RFID readers, is designed to be used with high sensitivity UWB coherent receivers such as described in [11] which are beyond the scope of this paper. The presented pulse generator is based on the topology presented in [9] which enables the generation of high energy pulses. In this work, we present a new design optimized to minimize the power consumed between the emissions of two consecutive pulses in order to be supplied by an UHF energy harvesting unit. This UHF energy harvesting unit is based on the topology presented in [12] which has been optimized to improve the power efficiency in the technology used. We show that the tag can generate 1.83Vpp pulses at a continuous Pulse Repetition Frequency (PRF) of 15kHz at 10 meters.

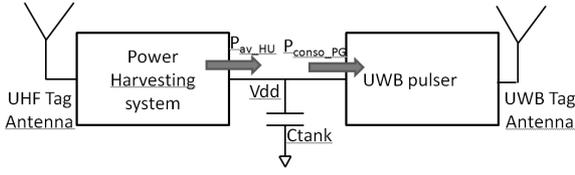


Figure 1. Tag system

Section II presents the principle of the proposed Tag and gives an analysis of the power budget according to EPC Gen2 standard regulation. Then, the design of the pulse generator and of the UHF energy harvesting unit is detailed in section III. Based on measurements of the power harvesting unit, the simulated performances of the transmitter using a 0.13 μ m CMOS design kit are then presented in section IV to validate our approach.

II. PRINCIPLE AND POWER BUDGET

Pulse generator power consumption and harvesting unit efficiency are the design key parameters. These parameters set the system performances in terms of bit rate and range.

Due to gated nature of the emitted signal, instantaneous current absorbed by the pulse generator can be very high during the pulse emission. Fig. 2 shows typical current consumption of a pulse generator [9].

The mean power consumption is a function of the mean bit rate (D_{b-mean}) and can be written as follows:

$$P_{cons_PG} = E_{ap} \cdot D_{b-mean} + P_{0Hz} \quad (1)$$

where P_{0Hz} is the constant DC power consumed at a PRF of 0Hz and E_{ap} is the active energy added while pulse is generated.

To properly power supply the pulse generator, the harvesting unit must provide an available power (P_{av-HU}) at least equal to P_{cons_PG} . P_{av-HU} depends on efficiency η of the harvesting unit and on regulated UHF downlink EIRP as follows:

$$P_{cons_PG} = P_{av_HU} = \left(\frac{\lambda}{4\pi d} \right)^2 \eta \cdot EIRP \quad (2)$$

where λ is the wavelength of UHF downlink.

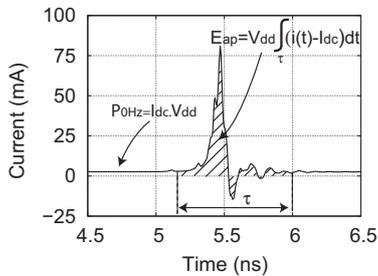


Figure 2. Pulsar consumption

This power budget gives the range d as a function of the mean bit rate:

$$d = \frac{\lambda}{4\pi} \sqrt{\frac{\eta EIRP}{(E_{ap} \cdot D_{b-mean} + P_{0Hz})}} \quad (3)$$

The maximum theoretical range is reached when D_{b-mean} is null, i.e. all the harvested energy is consumed by the P_{0Hz} . To be able to generate one or several UWB pulses, an energy tank must be included in the system. This energy tank is the capacitor C_{TANK} (see Fig. 1) which must be sized to supply energy consumed when UWB pulses are emitted, while a sufficient supply voltage V_{DD} is maintained.

For a given technology, with a minimum and a maximum voltage supply, respectively V_{DD-min} and V_{DD-max} , and assuming that the capacitor voltage is V_{DD-max} at the beginning of UWB pulses burst, the minimum tank capacitor value is given by:

$$C_{TANK} = \frac{2N \left[E_{ap} + T_s (P_{0Hz} - P_{av_HU}) \right]}{V_{DD-max}^2 - V_{DD-min}^2} \quad (4)$$

where N is the number of UWB pulses emitted into one burst and T_s , the symbol time into the burst period. It should be highlighted that if the system need transmission of an only one UWB pulse into one burst, the value of T_s is not defined and should be replaced by the pulse duration τ in (4).

It appears clearly that using an important number of pulses into one UWB burst leads to a large capacitor value which can lead to a large silicon area if the system is fully integrated. If the bit sequence is not very large (e.g. 96 bits for an EPC code), and if the technology is able to work with a large gap V_{DD-min} and V_{DD-max} , it may be possible to transmit such short bursts with a system using an integrated tank capacitor.

As a summary for this section we can note that: (i) the mean bit rate D_{b-mean} is set by harvesting power, energy consumption per pulse E_{ap} , and pulse generator DC power P_{0Hz} , (ii) the length N of bit sequence emitted during one burst depends only on tank capacitor value C_{TANK} .

III. SYSTEM DESIGN

A. Harvesting power unit design

The power harvesting unit is based on a Dickson voltage multiplier architecture implemented with MOS diodes in a CMOS technology as shown on Fig. 3. In [12] we give an analysis of this multiplier architecture and we show that the power efficiency depends, for a targeted output power, on the transistors sizing (width and length), and on the number of the multiplier stages.

In typical UHF RFID tags, no matching circuit between the antenna and the voltage multiplier are used and so, antenna must match input impedance of the harvesting unit. In addition it should be pointed that all impedance values are not achievable for a tag antenna and so, voltage multiplier must be designed with this constraint. As a consequence some designs have to be ignored thanks to impossible antenna matching [13].

The voltage multiplier design has been optimized for the 0.13 μm CMOS technology used in this work. To reach the best power harvesting efficiency, design key parameters are: (i) a MOSFET length and width of respectively 0.13 μm and 15 μm , (ii) a value of 1.2pF for multiplier capacitors C_m and (iii) a three stages multiplier.

A test chip has been realized including a standalone voltage multiplier with an ESD protection circuit at its input. The measured power efficiency of the harvesting unit as a function of its input power is shown in Fig. 4. The efficiency measurements are performed on chip at 900MHz, by using a Vector Network Analyzer (VNA) in a sweep power mode. As a consequence, the VNA provides the input power to the harvesting unit input while measuring its impedance. The power absorbed by the harvesting unit (P_{IN_ABS}) is then calculated from the VNA RF output power and the measured input impedance. The harvesting unit output is connected to a resistive load and an oscilloscope in order to measure the output voltage and the output power P_{AV_HU} . With an EIRP of 4W according to US regulation and a tag antenna of 0dBi the available input power is -15.5dBm at 10m range leading to an available power at the harvesting unit output P_{AV_HU} of 3.5 μW .

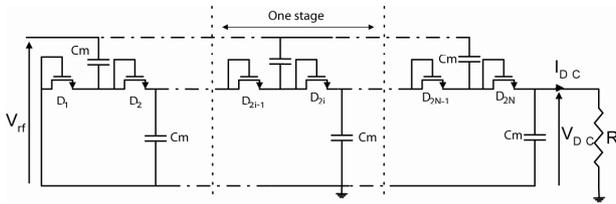


Figure 3. Power harvesting architecture

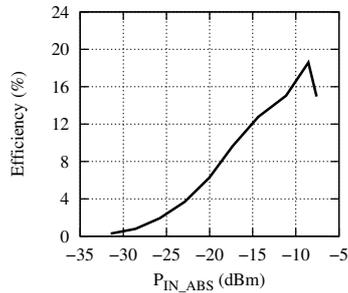


Figure 4. Measured efficiency vs input power

B. Pulser design

Among the different UWB pulse generation techniques, many works show that filtered combined edge method is well-suited when an high energy efficiency is required as in remote powered UHF applications [9][14][15]. The presented generator is a derivative of a previous designed pulse generator which consumes a static current of 2.6mA due to integrated digital edge combiner based on Current Mode Logic (CML) gates [9]. To reduce the static power consumption, the choice of a standard CMOS logic associated to a power manager is assumed.

In wireless emitters design, leakage currents of CMOS logic are often negligible compared to bias currents, however it becomes sizeable when no bias current are required. Furthermore, leakage currents which are channel width dependent increase owing to Drain-Induced Barrier Lowering (DIBL) effect when channel length and Threshold Voltage (V_t) decrease. For example, with ST 0.13 μm design kit, the use of low- V_t transistors for the pulse generator based on CMOS digital edge combiner leads to an unwanted leakage current greater than 50uA. To minimize this static leakage power consumption, multi- V_t and Multi-Threshold CMOS (MTCMOS) techniques can be used [16]. The first consists in using the most appropriate threshold type for transistors according to their function whereas the second implies the design of hybrid logic gates.

As shown in Fig. 5, UWB pulse generator can be divided in four parts: the band-pass filter, the high- V_t current driver, the low- V_t digital edge combiner and the high- V_t power manager.

Band-pass Filter uses Bessel-Thompson coefficients which allow UWB pulse duration to be minimized. Its input and output are matched to 50 Ω impedance in order to maximize power transfer to 50 Ω antenna. High- V_t Current Driver linked to Band-pass Filter is a class-C amplifier where current driver drain is biased by L. C1 capacitor prevents V_{DD} biasing of others filter nodes. Finally, a baseband pulses must be applied on High- V_t Current Driver gate to emit UWB pulses. A sizing method of the driver regarding the application needs and the filter characteristics is given in [9].

Low- V_t Digital Edge Combiner generates baseband pulses needed by High- V_t Current driver for UWB pulses generation. It is only designed with low- V_t MOS devices and supplied by Power Managed Supply thanks to V-VDD and V-GND supply buses. High- V_t Power Manager consists in D flip-flops, a delay cell, logic buffers, and a balun and uses only high- V_t MOS devices. It allows complementary power management signals which drive Power Managed Supply (PM and PM) to be generated.

To generate an UWB pulse, a rising edge has to be applied on High- V_t Power Manager input (CK) which allows power management to be disable ($PM='0'$ and $PM='1'$). Then, a 500ps delayed rising edge is generated on CKd in order to ensure that all V-VDD and V-GND supplies of Low- V_t Digital Edge Combiner are enable when it is propagating into itself. Delay cell consists in three strings of balanced and unbalanced inverters which mainly delays rising edges for a duration of 500ps.

In Low- V_t Digital Edge Combiner, rising edge from CKd is propagating in a string of buffered inverters loaded by a capacitor. Next, the buffered rising edge A2 is combined with the buffered falling edge B2 to make an inverted baseband pulse thanks to fast NAND logic gate. Capacitors in buffered inverters string are sized with the help of post-layout simulations to have a 75ps width buffered baseband pulse on driver current gate. This baseband pulse width is sized regarding the designed band-pass filter [9].

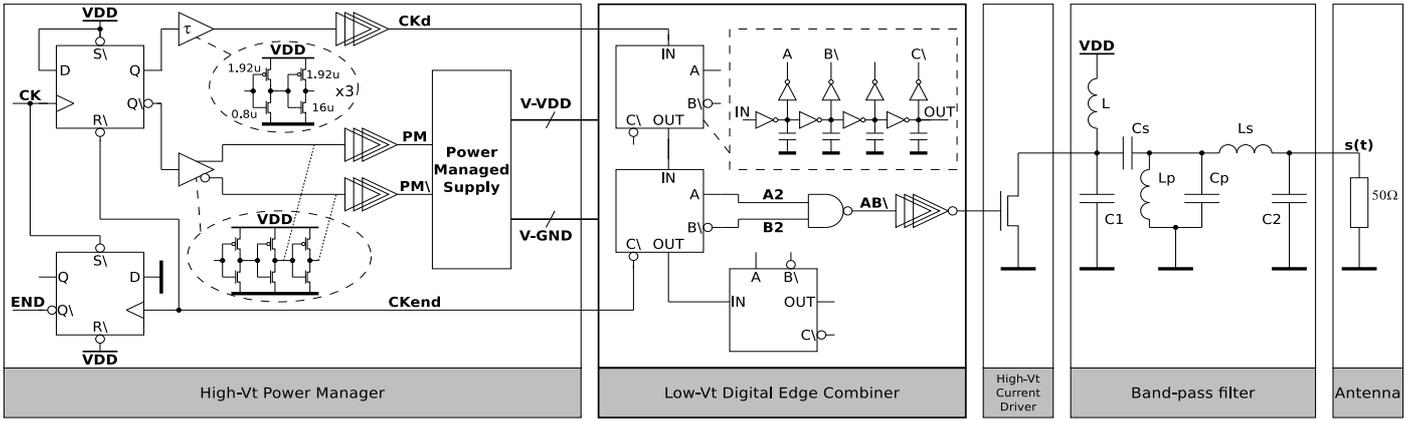


Figure 5. Pulse generator design

After the baseband pulse and so UWB pulse are issued, a falling edge is generated on CKd and Low-Vt Digital Edge Combiner is put in its sleeping state. When the falling edge arrives on CKend, END is set to '1' and power manager is enable (PM='1' and PM='0'). Finally, END is set to '0' when CK is reset.

The pulse generator presented in this work has been post-layout simulated in a 0.13 μ m CMOS from STMicroelectronics. Voltage supply is 1.2V and die area is 0.64mm². It achieves FCC compliant pulses with 1.83Vpp on 50 Ω resistive load as shown on Fig. 6. Central frequency and 10dB bandwidth are respectively equal to 7.25GHz and 6.25GHz.

As shown on Fig. 7, power consumption for a pulse frequency of 0Hz is 2.07 μ W and dynamic energy consumption is 68.6pJ/pulse which leads to a power consumption of 70.6 μ W at 1Mpulse/s. Duration of an UWB pulse generation cycle is greater than 4ns between CK rising edge and END rising edge. It imposes also a maximum power consumption of 13.7mW at the maximum PRF of 200Mpulse/s.

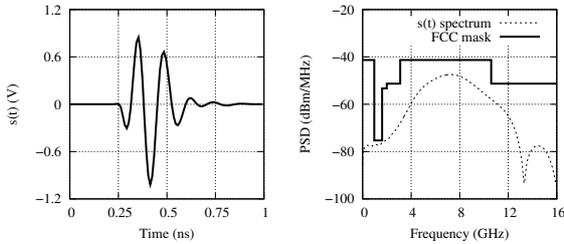


Figure 6. Pulse obtained with the proposed pulse generator on 50 Ω in time domain and frequency domain,

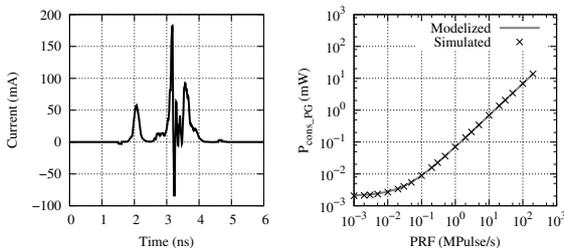


Figure 7. Consumed current during pulse generation and total power consumption versus PRF.

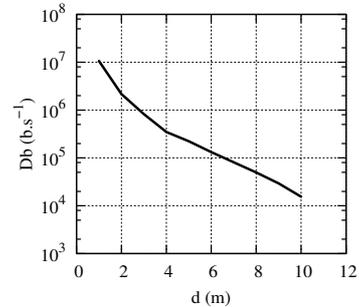


Figure 8. Mean bit rate as a function of the communication range.

IV. RESULTS AND VALIDATION

To validate the proposed system, the mean bit rate is evaluated as a function of the communication range. The bit rate is derived from (3) and is given by:

$$D_{b-mean} = \frac{1}{E_{ap}} \left[\left(\frac{\lambda}{4\pi d} \right)^2 \eta \cdot EIRP - P_{0Hz} \right]. \quad (5)$$

The bit rate is plotted in Fig. 8 using the characteristics (η , E_{ap} , P_{0Hz}) of our system. The theoretical maximum range is 11.83m and a mean bit rate of 15kb.s⁻¹ is obtained at 10m which corresponds to a received power of -15.5dBm.

The needed value of the capacitor C_{TANK} , regarding the number of pulses in a burst is calculated from (4). Assuming a maximum V_{DD} variation of ($V_{DD-max} - V_{DD-min} = \Delta V = 0.9V$), the minimum capacitor value is 56pF for $N=1$. A burst of $N=100$ pulses can be generated with a 5,6nF capacitor. The instantaneous bit rate during the burst can be increased up to 200Mb/s. Using high instantaneous bit rates allow the channel time occupancy to be significantly reduced. Indeed the 96 bits of an EPC gen2 frame could be transmitted in less than 500ns instead of 167 μ s in the best case of UHF gen2 uplinks. However on chip integration of high value capacitors increases significantly the silicon area.

TABLE I. CAPACITOR NEEDED FOR $\Delta V_{\max}=0.9V$

Number of bit by burst (N)	1	50	100
C_{TANK}	56 pF	2,8nF	5,6 nF

TABLE II. PERFORMANCE COMPARISON OF RECENT WORKS

	This Work**	[10]	[8]
UWB tx			
V_{pp}	1.83V	220mV	220mV
P_{cons}	7.09mW (@100Mbs ⁻¹)	6.5mW (@112Mbs ⁻¹)	918uW (@100Mbs ⁻¹)
E_c	70.9pJ	58.8pJ	9.2pJ
E_p^*	3.77pJ	0.24pJ	0.08pJ
$\eta=E_p/E_c$	5,3%	0.4%	0.86%
Pulse width (τ)	450ps	2ns	620ps
Harvesting			
V_{dd}	1.2 V	-	2.75V
C	56pF	-	211nF
System			
$D_{b,max}$ (burst mode)	200Mbs ⁻¹	-	100Mbs ⁻¹
D_b (mean)	15,4kbs ⁻¹	112Mbs ⁻¹	570kbs ⁻¹
Range	10m	10cm	13,9m
Sensitivity	-15.5dBm	14dBm	-18.5dBm

*Approximation: $V_{pp}^2/(8 \cdot \tau \cdot Z_0)$; **Mixed measurement and simulation results

The main characteristics of the proposed system are summarized in TABLE II. It especially shows the good energy efficiency of pulse generator which allows high energy pulses required for high accuracy localization to be generated.

V. CONCLUSION

A transceiver for hybrid UHF/UWB Tag has been presented for localization applications. This transceiver is based on an UHF energy harvesting unit which can supply a pulse generator, operating at a mean bit rate of 15kb.s⁻¹ at 10m. The pulse generator achieves high energy pulses which increase the localization accuracy in the case of TOA estimation. The transceiver can be fully integrated since the C tank of energy harvester is equal to 56pF and the overall area is estimated to be 0.8mm².

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