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R. Vauche, Sylvain Bourdel, N. Dehaese, O. Fourquin, Jean Gaubert. Fully tunable UWB pulse generator with zero DC power consumption. 2009 IEEE International Conference on Ultra-Wideband, Sep 2009, Vancouver, France. 10.1109/ICUWB.2009.5288788 . hal-01704302

HAL Id: hal-01704302

<https://hal.science/hal-01704302v1>

Submitted on 20 Dec 2021

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Fully Tunable UWB Pulse Generator with Zero DC Power Consumption

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Abstract—The design of a fully tunable pulse generator using only logic cells is presented and simulated with 0.13 μ m standard CMOS process. The generator is based on the elementary pulse combination and can synthesize different UWB pulse shapes. The generator uses logic gates to achieve the elementary pulses and a H-bridge to make the combination which leads to a zero DC power consumption. To achieve FCC compliant pulse having 2V_{pp} magnitude the generator consumes 140 pJ by pulse using 1.2V supply voltage.

UWB; Tunable Pulse Generator; H-Bridge; Pulse Shape;

I. INTRODUCTION

As a result of mounting need for wireless communications in North America, Federal Communication Commission (FCC) has regulated 3.1-10.6GHz band in 2002 for Ultra-WideBand (UWB) transmission [1]. Other local regulation organizations in telecommunications allocated later frequency bands, in particular 6-8.5GHz in Europe, and 3.4-4.8GHz, 7.25-10.25GHz in Japan. Width of these bands allows the use of Impulse Radio (IR-UWB) techniques which require very simple transceiver architecture [2]. Opposed to classical wireless systems, UWB systems do not involve integration of costly functions in terms of consumption and die area as frequency synthesizer and mixer.

In order to be suitable for IR-UWB low cost applications, the pulse generator must be as small as possible and consume a small amount of power while achieving high pulse magnitude in order to be used in low cost systems based on energy detection [3]. Moreover, the tuning capability of the generator is very important in addressing different applications and different frequency bands.

Several techniques are employed in order to generate UWB pulses such as filter impulse response [4] or Step-Recovery Diode (SRD) [5]. The main disadvantage of the first method is that it requires inductors which occupy a large silicon area whereas the second needs diodes not available in standard CMOS design kit. Moreover, previous methods create frozen pulse shape which can't be modified or tuned. Actually, two main techniques are used to achieve tunable pulse generator. The first one consists of using Local Oscillator (LO) to transpose different baseband pulses in different frequency bands [6]. The tuning capability of this technique is efficient

but it is limited by its starting time which impairs the maximum amplitude and bandwidth [7]. Moreover, due to the consumption of the LO and the mixer, the consumed energy by pulse regarding the pulse magnitude is high. Due to increases in technology performances, elementary pulse combination is often used to achieve fully digital pulse generator [8][9][10]. The main limitation of those generators is the limitation of the pulse magnitude in the upper bandwidth (>5GHz).

In this paper, we propose a fully integrated and tunable UWB pulse generator using H-Bridge principle. The generator structure allows a large variety of pulses to be synthesized. The main limitation is the number of elementary pulse needed which impact the size and the power consumption. Presented version of the generator can create pulse waveform composed by 6 elementary pulses which respects FCC regulation mask and drives 50 Ω differential load. Simulation with a 0.13 μ m CMOS technology design kit shows the generator's ability to achieve 2V_{pp} pulse magnitude with 1.2V voltage supply in a 10dB bandwidth of 5.3 GHz centered at 7.3 GHz and to use pulse repetition frequency (PRF) of 500MHz. Furthermore, the generator contains only custom-made standard CMOS logic cells and an H-bridge driver which implies zero DC consumption and steady energy dissipation around 140pJ by pulse without turning off the generator.

This paper is organized as follows. In Section II, the pulse combination method is explained. Section III introduces the proposed tunable UWB pulse generator based on H-Bridge. Simulation results obtained with 0.13 μ m CMOS technology are shown in Section IV and compared to others design results.

II. PULSE COMBINATION METHOD

As shown in Fig. 1[11], UWB pulses can be parsed by a sequence of elementary pulse. Also, an UWB waveform $s(t)$ can be approximated by a sum of elementary pulse where the n^{th} elementary pulse is characterized by a magnitude of A_n and a width of τ_n . Sequentially it is possible to synthesize a pulse by combining elementary pulse shapes $p_n(t)$ of width τ_n multiplied by their appropriated magnitude (A_n). Resulting UWB pulse $s(t)$ can be written with $\tau_0=0$ as follows :

$$s(t) = \sum_{n=1}^N A_n \cdot p_n \left(t - \sum_{p=1}^{n-1} \tau_p \right). \quad (1)$$

TABLE I. 5th GAUSSIAN PULSE PARAMETERS

n	1	2	3	4	5	6
A _n (V)	0,06	-0,43	1	-1	0,43	-0,06
τ _n (ps)	90	72	68	72	79	90

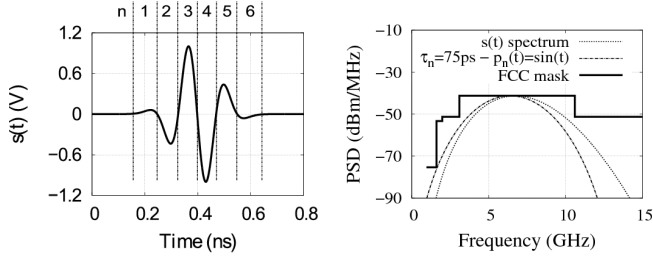


Figure 1. 5th Gaussian pulse [11] with its approximated spectrum

Such method of generation is the more interesting since it is robust against τ_n or $p_n(t)$ variation. As shown in Fig. 1, a good approximation of 5th Gaussian pulse in TABLE I can be achieved with constant τ_n and sinusoidal $p_n(t)$. This allows easy generator settings and the number of necessary elementary pulse N to be easily predicted. Central frequency spectrum f_0 is equal to pulse pseudo-period and can be estimated from the average τ_n as follows :

$$f_0 \approx \frac{N}{2 \cdot \sum_{n=1}^N \tau_n} \quad (2)$$

Moreover, 10dB pulse bandwidth (BW) can be approximated as the invert of pulse length and expressed as follows :

$$BW \approx \frac{2}{\sum_{n=1}^N \tau_n} \quad (3)$$

Finally, the minimum number of necessary elementary pulse N_{min} to respect a given mask can be written as follows :

$$N_{min} \approx \frac{4 \cdot f_0}{BW} \quad (4)$$

Therefore, the more UWB spectrum to generate is narrow, the more number of elementary pulse to combine is high. For example, FCC mask requires at least 4 elementary pulses whereas the first 500MHz channel centered on 3.5GHz of 802.15.4a IEEE norm needs more than 28 pulses.

To illustrate this point, Fig. 2 and Fig. 3 show respectively a pulse shape in time and frequency domains which can be used respectively to match with FCC and ESTI mask. The first UWB pulse is obtained with an ideal 3rd order Bessel filter driven by a triangular generator. Its bandwidth (BW) is tuned to 2.5GHz with an attenuation of 1dB and its central frequency is set to 8GHz. The second pulse is the response of an ideal 3rd order Chebyshev filter centered on 7.55GHz. Its bandpass is equal to 1.2GHz with a ripple of 1dB and its bandstop is tuned to 2.1 GHz with an attenuation of 30dB. The impulse response of Bessel filter for FCC mask need 7 elementary pulses to be synthesized and the impulse response of Chebyshev filter for ESTI mask needs more than 30 elementary pulses.

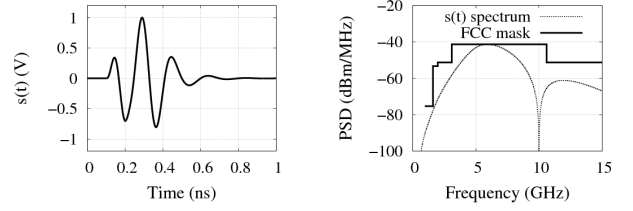


Figure 2. Response of an ideal 3rd order Bessel filter set for FCC band

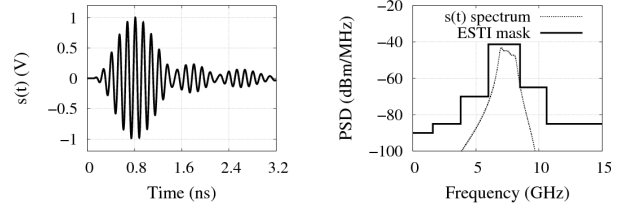


Figure 3. Response of an ideal 3rd order Chebyshev filter set for ESTI band

III. FULLY TUNABLE PULSE GENERATOR DESIGN

A UWB pulse generator based on the pulse combination method uses two main functions. The first is it generates all elementary pulses with their associated width and the second is it combines each pulse at the output stage with a desired magnitude. A bloc diagram schematic is shown in Fig. 4.

A. Gaussian-like Generator Design

As shown in Fig.5, elementary pulses are generated by digital triangular generator [4][8] which uses a digital delay line to propagate a positive edge. Two consecutive edges are then combined using logic gate (OR and AND) to generate an elementary pulse (EPn) and its opposite (EPnN) needed to command the H-Bridge. The delay between two consecutive edges sets the width of the elementary pulse (τ_n) and must be tunable. Particular attention must be paid to the matching between an elementary pulse and its opposite because mismatch between EPn and EPnN degrades the combination in the H-Bridge. Moreover, the elementary pulse generator must achieve pulse width less than 60ps with the 0.13μm used CMOS technology, to cover the full FCC band.

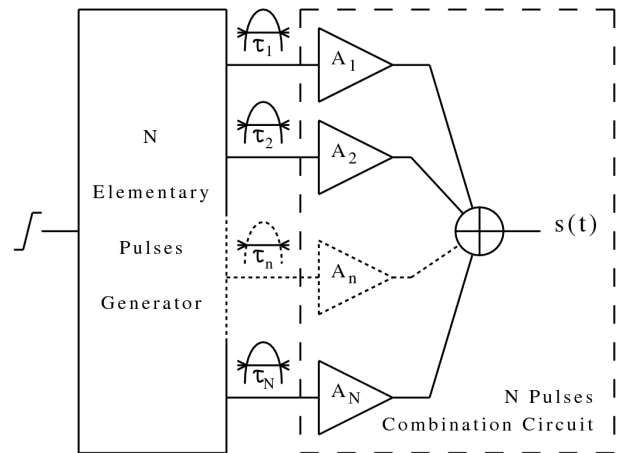


Figure 4. Bloc diagram of pulse generator using combination method

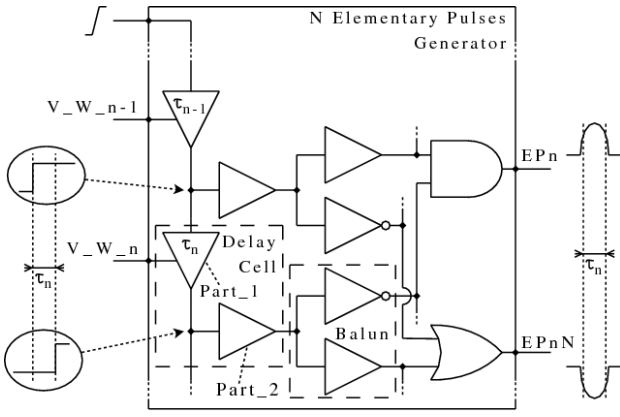


Figure 5. Simplified schematic of elementary pulses generator

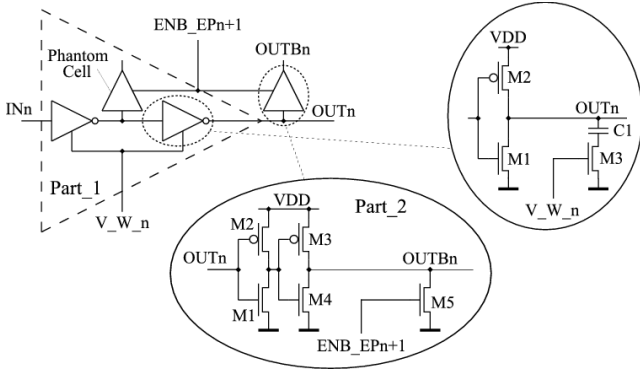


Figure 6. Electrical structure of the used delay cell

Achievement of a triangular generator is directly bound up by the design of Voltage Control Delay Line (VCDL) which consists of tunable delay buffer. As shown in Fig. 6, a delay cell is built up of two parts (Part_1 and Part_2). Part_1 consists of two stages based on CMOS inverter loaded on a capacitor (C1) in series with a NMOS analog "switch" (M3) and it drives the next delay cell. Variation of voltage applied on M3 (V_{W_n}) changes the current in C1 and allows elementary pulse width (τ_n) to be modified. C1 is sized to achieve delay from IN_n to OUT_n , between 50ps and 100ps ($C1=500fF$). The main advantage of this delay cell structure is its low sensitivity to control voltage variation. The second part of the cell (Part_2) is made up of two CMOS inverters and one "reset transistor" (M5), which enables the propagation through the delay line to limit the number of elementary pulses in case of short pulse generation. As shown in Fig. 6, a phantom cell is inserted to ensure a constant load between each elementary delay cell.

Final stage of elementary pulse generator is achieved by standard NAND and NOR logic gates with an inverter at their output. To achieve complementary elementary pulses these gates need to be driven by two complementary command signals issued by the delay line. To generate those signals, buffers based on CMOS inverter are used. The first and the last inverters are sized with the fan out law in order to optimize signal propagation. To obtain synchronized balanced signals, an intermediate series inverter and an intermediate parallel inverter is inserted respectively in the unbalanced and the balanced path as represented in Fig. 7.

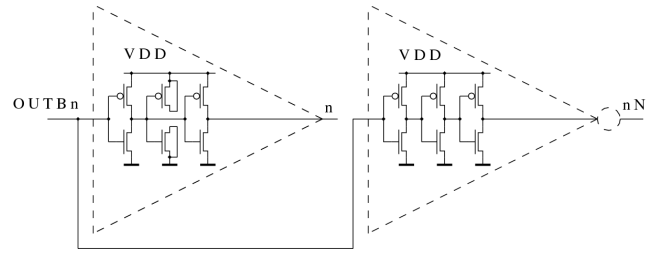


Figure 7. Electrical structure of the designed balun

B. H-Bridge Design

To maximize the pulse's magnitude, the presented design uses a customized H-Bridge to drive the 50Ω output antenna. As shown in Fig. 8, the driver circuit consists of CMOS transmission gate and allows the peak to peak magnitude of the UWB pulse to stretch a theoretical value of $2V_{DD}$. Each elementary pulse (EP_n) and its complementary (EP_{nN}) command two transmission gates (TG_{nN} and TG_{nP}). The magnitude of each elementary pulse (A_n) is set by the DC voltage (V_{M_n}) of each branch. Positive and negative elementary pulses are combined by current sum in the load [12]. In comparison with classical differential structure, the impact of this driver on the power consumption is minimized because it consumes zero DC power. Moreover, pulse combination method using H-Bridge enables to synthesize UWB pulse composed by a high number of elementary pulses which allows a large tuning of the pulse spectrum. If some transmission gates are not needed (to synthesize short pulse), they are on high impedance state because they are disabled.

As shown in Fig. 8, transmission gates are achieved by a NMOS in parallel with the associated balanced PMOS transistor. For sizing the NMOS transistor width, it is necessary to make a tradeoff between the maximum pulse magnitude and H-bridge power consumption. To achieve pulse magnitude of 2V (peak to peak) on 50Ω load, the width is around 200μm for the 0.13μm used CMOS technology. The PMOS transistor associated is a 460μm width which can lead to a large silicon area in the case of narrow band pulse. Considering the large size of the transmission gate transistors, it is necessary to insert, between the elementary pulse generator and the H-bridge, a buffer based on four CMOS inverter designed using the fan out laws.

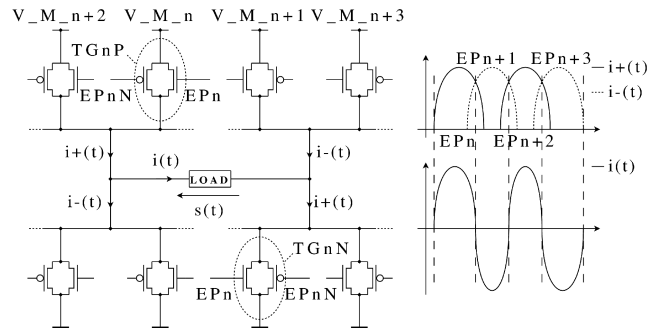


Figure 8. H-Bridge combination principle

Due to the shape of the elementary pulse which commands the transmission gate and due to the time response of the gate, there is an aliasing in the conduction time between TGn gates (TGnN and TGnP) and TGn+1 gates (TGn+1N and TGn+1P) which results in narrower generated elementary pulse. This phenomenon is represented in Fig. 8. It implies that delay cells which generate the first and the last effective elementary pulses have to be tuned separately, in order to apply the width reduction to these pulses.

Finally an additional transmission gate stage is added. For a pulse generation using N elementary pulses, this stage is commanded by a N+1 elementary pulse which occurs at the end of the pulse. This stage is tuned at 0V in order to short-circuit the load at the end of the UWB pulse to discharge the parasitic capacitors and avoid a time spreading of the pulse.

IV. SIMULATION

A. Simulation Results

The proposed UWB pulse generator is designed with standard 0.13 μ m CMOS technology design kit and simulation results are obtained with the software ADS for a supply voltage of 1.2V.

Pulse generation is based on a tunable delay line. One advantage of this architecture is the delay per stage could be tuned to set the delay in presence of Process Voltage Temperature (PVT) variation and hence the center frequency of the pulse. The elementary pulse generator simulations shows in Fig. 9 its ability to generate a minimum pulse width of 60ps (narrower pulse width leads to lower pulse magnitude and can not efficiently command the transmission gates) which is sufficient to cover the FCC band. This allows pulse to be centered on 8.33GHz.

A six order pulse generator has been designed for the FCC band. A first example of pulse generation is given in Fig. 10. The generator is set to synthesize a Gaussian pulse modulated by a sinusoid. In this case all the elementary pulses have the same width which limits the amount of input of the final circuit and simplifies the circuit measurement. The setting of the different control voltages needed to generate this pulse and the different values of A_n and τ_n are summarized in Table II. The pulse is compliant with the FCC spectral mask and its 10dB bandwidth is 5.3GHz centered on 7.3GHz. The pulse magnitude is $2V_{pp}$ and its duration 0.42ns. The control voltage used to set the programmable generator is linearly extrapolated from the value of A_n as shown in Fig. 12. This shows the very small distortion involved by the H-bridge and the ease of tune of the generator. Fig. 11 underlines the generator's ability to generate different UWB pulse shapes. In this case, a Bessel filter response is generated with the values shown in Table III resulting in narrower pulse bandwidth and a different pulse shape.

An approximation of the silicon area of this generator can be made from the size of the transmission gate and the number of elementary pulses needed to synthesize the pulse. In the technology used, a 200 μ m NMOS transistor and a 460 μ m PMOS transistor with 10 μ m finger occupy a silicon area of

respectively 170 μ m² and 460 μ m². The designed generator will occupy 0.02mm² and a pulse generator for ECC band having 20 elementary pulses would occupy 0.05mm².

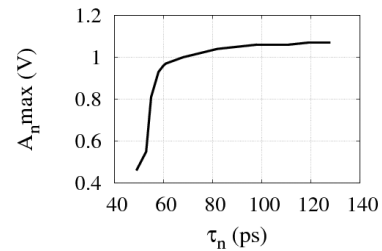


Figure 9. Maximum elementary pulse magnitude versus its width

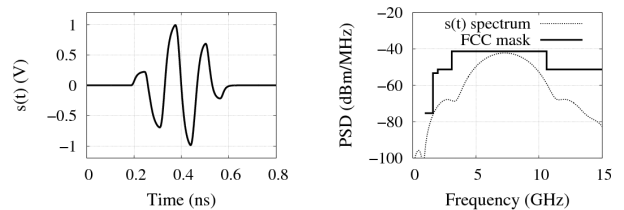


Figure 10. Pulse obtained with the proposed generator on 50 Ω (Table II)

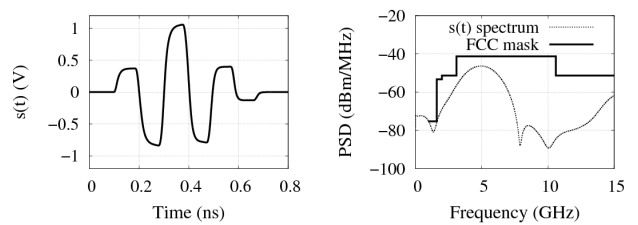


Figure 11. Pulse obtained with the proposed generator on 50 Ω (Table III)

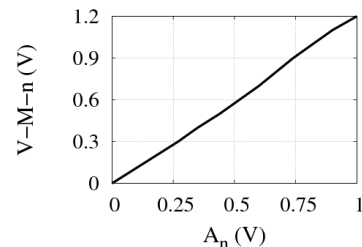


Figure 12. Control voltage V_{M-n} versus pulse magnitude A_n on 50 Ω

TABLE II. PULSE PARAMETERS OF SINE MODULATED BY GAUSSIAN

n	1	2	3	4	5	6
A_n (V)	0.22	-0.69	1	-1	0.69	-0.22
τ_n (ps)	71	71	71	71	71	71

TABLE III. PULSE PARAMETERS OF BESSEL FILTER RESPONSE

n	1	2	3	4	5	6
A_n (V)	0,35	-0.8	1	-0,75	0.37	-0.12
τ_n (ps)	101	101	101	101	101	101

B. Performances Comparison

The simulated power consumption is 26.8mW for a Pulse Repetition Frequency of 200MHz. The energy consumed by pulse is then 140pJ. In comparison to previous published works, this consumption is high, as shown by Table IV. But, it is important to emphasize the fact that the energy by pulse criterion suppose that the power supply is turned off between two consecutive pulses to be independent of frequency. The total power consumption depends on the performances of the power manager circuit and the power consumed during the time needed to turn on and off the system can not be evaluated. As shown in Fig. 13, the presented pulse generator consumes zero DC current. This generator does not need power management to achieve a consumption of 140pJ by pulses. It's high in comparison with other generators but energy efficiency is better than previous works thanks to maximum pulse magnitude.

Moreover, the power consumption of the presented generator is essentially due to the size of the transmission gates. Such widths are used to achieve large pulse magnitudes in order to increase the transmission range. It is trivial to say that smaller pulse magnitude would lead to a smaller transmission gate and smaller consumed energy by pulses. To achieve a comparison of the energy by pulse regarding the pulse magnitude the following figure of merit is introduced:

$$\eta = \frac{E}{V_{pp}} \quad (5)$$

where E is the consumed energy by pulse and V_{pp} the peak to peak pulse magnitude. Simulated pulse generator performances are summarized and compared with others generators in Table IV. The consumed energy by pulses by volt is 70pJ.

TABLE IV. PERFORMANCE SUMMARIZE OF PROPOSED GENERATOR AND COMPARISON WITH PREVIOUS WORKS

Reference	Technology (μm)	V_{DD} (V)	V_{PP} (V)	E (pJ/pulse)	η (pJ/pulse/V)
[6] - 2007	CMOS-0,18	1,5	0,18	18pJ	100
[13] - 2006	CMOS-0,18	1,8	0,9	180pJ	200
[9] - 2007	CMOS 0,09	1	0,65	47pJ	72.3
[7] - 2008	CMOS 0,18	1,5	0,16	16,8pJ	105
This Work	CMOS 0,13	1,2	2	140pJ	70

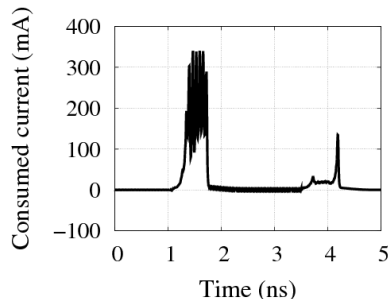


Figure 13. Consumed current at PRF=200MHz

V. CONCLUSION

The use of a H-Bridge as pulse combination circuit in fully tunable generator is proposed and simulated with 0.13 μm CMOS technology. Simulation results show the circuit ability to generate different pulse shapes with peak to peak pulse magnitude of 2V with supply voltage of 1.2V. The pulse generator consumes zero DC power and 140pJ by pulse. Finally, the performances of the H-bridge allow the generation of pulse spectrum close to the predicted one which allows simple pulse tuning.

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