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CMOS UWB Pulse Generator Co-Designed with Package Transition

S. Bourdel, J. Gaubert, O. Fourquin, R. Vauche, N. Dehaese

Aix-Marseille University, IM2NP, and CNRS, IM2NP (UMR 6242), Campus de Saint-Jérôme, Avenue Escadrille Normandie Niemen - Case 142, F-13397 Marseille Cedex, France

Abstract — The design of an UWB pulse generator is presented in the context of low cost applications. The pulse generator is fully integrated in a 0.13 μm CMOS technology and achieves 1Vpp magnitude pulses with only 2.25pJ of energy consumed by pulse and 1.2V voltage supply. The generation method used in this design is well suited for packaged IC using wire bond interconnections. Two methods of interconnection are presented. It is shown that a co-design of the generator with the package transition can preserve the signal integrity while increasing the pulse magnitude up to 1.4Vpp with the same power budget.

Index Terms — Pulse Generator, UWB, Packaging.

I. INTRODUCTION

The demand for low cost wireless systems is constantly increasing due to the development of applications like Piconet, PAN, or RFID, for which the production cost of the transceiver is crucial. For such applications, UWB Impulse Radio is a good solution because of its simplicity, its diversity path immunity and its localization capability.

To address the low cost market, IR-UWB must use energy detector receiver instead of coherent detection to avoid the use of complex synchronization schemes and powerful digital sections. In transceivers using energy detection, the energy of the emitted pulse must be maximized to ensure the range. Such energy maximization is possible since the peak power limitation imposed by the FCC is 0dBm in 50MHz RBW which allows high energy pulses [1]. But, the generation of high pulse using low cost technologies such as CMOS is currently a bottleneck.

Among the various techniques used to generate pulses [2][3][4], the filter impulse response method has a great potentiality for generating pulses with magnitude around 1Vcc [4]. Moreover, it appears that for FCC systems, the order of the emission filter is low enough to be fully integrated in CMOS technologies on less than 1 squared millimeter area.

In the case of fully integrated systems, the die must be packaged. For UWB generators, high frequency package transition must be used to preserve signal integrity which is a major drawback for the system cost. To avoid the use of an expensive package, it is possible to co-design the emission filter of the generator using the transition because this transition acts as a filter. In this approach, parts of the emission filter are embedded in the package transition and other parts are implemented On Chip. Such an approach is

particularly well suited for low cost packages like BGA since they use bonding [5].

In this paper, we present the design of a fully integrated unipolar pulse generator using filter impulse response. The pulse generator is designed for OOK modulation and is compliant with FCC regulation mask. It achieves 1Vpp pulse magnitude and the die area is 0.38mm². Based on this generator, we propose a method to co-design the emission filter of the generator and the transition used in the package. We show that such a co-design reduces the inductor number which results in a die size of 0.23mm². Moreover, this co-design approach limits the losses of the filter which increases the pulse magnitude since the bonding is a better inductor than integrated inductors. At last, such a co-design approach is useful to other pulse generator topologies since it uses emission filter.

The paper is organized as follows. In section II, the generation method, based on the filter impulse response excitation, is presented. The fully integration of the generator in a 0.13 μm CMOS technology is then described in section III. Section IV deals with the interconnection methods and presents a co-design of the generator with the package transition.

II. IMPULSE RESPONSE GENERATION METHOD

The impulse generation method consists on exciting a filter with a very short baseband pulse ($g(t)$) to generate its equivalent Dirac response ($h(t)$). $g(t)$ is commonly achieved by a digital baseband pulse generator [4] which is well suited to CMOS technologies. If we assume $g(t)$ to be a square function of width equal to τ . The spectrum of the emitted pulse is :

$$(1) \quad S(f) = A\tau \text{sinc}(\pi\tau f) \cdot H(f)$$

In the case of linear modulation such as OOK or BPSK the Power Spectrum Density (PSD) of the emitted signal can be expressed as follows:

$$(2) \quad PSD_e(f) = \frac{\sigma_a^2}{T_s} |S(f)|^2 + \frac{\mu_a^2}{T_s^2} |S(f)|^2 \sum_{i=0}^{\infty} \delta\left(f - \frac{i}{T_s}\right)$$

Where μ_a^2 and σ_a^2 are respectively the mean and the variance of the data sequence $\{a_k\}$ and T_s the symbol time. If we take into account the filter losses (1) and the antenna impedance (Z_0) the emitted signal PSD is given by:

$$(3) \quad PSD_e(f) = \frac{(A\tau \text{sinc}(\pi\tau f) |H_e(f)|)^2}{lZ_0T_s} \left\{ \sigma_a^2 + \frac{\mu_a^2}{T_s} \sum_{k=-\infty}^{\infty} \delta\left(f - \frac{k}{T_s}\right) \right\}$$

where $H_e(f)$ is the normalized function transfer of the filter. The signal PSD is composed of a continuous spectrum and, when the mean of the sequence is not zero, a discrete spectrum. The equ. (3) shows how the PSD is impacted by the main generator parameters such as : modulation type (OOK, BPSK), filter characteristics (order, nature, losses), baseband pulse magnitude (A) and width (τ). Those parameters (summarized in Table I in the case of the presented design) must be set to have a signal PSD compliant with the FCC standard while taking into account the constraints due to technology. In our case of study, the PSD is plotted in Fig. 1(a). Here, the magnitude of the discrete spectrum must be evaluated since it is much higher than the continuous spectrum. To maintain a high pulse magnitude it is possible to decrease the symbol rate in the case of OOK modulations. Moreover, the equ. (3) determines the filter characteristics. For FCC standard, low order filter can be used which is a major advantage since the losses of CMOS integrated filter dramatically grow with the order. At last, Equ. (3) shows the impact of the characteristics of the baseband pulse ($g(t)$) on the PSD. τ impacts the spectral efficiency of the signal and the energy of the pulse. The decrease of τ increases the spectral efficiency since it limits the influence of the sinus cardinal function but, at the same time, it decreases the energy of the pulse. A value of 75ps is good tradeoff and can be achieved with baseband pulse generator in the targeted technology [4].

TABLE I
SUMMARY OF THE GENERATOR CHARACTERISTICS

Filter	fo	6.9GHz
	BW (-3dB)	5.4GHz
	Nature	3rd order Bessel
	Power losses	3dB
Modulation	Nature	OOK
	ma	0.5
	sa2	0.25
	Rate	36Mbs-1
Base Band Pulse	A	2.9V
	t	75ps

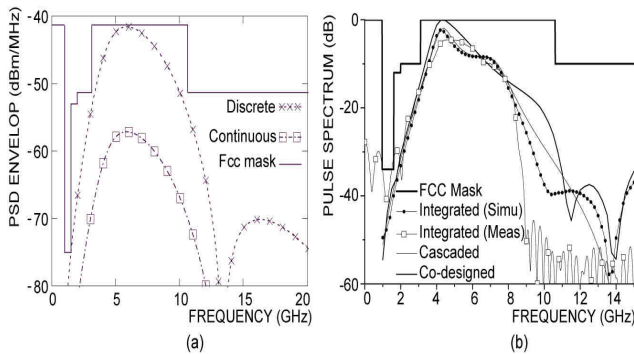


Fig. 1: (a) Theoretical signal PSD, (b) pulse spectrum of the different generators

III. FULLY INTEGRATED PULSE GENERATOR DESIGN

As shown in Fig. 2, the pulse generator is composed of three elements: a baseband pulse generator often called triangular pulse generator, a filter driver and an on-chip filter.

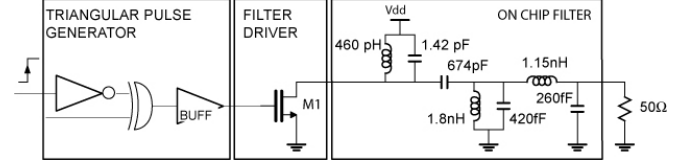


Fig. 2: Pulse Generator Topology

Because CMOS technologies provide low quality passive devices the design of the on-chip filter is crucial. A major problem lies in the use of inductors which achieve low Q factor. Moreover the value of the Q factor (and also the self frequency resonance) depends on the inductor value. Fortunately, due to large relative bandwidth imposed by FCC (close to 1), the range of L needed to implement the filter is not excessive. It is then possible to choose inductors that have good Q factor to limit losses. In our case, a 3rd order Bessel using the topology presented in Fig. 2 leads to inductor values between 0.5pH and 2nH. In the targeted technology, such inductors have acceptable Q-factor (higher than 8) and their nominal values do not vary more than 100% in the full UWB bandwidth.

As specified in the previous section, the baseband pulse at the filter input must have a voltage magnitude of 2.9 V to maximize the signal PSD. To reach magnitude greater than V_{DD} the filter must be driven in current mode as shown in Fig. 2. The baseband pulse is applied to the gate of M1, which provides a current pulse at the filter input. M1 must be sized with regard to the pulse magnitude needed at the filter input ($A=2.9V$) and the filter input impedance (50Ω for a 3rd order Bessel filter loaded by a 50Ω antenna). In the case where $g(t)$ is a square function with magnitude equal to V_{DD} , the current given by M1 to the load during the time τ can be approximated using the small signal assumption. Under this assumption the width of M1 can be expressed as follows:

$$(4) \quad W = \frac{L \cdot A}{Z_0 \cdot \mu_0 \cdot C_{ox} (V_{DD} - V_t)^2}$$

The M1 width is 100 μ m to generate a current pulse of 60mA magnitude, equivalent to a voltage pulse of 2.9V with a 50 Ω impedance. The drain of M1 is biased using the first resonator of the filter and the gate is not biased to operate in C class in order to reduce power consumption.

To drive M1, a buffer must be inserted in the triangular pulse generator. The transistor sizes of the baseband pulse generator are the smallest the technology allows to achieve pulse width of 75ps. The buffer consists of six cascaded

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED PULSE GENERATOR WITH PREVIOUSLY PUBLISHED WORKS

References	V _{pp} (V)	V _{dd} (V)	Pulse Width (ns)	BW (-10dB)	Technology (μm)	Power Cons.	Energy Cons. (/pulse)	area (mm ²)	Modulation
[2] - 2007	1,24	2,2	1,75	1,4GHz	CMOS-0,18	29,7mW@36MHz	-	0,4 (core)	DBPSK
[3] - 2007	0,18	1,5	3,5	500MHz	CMOS-0,18	1,82mW@100MHz	18pJ	0,39 (die)	OOK
[6]- 2006	0,9	1,8	2,5	1,2GHz	CMOS-0,18	1,8mW@10Mp/s	180nJ	1,21 (die) / 0,57 (core)	BPSK
[7]- 2007	0,65	1	3	550MHz	CMOS 0,09	-	47pJ	0,08 (core)	DBPSK
[8]- 2008	0,16	1,5	3,5	520MHz	CMOS 0,18	1,68mW@100MHz	16,8pJ	0,3 (core)	OOK
This Work	1	1,2	0,6	4,3GHz	CMOS 0,13	2,7mW@200MHz	2,25pJ	0,38 (core)	OOK

inverters. The width of each inverter is twice the width of the previous one to achieve a smooth size transition between the small transistors of the base band generator and M1.

The pulse generator has been realized using a 0.13μm standard CMOS technology from ST-Microelectronics and performs well compared to pulse generators recently published and presented in TABLE II. As shown in Fig. 3 the measured pulse magnitude is 1V_{pp} with only 1.2V voltage supply. Moreover the power consumption is 2.7mA for a Pulse Repetition Frequency (PRF) of 200MHz and the energy consumed by pulse is very low (2.25pJ/pulse), regarding the pulse magnitude. The power consumption performances of the generator show the efficiency of the current driver which consumes no DC current while no pulses are transmitted. Simulation and measurement shown in Fig. 1(b) concord and the measured spectrum is compliant with FCC regulation mask. The measured BW is 4.3GHz and the pulse width is 0.6ns. The die photograph is presented in Fig. 4. The silicon area is 0.38mm².

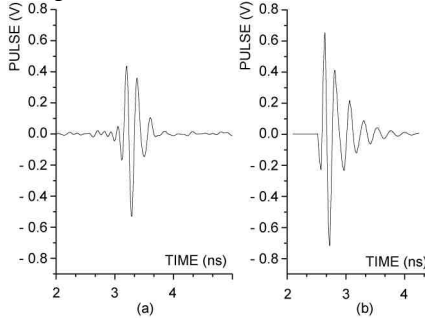


Fig. 3 : output of the measured integrated generator (a) and of the simulated co-designed generator (b)

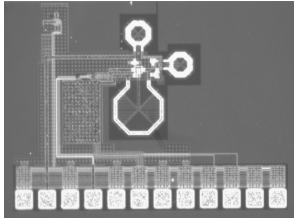


Fig. 4 : Die photograph of the fully integrated pulse generator.

III. PULSE GENERATOR PACKAGING

A key point in radio frequency applications and more specifically for UWB applications where large bandwidths

are used is to connect the die with the antenna without impairing the signal integrity. To achieve low cost, in UWB applications the antenna can be directly printed on the chip carrier [9]. In this section we study different ways to connect the pulse generator described in section II to a 50Ω ground coplanar transmission line which is used to drive a 50Ω printed antenna. We used a standard laminate (RO4003) as chip carrier and wire bond attaches. Such a carrier to die transition can be modeled by a π network when the through phase shift associated to the transition is low [5]. Such conditions are achieved in the UWB frequency band for sub millimeter wire bond lengths. The equivalent π model of the wire bond transition is given in Fig 5(a). The values of the model parameters can be obtained accurately from measurements or EM simulations [5]. The value of L_{WB} is linked to the wire bond length while the value C_{OnDie} is mainly given by the pad of the silicon chip. C_{OnDie} do not penalize the bandwidth because it can be included in the 260 fF capacitor of the on chip filter of the pulse generator (see Fig. 2). The wire bond transition bandwidth can be extended by adding a capacitor δC_{OffDie} in parallel to C_{OffDie} in order to synthesize a standard LC second order low pass filter [5] shown in Fig. 5(b). This way the packaged pulse generator performs like the on chip pulse generator cascaded to the second order filter. So to maintain the signal integrity this second order filter must have a cutoff frequency larger than the UWB frequency range. The standard LC second order low pass filter, which is defined by the coefficients g_1, g_2, g_3 [10], is given in normalized values in Fig. 5(b). We used a 1.3 dB ripple Butterworth response with a cut-off frequency of 11 GHz. Such Butterworth response with a low ripple value produces 50Ω termination, low group delay ripple and low attenuation in the UWB bandwidth. The filter element values are given by:

$$(5) \quad L_{WB} = Z_0 \frac{g_1}{2\pi f_{cutoff}}$$

$$(6) \quad C_{OffDie} + \delta C_{OffDie} = \frac{g_2}{2\pi f_{cutoff} Z_0}$$

That leads to a 0.8 mm wire bond length, and a shunt capacitance value $\delta C_{OffDie}=190$ fF. This capacitor value can be implemented on the chip carrier by decreasing the characteristic impedance of the transmission line near the wire bond transition. Fig. 6 shows the HFSS model of the

modified wire bond transition which has been used to compute the scattering parameters of the transition. The simulated output spectrum of the pulse generator cascaded with the transition is given in Fig. 1(b). We can notice that the modified WB transition does not significantly impair the signal integrity of the emitted pulse. The simulated pulse magnitude in the time domain is 1.05Vpp and is roughly the same as the on chip pulse generator pulse magnitude.

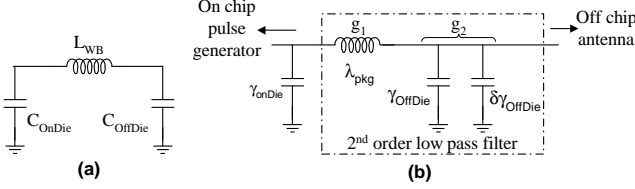


Fig. 5 : (a) Wire bond transition lumped equivalent model. (b) 2nd order low pass filter based on the bond wire transition model.

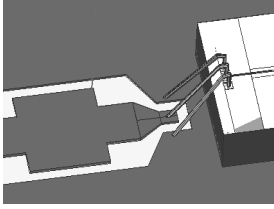


Fig. 6 : HFSS model of the modified bond wire transition.

Another way to maintain the signal integrity of the packaged pulse generator is to embed the carrier to die transition in the pulse generator filter. Indeed, as shown in Fig 7, the π model of the transition can be used to build the last π section of the pulse generator filter. The wire bond length must be sized so the inductor L_{WB} of the π model of the transition match the filter inductor value.

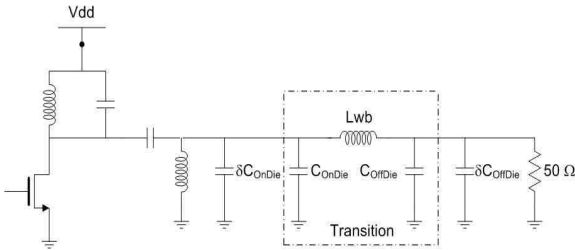


Fig. 7 : Pulse generator co-designed with the wire bond transition.

By using EM simulation tool we obtain a wire bond length of 1.4 mm and C_{OnDie} and C_{OffDie} of 120 fF and 60 fF respectively. In order to synthesize the desired filter a lumped capacitor on die (δC_{OnDie}) and a distributed capacitor on the chip carrier (δC_{OffDie}) have been added to match the filter capacitors values. The simulated output spectrum of the co-designed pulse generator is given in Fig. 1(b). Using a co-design process has several advantages. First the silicon

area is reduced. Indeed, the last on chip inductor in Fig. 2 is replaced by the wire bond and the silicon area is so reduced to 0.23mm². Moreover, in CMOS technology, inductors have poor quality factor. In the co-designed pulse generator, due to the wire bond which has a high quality factor, the filter losses are reduced and the pulse amplitude is increased from 1Vpp to 1.4Vpp as shown in Fig 3(b).

CONCLUSION

The design of an UWB pulse generator is proposed and implemented in a 0.13mm CMOS technology showing the potential of this design to generate large pulse magnitude (1Vpp) with voltage supply of 1.2V while consuming a small amount of energy by pulse (2.25pJ). Moreover, this generator is well suited to wire bond package transitions and a co-design method can lead to pulse magnitude of 1.4Vpp and reduce the chip size to 0.23mm².

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