



HAL
open science

Electrical Characterizations and evaluation of thermo-mechanical stresses of a power module dedicated to high temperature applications

Laurent Dupont, Zoubir Khatir, Stéphane Lefebvre, Régis Meuret, B Parmentier, S Bontemps

► To cite this version:

Laurent Dupont, Zoubir Khatir, Stéphane Lefebvre, Régis Meuret, B Parmentier, et al.. Electrical Characterizations and evaluation of thermo-mechanical stresses of a power module dedicated to high temperature applications. EPE 2005 - 11th European Conférence on Power Electronics and Applications, Sep 2005, Dresde, Germany. 11p, 10.1109/EPE.2005.219580 . hal-01704015

HAL Id: hal-01704015

<https://hal.science/hal-01704015>

Submitted on 8 Feb 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Electrical Characterizations and evaluation of thermo-mechanical stresses of a power module dedicated to high temperature applications

L. Dupont^(1,2), Z. Khatir⁽¹⁾, S. Lefebvre⁽²⁾, R. Meuret⁽³⁾, B. Parmentier⁽⁴⁾, S. Bontemps⁽⁵⁾

⁽¹⁾INRETS-LTN, ⁽²⁾SATIE ENS Cachan, ⁽³⁾HISPANO SUIZA, ⁽⁴⁾SCHLUMBERGER, ⁽⁵⁾APT EUROPE

Abstract

In avionic area, the trend is to a growing use of power electronics systems. In this context, we will present results concerning test vehicles (power modules) in order to improve a device assembly technology dedicated to be located “on the engine”, in harsh operating conditions with thermal cycling from -50°C to 200°C in the worst case. The paper focuses on failure modes observed under high operating temperature and high temperature cycles, especially ceramic cracks, conchoidal fracture under the copper lead-frame and solder crack initiation. Numerical thermo-mechanical simulations of the assembly allow to understand the origin of the failures and to improve the assembly lifetime under such severe operating conditions. The objectives of the study are to assess the lifetime behaviour of these modules towards both high temperature and thermal cycling effects.

Introduction

Temperature and thermal cycling are generally considered to be the key factors in the reliability of power semi-conductor devices [1]. Avionic applications lead to use power converters in harsh environment with high temperature cycles and elevated ambient temperature when power modules are located on the engine. The application considered in this study is concerning with a three phase inverter for a low power ($< 5\text{kW}$) actuator control. The power electronic part will be located on the engine with a maximum ambient temperature about 200°C . Moreover, the mission profile results for high temperature variation during landing and takeoff phases, in the worst case between from -50°C to $+200^{\circ}\text{C}$, with a rate about $\pm 10^{\circ}\text{C}/\text{min}$. These extremely hard operating conditions result in thermo mechanical stresses and makes the power modules particularly exposed to fatigue failures. Moreover, the required lifetime is about 50,000 hours corresponding to 5,000 to 10,000 cycles.

The aim of this study is to assess the robustness and lifetime behaviour of a dedicated power module towards both high temperature environments and thermal cycling effects required for a specific avionic application. Thus, in this article we present electrical characterizations carried out on specific power modules realised by APT Europe and dedicated to high temperature applications. These measurements were compared with the electrical characterizations realised on discrete devices in epoxy encapsulation, in order to point out the package module influence [2].

As expected, we will show that the Direct Copper Bonding (DCB) technology (AlN with too thick copper films) is not well adapted for avionic constraints, especially under high temperature cycles. Nevertheless, the test vehicles have allowed device characterisations in high temperature adapted packages and studies on the solders. These first results will be completed by investigations on more adapted ceramic substrates such as dimples on DCB, DAB or Si3N4.

In order to evaluate the ability of the power assembly to operate in high temperature environment and its reliability to undergo high temperature cycling variations according to the application requirements, thermal cycling tests have been performed on the tests vehicles. Finally, finite element analysis (FEA) results are presented in order to evaluate mechanical stresses applied to the electronic assembly and to explain the observed failure modes. The combination of experimental and numerical results allowed us to identify the failure modes and helped us to propose solutions in order to improve the device lifetime according to the mission profiles. Furthermore, the aims of these investigations are to identify the main factors that could increase the lifetime expectancy of the power module in such a harsh environment.

Power module dedicated to high temperature application

The test vehicle and module assembly are presented in Figure 1. It has been developed by APT Europe in order to be used in harsh environment for avionic applications where devices are subjected to both high temperature environment and high temperature cycles.

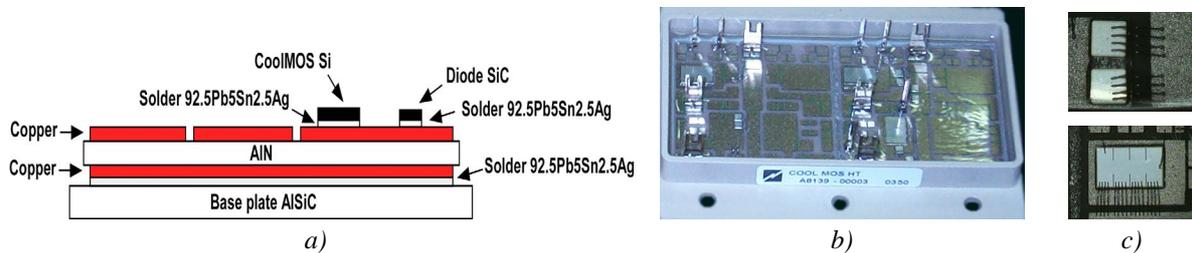


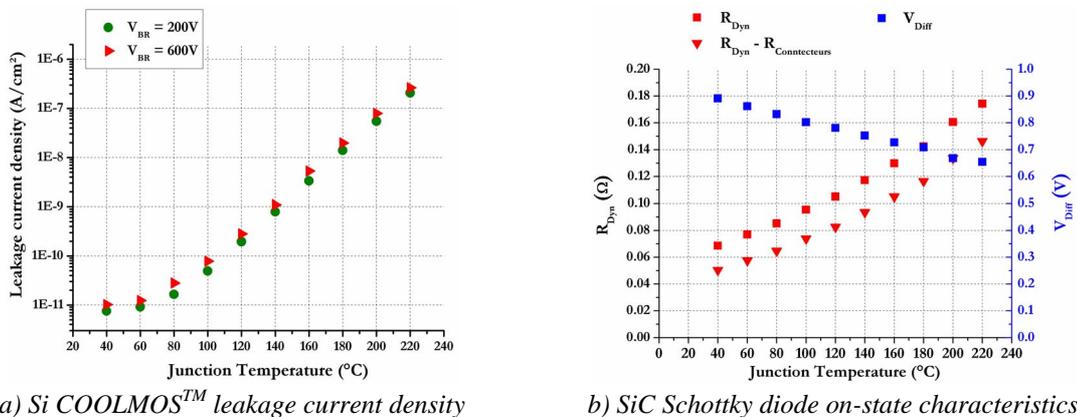
Figure 1 : Presentation of the power module developed by APT Europe
 a) Assembly b) Power Module c) SiC Diode CREE (top view), Si COOLMOS™ APT (bottom view)

Materials selection is made not only to reach the lowest possible junction to case thermal resistance but also to minimize the mechanical stresses caused by thermal expansion coefficients mismatches. This is a very important issue for the reliability of the device. DCB on AIN substrates, AISiC base plate and appropriate solder alloys were selected in order to meet these goals. These modules integrate two electrical functions: a buck chopper for electrical characterisations of each semiconductor types (Si CoolMOS transistor APT 47N60BC3 47A – 600V and SiC Diode CREE CSD1060 10A – 600V) and a phase inverter in order to evaluate electrical functionalities at high ambient temperature (200°C).

The studied power module is used as a test vehicle for evaluating both electrical performances in the 25°C to 200°C temperature range and the ability of the device assembly to undergo high temperature cycles.

Electrical characterization results

Si COOLMOS™ transistors and SiC Schottky diodes integrated in the test vehicle have been characterized. Some electrical characterizations results (leakage current density, on state voltage, threshold voltage and dynamic characterizations) are shown below for junction temperature varying from 40°C to 200°C. A previous paper [3] as already presented in detail electrical characterization results on discrete devices which correspond to the dies integrated in the test module developed by APT Europe. These last electrical characterisations are very similar to those made on discrete devices, so only few results will be presented in this paper.



a) Si COOLMOS™ leakage current density

b) SiC Schottky diode on-state characteristics

Figure 2 : Examples of steady-state electrical characterization results of semiconductor devices integrated in test module.

The leakage current density of the Si CoolMOS™ APT47N60BC3 integrated in the test vehicle is presented in Figure 2a. The leakage current shows a constant value for low junction temperature induced by the DCB leakage current. Figure 2b shows the on state electrical characteristics results (diffusion voltage and dynamic resistance) of the SiC Schottky diode integrated in the module (two dies connected in parallel). The on state characterizations were performed for several temperature levels in order to define the diffusion voltage (V_{Diff}) at zero current and the dynamic resistance (R_{Dyn}) by a linear interpolation for an anode current varying between 3A to 20A. The higher value of the SiC Schottky diode dynamic resistance measured in the module is explained by the resistance of the bond wires and connectors, which has been measured and subtracted.

Figure 3 shows the switching performances of the COOLMOS™ and SiC Schottky diode associated in a buck chopper test circuit which is integrated in the test vehicle. Results are shown for 25°C and 200°C junction temperature. As a result, junction temperature doesn't have significant influence on the switching performances. These results show the ability of 600V Si COOLMOS™ transistors and SiC Schottky diode to be used at high junction temperature, about 200°C.

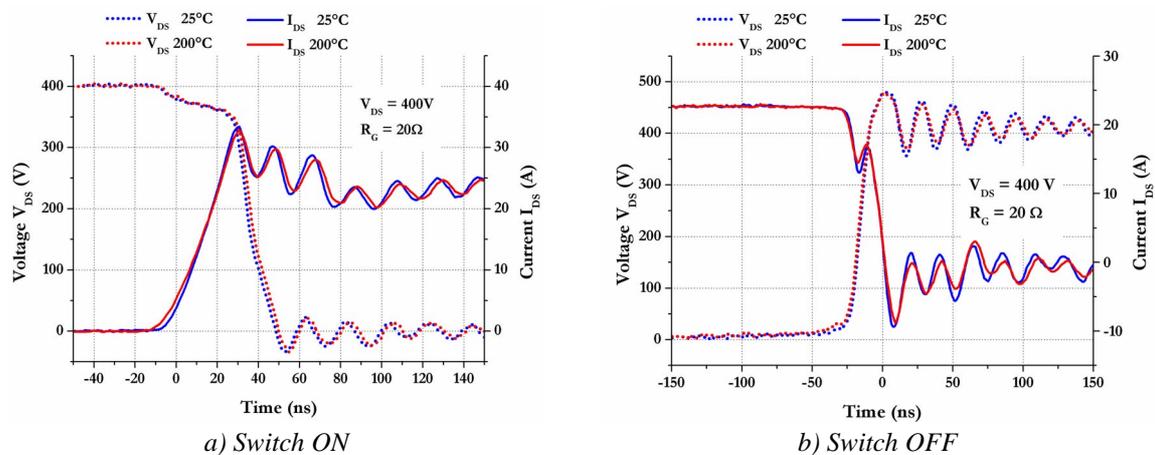


Figure 3 : Switching performances $E = 400 \text{ V}$, $I_L = 20 \text{ A}$ (COOLMOS™ Transistor and SiC Schottky diode)

It is significant to note that problems appeared on the external connectors during the electrical characterizations at high temperature. Indeed, the external connectors solder (Sn95Sb5) present a crack especially induced by the intermetallics growth in Sn solder which finally leads to failure. This failure mode had been presented in various articles about high temperature [4, 5].

Passive thermal cycling tests and results

In order to evaluate the ability of the power assembly to operate in high temperature environment and its reliability to undergo high temperature cycling variations according to the application requirements, thermal cycling tests have been performed. The thermal profile of these tests is presented in Figure 4 where the black dotted line is the ambient temperature in the oven and the red solid line is the module base plate temperature. The cycle duration is about 70mn with a device temperature rate of rise about 8°C/mn and 9°C/mn for the decreasing rate. Temperature varies from -30°C to 180°C. In a first step, in order to get the worst tests conditions, we have applied a very short dwell time (15mn). In these conditions, durations are not sufficient for the solder alloy to have a significant creep effect during dwell time. A second test campaign is under development in order to investigate the dwell time effect and elasto-plastic and creep analysis for the whole loading history will be reported later.

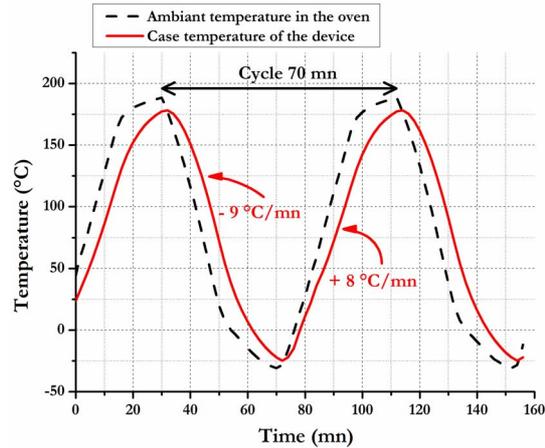
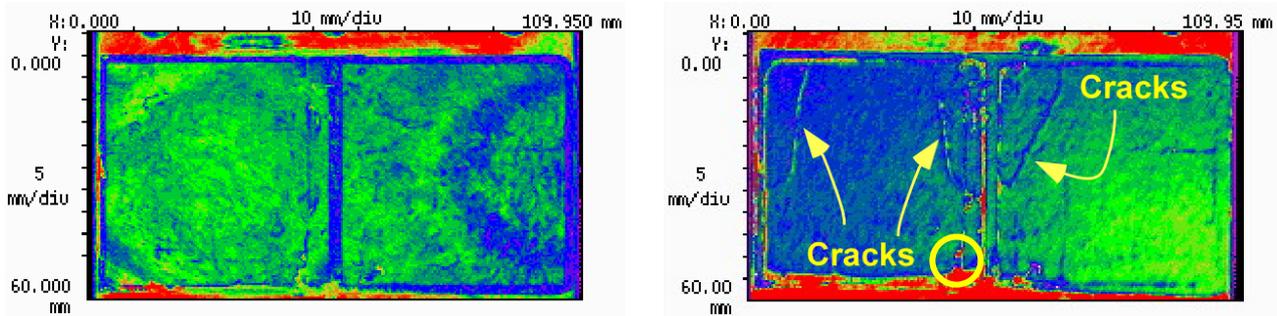


Figure 4 : Passive thermal cycling profile applied onto the test vehicle

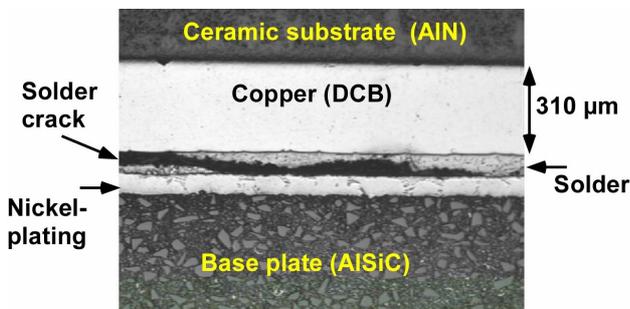
As a result, Figure 5 shows a comparison of SAM analyses of the solder layer between base plate and ceramic between initial state and after 100 cycles. While no damages appear in the initial state (Figure 5a), delaminations, located at some corners of the solder layer, are visible in Figure 5b. These degradations of the solder have been already observed after only 50 thermal cycles in the same proportion. After 100 cycles, acoustic analyses show furthermore longitudinal cracks in the same solder layer, which look like fractures rather than delaminations. One of such a fracture is shown in Figure 6a in its lengthwise. These defects are probably due in one hand to the fact that no stress relaxation occurs in the solder and in the other hand to the high cycling temperature range and especially because of the very low minimum reached temperature (-30°C) where the solder is mechanically hardened before to soften when the temperature rises. Concerning the die attach solder, it seems to remain safe as presented in Figure 6b.



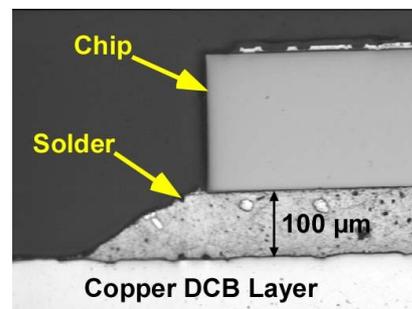
a) Initial acoustic analysis

b) Acoustic analysis after 100 cycles

Figure 5 : Acoustic analysis of the solder / copper DCB interface before and after 100 Cycles



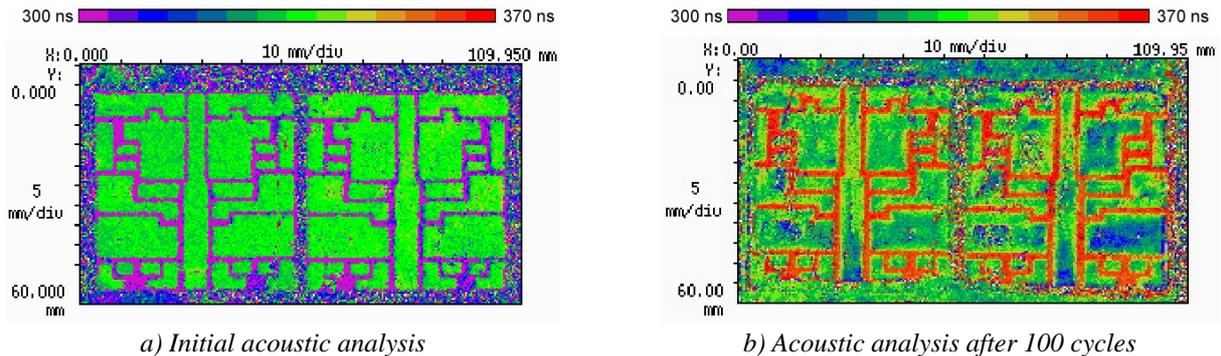
a) Solder between base plate and the copper DCB layer



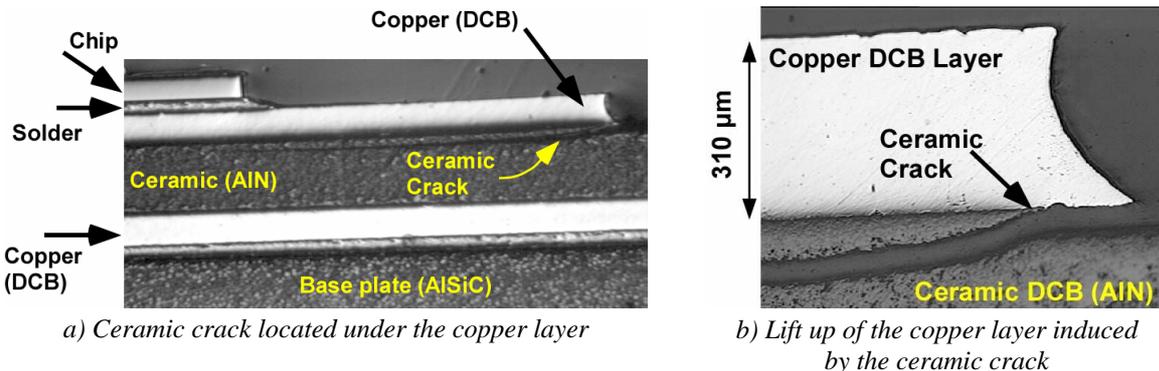
b) Solder between the copper DCB layer and the chip

Figure 6 : Solders after 100 thermal cycles

Figure 7 presents the acoustic analysis realised on the test vehicle before and after 100 thermal cycles. Both images are a time representation of the interface between the ceramic (AlN) and the top copper DCB layer. In Figure 7a (before cycling), we can see that the lead frame echo (in green) is time pinpointed later than the ceramic layer echo (in purple), i.e. that we observed a good assembly of these two layers. Contrariwise, in Figure 7b the ceramic layer echo (in red) is time pinpointed before the top copper layer echo (in green). This lets suppose that the copper lead-frame is dissociated from the ceramic. In order to verify this assumption, a microsection has been performed with all the careful attention needed for a such analysis. As a result, these microsections have confirmed the acoustic analysis results: cracks are visible in Figure 8. As it can be seen in Figure 8a, the crack has propagated from the lead-frame edge until under the chip. This result has been already observed by others authors [6-8]. This failure leads to an increase of the thermal resistance and thermal management problems.



a) Initial acoustic analysis
 b) Acoustic analysis after 100 cycles
 Figure 7 : Acoustic analysis of the interface between ceramics and the copper DCB lead frame before and after 100 thermal cycles



a) Ceramic crack located under the copper layer
 b) Lift up of the copper layer induced by the ceramic crack
 Figure 8 : Optical microscopy analysis of the DCB ceramic (AlN) – lead frame lift up.

No lift off bond wires (100 μ m diameter) have been observed during the thermal cycling test, but the solder of external connectors have been damaged by the increasing of intermetallic and keep off to realise all electrical characterizations. We nevertheless could measure some parameters like threshold voltage, leakage current and on-state voltage which weren't modified after 100 thermal cycling.

Thermomechanical finite element analysis

In order to understand and to corroborate the experimental results such as the ceramic substrate cracks or the solder fracture, the thermomechanical behaviour of the test vehicle during thermal cycling has been simulated. In a more general approach, the aims of these investigations are to assess lifetime expectancy of the power module through the applied stress intensity which are the key factors of the assembly reliability with high cycling temperature. These simulations have been performed by Finite Element Analysis (FEA) with ANSYS 8.0 [9]. Because of high thermal cycling amplitude, the physical parameters are modelled with temperature dependence. Finally, according to the very small time constants of the mechanical stress-strain variables and the rate dependent plasticity of the solder, quasi-static with transient effects calculations have been performed during the simulated thermal cycles.

Finite Element Model

A simple model representative of the power module has been used in a 2D axisymmetric model (Figure 9). The power module is made of an AlSiC base plate where a DCB substrate is soldered with a solder material (92.5Pb5Sn2.5Ag).

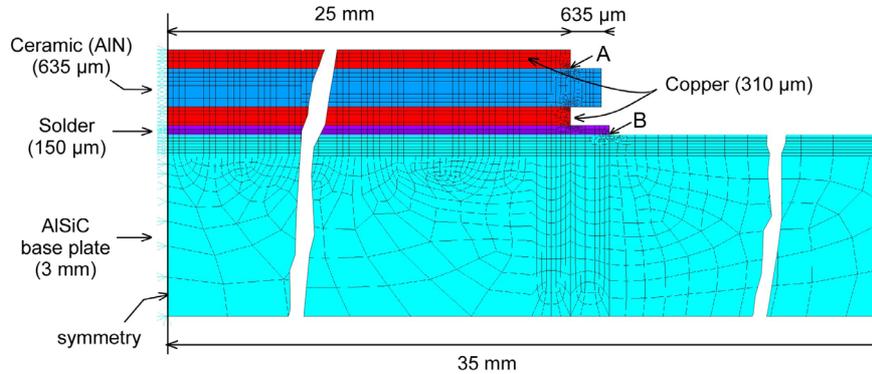


Figure 9 : Finite Element Model of the assembly.

Such a model is rather complex and consequently material properties have to be considered carefully. Both the AlSiC base plate and the Aluminum Nitride ceramic are assumed to be linear elastic. Concerning the 92.5Pb5Sn2.5Ag solder, which has a liquidus temperature near 290°C, it has been considered viscoplastic in order to take into account the rate dependent plasticity (creep behaviour) which occurs over time. Finally, a rate independent plasticity has been considered for the copper layers of the DCB substrate with a multilinear isotropic hardening behaviour (see Figure 10) because the very high temperature swings. The plasticity and thus the strain rate hardening effect are active only after plastic yielding of 49MPa. Material properties are given in Table 1 and the Anand law [10-12] was used for the viscoplastic behaviour of the solder with the parameters given in Table 2, where parameters are defined in [12]. One of the modelling difficulties is due to the geometry where layer thicknesses are very small compared to their areas. The whole model has been meshed with PLANE42 elements except for the solder material which has been meshed with VISCO106 elements for highly non-linear behaviour such as creep. The finite element model required a total of 9514 elements and 9729 nodes.

Table 1 : Materials proprieties used in thermomechanical simulation

Materials	Thickness	CTE	Young's Modulus	Poisson ratio	Specific Heat	Thermal conductivity	Tensile strength
	mm	ppm	Mpa	-	J.Kg ⁻¹ .K ⁻¹	W.m ⁻¹ .K ⁻¹	MPa
AlSiC	3	8	200	0.24	740	190	
Solder 92.5Pb5Sn2.5Ag	0.15	29	24.1-28×10 ³ T(°C)	0.4	130	23	
Copper DCB	0.31	14.5	130	0.34	390	390	
Ceramic (AlN)	0.635	5	320	0.23	730	170	270

Table 2 : Anand parameters for the viscoplasticity properties of 92.5Pb5Sn2.5Ag solder [12]

s ₀ (Mpa)	Q/R (K)	A (s ⁻¹)	ξ	m	h ₀ (MPa)	$\bar{\sigma}$ (MPa)	n	a
C1	C2	C3	C4	C5	C6	C7	C8	C9
33.07	11 000	105 200	7	0.241	1432	41.63	0.002	1.3

The methodology consists to compute, in a first step, the initial mechanical stresses induced by the assembly process when cooling down the solder material from 287°C to 20°C (room temperature). The highest temperature is the liquidus value of the solder for which this material is assumed stress-free. Then, a simulated thermal cycling is applied to the assembly model as presented in Figure 11. The model is first uniformly cooled from 20°C to -30°C with a negative ramp of 10°C/mn, then 30 minutes dwell time followed by heating phase ramp of 10°C/mn until 180°C and 30 mn dwell time and so on.

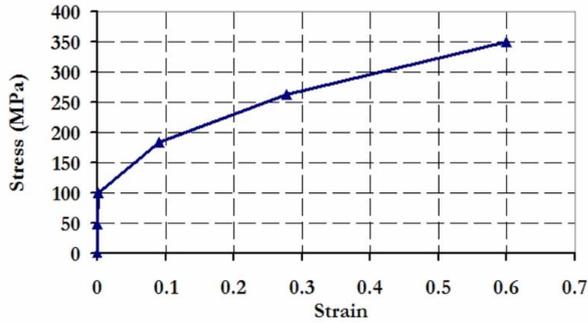


Figure 10 : Multilinear isotropic hardening model for the copper plasticity behaviour [7]

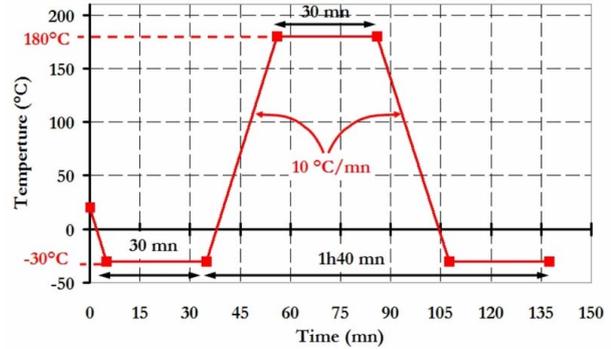


Figure 11 : Simulated passive thermal cycling

Numerical results

The Von Mises residual stresses distribution, after the module has been cooled down from soldering temperature (290°C) to room temperature (20°C), are shown in Figure 12, where only a part of solder material layer and the DCB substrate are visible. As expected, the stress levels are more important in the DCB substrate than in the solder material, with a maximum value of 199 MPa localized at point A in the ceramic (see Figure 9). This is due to the strain hardening of the copper and the high CTE mismatch between the copper lead-frame (14.5 ppm) and AlN ceramic (5 ppm). Indeed, the plastic yielding of the copper metalisations has been reached during the soldering process and this material has hardened leading to high residual stresses in the ceramic. Nevertheless, we did not take into account all the stress history of the metalization such as the DCB process itself and only the soldering process has been simulated in this paper. Lower residual stresses are visible in the solder (Figure 11) which was stress-free at 290°C but its cooling down increases the stress levels until around 28 MPa at the corner edge (point B of Figure 9).

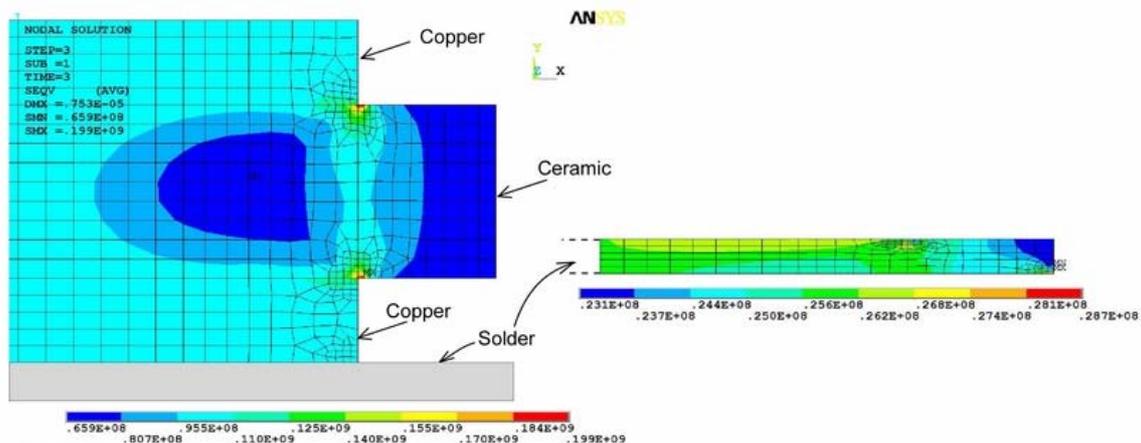


Figure 12: Residual stresses (Von Mises in MPa) in the solder layer and DCB substrate.

The maximum value of stress in ceramic (point A) is plotted with time dependence during thermal cycling in the lower graph of Figure 13 in red solid line (the copper thickness is 310 μm), whereas the temperature cycles are shown in the upper graph between -30°C and 180°C . From the initial value of 199 MPa (Figure 12), the stress level increases at every cycle, according to the strain hardening of the copper layers, and reaches, at the 9th cycle, the AlN tensile strength which is about 270 MPa [13]. This theoretical result means that the ceramic would have cracked. These simulated results confirm the experimental observations described above (Figure 7 and Figure 8). The Von Mises and Shear stress distributions in the DCB assembly are visible in Figure 14 for the 9th cycle and at hottest value (180°C).

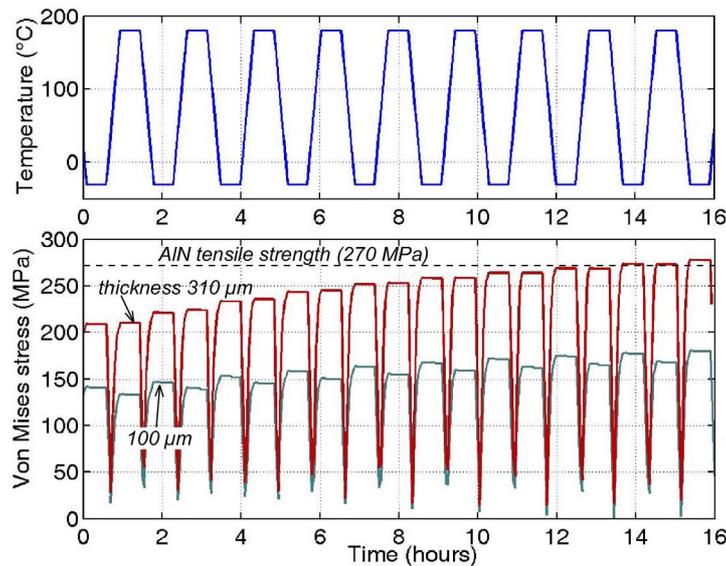


Figure 13: Von Mises stresses evolution in ceramic (point A) and copper thickness effect.

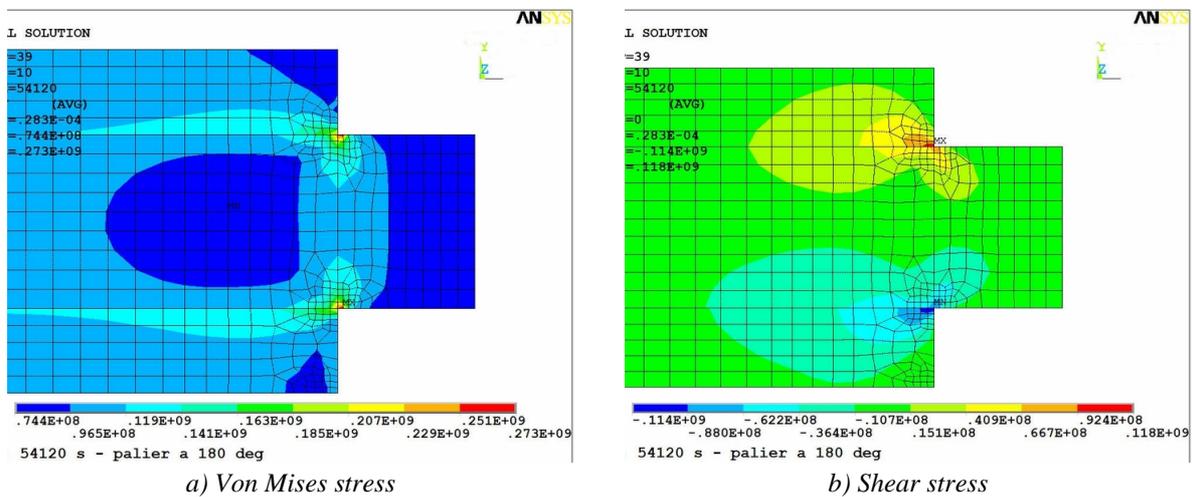


Figure 14: Stress distributions in DCB substrate at the 9th cycle at 180°C .

Such DCB assembly, which is used in the power module presented above (Figure 1), is clearly unsuited for high temperature applications. In order to reach at least 180°C - 200°C maximum temperature with aluminum nitride, one must use thinner copper lead-frames while remaining compatible with the current rating of the module. As illustration, we can see in the lower graph of Figure 13, in green line, the Von Mises stress evolution, at the same location of the ceramic, for 100 μm thickness of copper in both sides of AlN. As a result, the initial stress are significantly lower, around 140 MPa instead of 199 MPa, and the stress increase is smaller and reaches only 178 MPa at the 9th cycle. In these conditions, the assembly may undergo much more thermal cycles before ceramic failure. In an other way, the use of dimples along the copper edges may reduce the ceramic stresses,

but this must be analysed carefully. Other potential solution could be the use of aluminium metalisation for Direct Aluminum Bonding (DAB) which provides much lower yield strength and no significant strain hardening.

The copper hardening is visible in Figure 15, where the shear stress – shear strain loops during thermal cycles are shown. In this figure, total shear strain is taken into account. At the beginning, we can see that shear strain range is maximum whereas the shear stress are minimum. Progressively, during thermal cycles, copper hardens and the shear strain variation decreases whereas shear stress increases symmetrically in both directions.

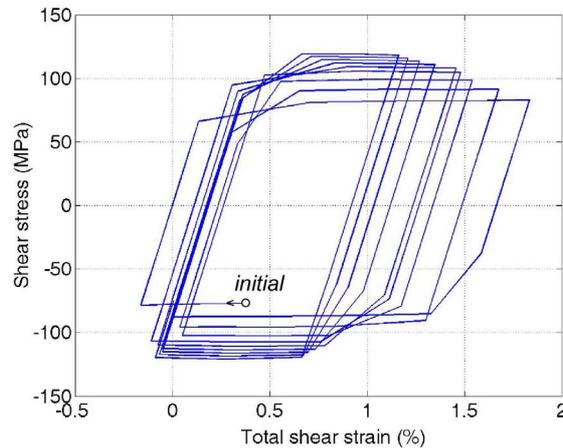


Figure 15: Stress-Strain cycles

We can see, in Figure 16, during two thermal cycles (blue line), the shear stress evolution (red line) in the solder material located in point B (Figure 9), where the stresses are maximum. At the end of the dwell time at low temperature (-30°C), stresses are around -16 MPa in this corner location. Then, as soon as the temperature begins to rise from -30°C to 180°C , shear stress varies very sharply and quasi-instantaneously from -16 MPa to 15 MPa , in such a way that a shear stress variation of more than 30 MPa is applied to the solder. This may explain the fractures obtained experimentally in the power module and visible in Figure 5 and Figure 6. Further investigations have to be performed in order to confirm this hypothesis. Then, during the rise period of the temperature, stresses are relaxed in the solder due to the viscoplastic behaviour until a low value of 1.2 MPa . During the 30 mn dwell time at 180°C , stresses continue to decrease lightly in the solder at constant temperature. When temperature decreases from 180°C to -30°C , stress increases to -20 MPa . Then, during dwell time at -30°C , we observe once again a stress relaxation in the solder. Contrarily at the high temperature behaviour, this last relaxation is very light (from -20 MPa to -17 MPa) due to strengthening of the solder material at low temperature. So the stress relaxation is more important at high temperature (around 13 MPa) whereas at low temperature this relaxation is only 3 MPa .

As a result, a large amount of plastic strain occurs in the solder which can lead to the delamination of this very large layer area. During the thermal cycles, the plastic work density per cycle which is dissipated in the solder at this location (point B) is around 1 J/cm^3 .

Figure 16 gives the shear stress distributions in the solder layer in the vicinity of point B during the dwell times both at -30°C and 180°C . The stress values at point B are those visible in Figure 17 at the same location during the cycle, around 1.2 MPa at 180°C and -17 MPa at -30°C .

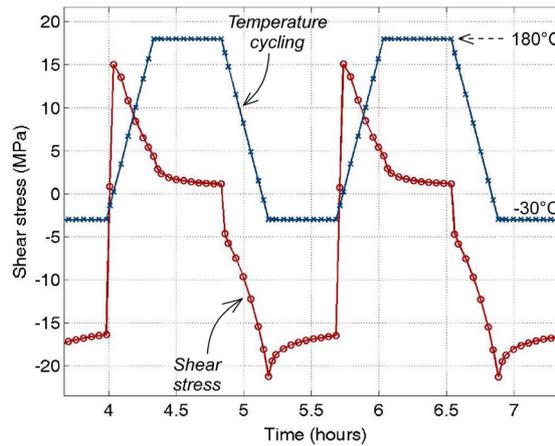


Figure 16: Shear stresses evolution in solder (point B) and temperature cycling.

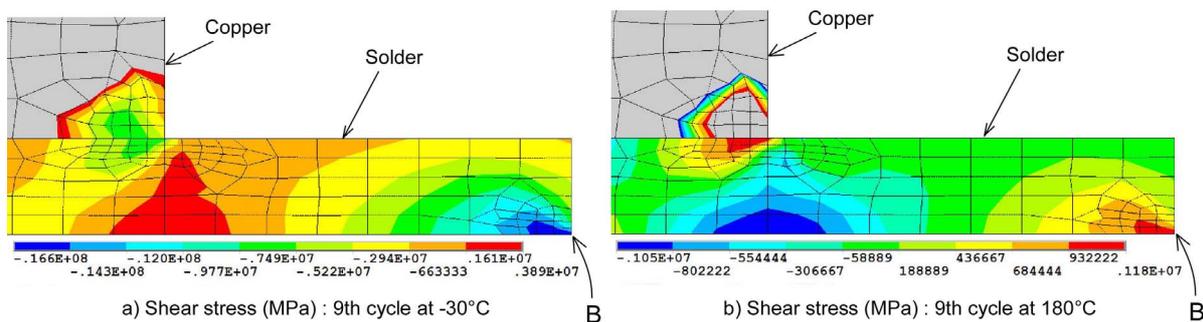


Figure 17: Zoom of shear stresses distribution in solder (point B region).

Conclusion

In this paper, it has been presented some results of thermal cycling tests applied to a test vehicle. Thermal cycling of high amplitude have been applied between -30°C and 180°C with high temperature variations about $8.5^{\circ}\text{C}/\text{mn}$. After only 100 cycles, microsection analyses have shown that ceramic cracks occurred and have lead to conchoidal fractures of the ceramic under the copper metalisation. This is due to the strain hardening of the copper layers which lead to increase stress levels in the ceramic at high temperature during the thermal cycling until its tensile strength. Furthermore, acoustic analyses have shown longitudinal cracks in the solder layer, which look like a fracture rather than a delamination.

Finite element modelisations have been performed in order to evaluate the stress and strain levels applied to the test vehicle during thermal cycling. The numerical results have allowed to understand the observed failures. In particular, the hardening behaviour of the copper metalisation which leads to the ceramic fracture has been shown. Further experimental and numerical investigations must be done in order to investigate the dwell time and the creep effect. The cyclic plastic work density has to be compared with the given value and should give some indications on the number of such temperature cycles the device assembly can undergo before failure. In an other way, in order to lower the stresses in the ceramic at high temperature values, near 200°C , and avoid the conchoidal cracks, dimples associated with DCB substrates or more adapted ceramic materials, such as Si_3N_4 or Direct Aluminum Bonding (DAB) will be fully investigated.

Acknowledgments

The authors acknowledge contribution from TRONICO company for the thermal passive cycling tests as well as STRUERS company who helped us to realise a microsection of the test module after thermal cycling in order to analysis the failure modes.

Bibliography

- [1]. W. Wondrack, "*Physical Limits and Lifetime Limitations of Semiconductor Devices at High Temperatures*", Microelectronics Reliability, June-July 1999, Vol. 39 (6-7), p. 1113-1120.
- [2]. P. McCluskey and al., "*Packaging of Power Electronics for High Temperature Applications*", Advancing Microelectronics, Jan./Feb. 1998, p. 19-24.
- [3]. L. Dupont and al., "*Characterisation of Silicon Carbide Schottky Diodes and COOLMOSTM Transistors at High Temperature*", in PESC conference, Aachen, 2004.
- [4]. X. W. Liu and W. J. Plumbridge, "*Thermomechanical Fatigue of Sn-37 wt.% Pb Model Solder Joints*", Materials Science and Engineering A, 5 December 2003 2003, Vol. 362 (1-2), p. 309-321.
- [5]. B. Y. Wu and Y. C. Chan, "*Electric Current Effect on Microstructure of Ball Grid Array Solder Joint*", Alloys and Compounds, 21 September 2005, Vol. 392, p. 237-246.
- [6]. G. Mitic, R. Beinert, and al., "*Reliability of AlN Substrates and their Solder Joints in IGBT Power Modules*", Microelectronics Reliability, 1999, Vol. 39, p. 1159-1164.
- [7]. Y. Nagatomo and T. Nagase, "*The Study of the "Power Modules with High Reliability for EV Use"*", in 17th EVS conference, Montreal, Oct. 2000.
- [8]. J. Schulz-Harder, "*Advantages and New Development of direct Bonded Copper Substrates*", Microelectronics Reliability, 2003, Vol. 43, p. 359-365.
- [9]. ANSYSTM, "*ANSYSTM 8.0*", Inc., Editor, 2002.
- [10]. L. Anand, "*Constitutive equations for hot-working of metals*", International Journal of plasticity, 1985, Vol. vol.1, p. 213-231.
- [11]. ANSYSTM, "*Rate-Dependent Plasticity* ", 2005, ANSYSTM theory Book.
- [12]. J. Wilde and al, "*Rate Dependent Constitutive Relations Based on Anand Model for 92.5Pb5Sn2.5Ag Solder*", IEEE transactions on Advanced Packaging, 2000, Vol. Vol.23 N° 3, p. 408-414.
- [13]. J. Shackelford and W. Alexander, "*The Crc Materials Science and Engineering Handbook*", CRC Press, 2000, Vol. Third Edition.