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Mounira Bouarroudj, Zoubir Khatir, Jean Pierre Ousten, Frédéric Badel, Laurent Dupont, et al.. Degradation behavior of 600V-200A IGBT modules under Power cycling and high temperature environment conditions. 18th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Oct 2007, BORDEAUX, France. pp. 1719-1724, 10.1016/j.microrel.2007.07.027 . hal-01702036

HAL Id: hal-01702036

<https://hal.science/hal-01702036>

Submitted on 6 Feb 2018

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Degradation behavior of 600V-200A IGBT modules under Power cycling and high temperature environment conditions

M. Bouarroudj^a, Z. Khatir^{a,*}, J.P. Ousten^a, F. Badel^a, L. Dupont^b, S. Lefebvre^b

^a INRETS-LTN, 2 Av. Malleret-Joinville, F94114, Arcueil cedex, France

^b SATIE ENS Cachan, CNAM, CNRS, UniverSud, 61 Av. du président Wilson F94235 Cachan cedex

Abstract

One challenge for automotive hybrid traction application is the use of high power IGBT modules that can withstand high ambient temperatures, from 90°C to 120°C, for reliability purpose. The paper presents ageing tests of 600V-200A IGBT modules subjected to power cycling with 60°C junction temperature swings at 90°C ambient temperature. Failure modes are described and obtained results on the module characteristics are detailed. Especially, physical degradations are described not only at the package level, like solder attach delaminations, but also at the chip level, with a shift on electrical characteristics such as threshold voltage. Finally, numerical investigations are performed in order to assess the thermal and thermo-mechanical constraints on silicon dies during power cycling and also to estimate the effect of ambient temperature on the mechanical stresses.

1. Introduction

The engine compartment of automobiles is a harsh environment for power electronic devices and the reliability goals are real challenges [1]. If no specific cooling circuit is used for power electronic devices, these ones should be cooled by the ICE (Internal Combustion Engine) circuit thermal management where coolant liquid is near 90°C and may reach 120°C. These high ambient temperatures are particularly penalizing for high power modules which they are driven towards their limits and also because they accelerate failure mechanisms [2,3]. In field operation, these ambient temperatures are combined with temperature variations due to devices self-heating (power cycling), which is the greatest challenge for reliability issues. Furthermore, devices are also subjected to very low frequency – high temperature

variations due to climatic conditions which can vary from -40°C to 80°C [4]. In these conditions, power devices are highly vulnerable to thermal fatigue.

Several papers have been published on the effect of power cycling on power devices [5-8], especially in the field of railway traction applications. Some research programs, such as HIMRATE (*High-temperature IGBT- and MOSFET-modules for railway traction and automotive electronics*), have produced some results about power cycling of high power modules in high temperature environment [9]. Actually, many researches are under progress in this area. It is the case of the EPO-Auto project, which is a French funded project where we are involved.

One of the main targets is to understand the failure mechanisms which take place on 600V power IGBT modules, both at package and chip levels, in such high

* Corresponding author. khatir@inrets.fr
Tel: +33 1 47 40 73 34; Fax: +33 1 45 47 56 06

temperature environments and applicative use.

2. Power cycling tests

For this purpose, power IGBT modules (600V-200A) have been tested in power cycling conditions and high ambient temperature. Test vehicles are six-pack IGBT power modules composed of three DBC alumina substrates as shown in the opened sample in figure 1. IGBT dies are of the third generation which maximum allowable junction temperature is 175°C even if module assembly remains limited to 125°C. IGBT dies were numbered as shown in the same figure. The tested packaging technology minimizes the number of bond wires by using them only for chip interconnections. Output terminals are directly bonded on the DCB substrates, gate and Kelvin connections are insured by spring contacts. Output terminals and springs were removed from the module shown in figure 1 for visibility reasons.

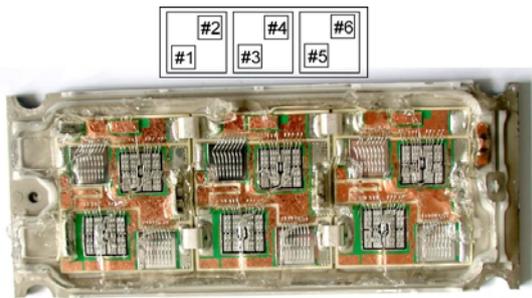


Fig.1: Tested devices: six-pack IGBT power modules (600V-200A)

Power cycling tests have been performed by subjecting the module to cyclic DC power injection with 15s power on and 30s power off. The total current injected in the whole three phase legs is 260 A. One difficulty was to estimate the current sharing between phases, but the junction temperature measurements have given relatively close results for all chips leading to considering a good current sharing. Assuming this assumption, power level (102W/chip) has been chosen in order to set the junction temperature variation (ΔT_j) to 60°C. This relatively long cycle is performed in order to activate assembly failure modes. Thermal environment is simulated with a vulcatherm system which delivers a glycol-water coolant thermally regulated at 90°C to the module heat-sink. Further tests will also be considered at 120°C. Several thermal and electrical parameters are monitored during the ageing tests. Especially, junction temperatures of all IGBT chips are measured by optical fiber thermal contact

sensors. Maximum junction temperatures are correlated by a thermo-sensitive parameter (V_{ce}) during off power phases at the end of power injection. Case temperature is measured, under each IGBT chips, with thermocouples. Figure 2 shows a partial sight of the power cycling test bench. One can see the power module mounted in its copper heat sink.

Several electrical and thermal parameters are monitored before and during ageing tests in order to understand failure mechanisms. Thermal parameters such as junction-to-case and junction-to-water thermal resistances (R_{thjc} , R_{thjw}) are measured. Some electrical parameters, such as threshold voltage of each IGBT chips (V_{ge}), forward voltage drop (V_{ce}) and collector leakage current (I_{ces}) are also recorded.

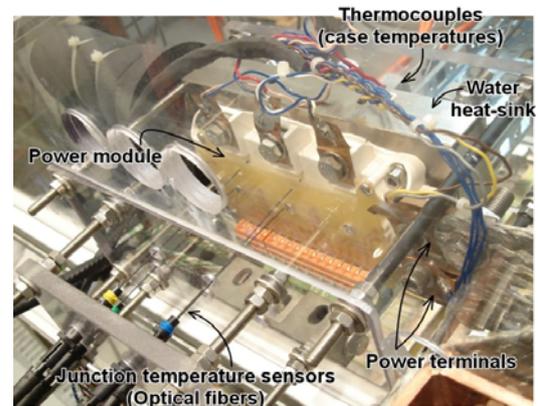


Fig.2: Power cycling test bench.

Figure 3 gives, for one chip and after 100 000 power cycles with 90°C water cooling heat-sink, a sample of the injected power cycles with the evolution of corresponding junction temperature of chip#3 and case temperature under same chip.

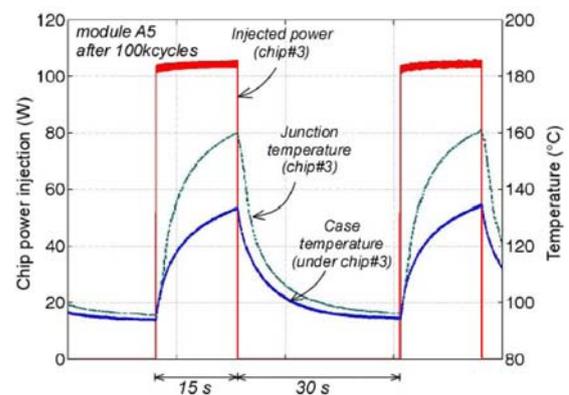


Fig.3: Power cycles with junction and case temperatures.

As we can see, junction temperature swings between 97°C and 160°C whereas case temperature varies between 95°C and 135°C.

3. Power cycling results

Results given in the following section concern two identical tested power modules, named A5 and B3. The two modules were tested in same conditions (given in the previous section). In order to understand failure mechanisms, we need to analyse the modules at the beginning of the degradation process (at early stage). So, we fixed the lowest possible failure criteria on the monitored failure indicators. Tests on module A5 were stopped when the junction to water thermal resistance (R_{thjw}) had reached an increase of only 10% of the initial value, i.e. after 100 000 power cycles (Fig.4). Module B3 was stopped after only 54 000 power cycles and only MEB visualizations of its chip surfaces are given hereafter.

Concerning module A5, after ageing we have not observed any significant variation of the junction-to-case thermal resistances (R_{thjc} , not shown in the figure) and no variation of collector voltage (V_{ce}) as well (see figure 4). This figure gives only parameter variations of chip#3 but all chips exhibit the same behaviors with quite the same values. The fact that R_{thjw} increases whereas R_{thjc} does not is due to permanent spreading out of the thermal grease. This has been observed by visual inspection after disassembling the module from the heat-sink.

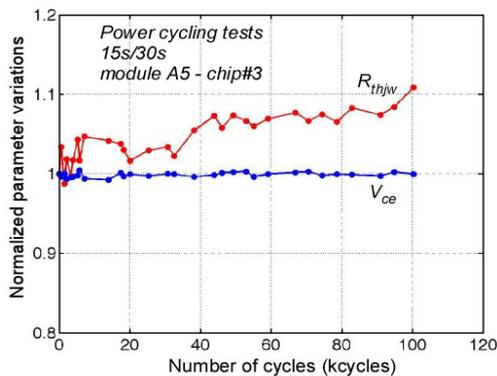


Fig.4: Evolution of normalized values of junction to water thermal resistance and collector voltage (module A5).

In spite that no significant variation of R_{thjc} was observed, scanning acoustic microscopy (SAM) analyses have shown a beginning of delamination process of the solder attach at some DCB corners and crack initiations in other ones (Fig.5). IGBT chips

location in the DCB substrate (Fig.1) and the reached delamination level do not allow to significantly affect the junction-to-case thermal resistance and no variation of this parameter is detectable. Concerning die attaches, no degradation was observed by SAM analyses.

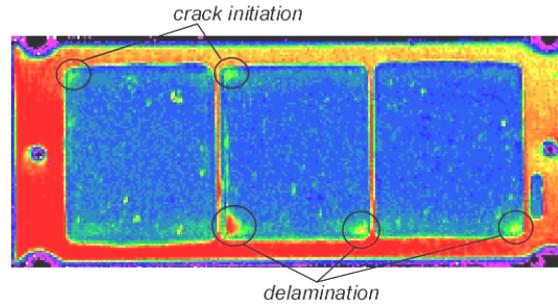


Fig.5: Solder degradation after 100 kcycles (module A5).

These harsh test conditions have not only affected the package level but also the chip level. Threshold voltages (V_{gth}) of all IGBT chips have been modified by the power cycling at these high ambient and junction temperature conditions. Figure 6 shows threshold voltages versus temperature for each IGBT chips of the module, at the initial state and after power cycling. We can observe a light increase of about 300mV of the threshold voltage whatever the junction temperature. These results clearly point out a degradation of the gate oxide characteristics.

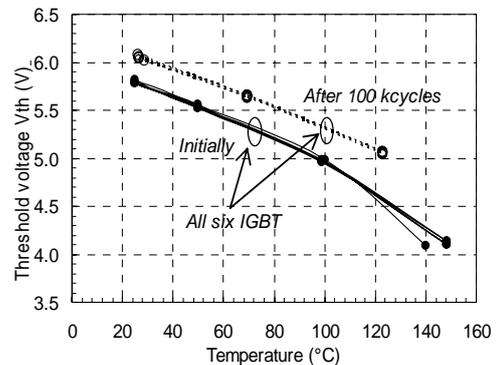


Fig.6: Threshold voltage degradation (module A5).

Such a behavior is usually observed in micro-electronics devices which have thin oxide layers. In these devices, this degradation may be explained by hot carrier mechanisms which increase interface trapped charges between semiconductor and silicon oxide. In our case, oxide layers of trench gate IGBTs are thicker (about 150nm). So, could temperature

environment and high collector current level contribute to such mechanism? These results must be confirmed in more tested devices and further investigations, including C(V) measurements, are in progress in order to understand this parameter shift.

Concerning module B3, surface of IGBT chips were inspected by optical and electronic microscopy (MEB) and compared with a non aged device. As a result, some bond wires of the aged module exhibit heel crack initiation (Fig.7). This failure mechanism is due to thermo-mechanical effect [10]: the wire, subjected to temperature cycles, expands and contracts leading to mechanical fatigue at the knee of the bond wire. As explained in [10], this failure mechanism rarely occurs in modern IGBT multichip modules and has been observed only once in our laboratory after power cycling tests of high IGBT power modules for railway application.

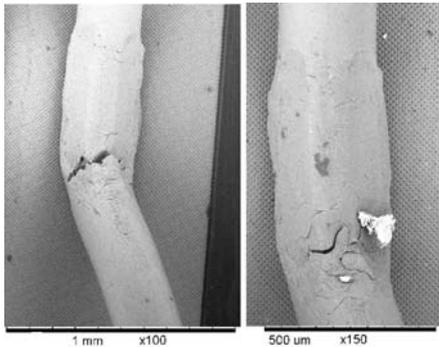


Fig.7: Heel crack initiation (module B3).

In order to explain such observations, we must recall some basic technology details and tests conditions. As said before, tests conditions in these 600V-200A power modules are imposed in order to reach $\Delta T_j=60^\circ\text{C}$ ($T_{j\text{min}}=95^\circ\text{C}$, $T_{j\text{max}}=155^\circ\text{C}$) and bond wires (Al $\varnothing 300\mu\text{m}$) are surrounded only by gel, no coating layer is used. Usual power modules tested in our laboratory are dedicated to railway traction application with higher current levels and thicker wire diameter ($\varnothing 400\mu\text{m}$). The maximum accelerated power cycling tests conditions for these devices are temperature swings about $\Delta T_j=80^\circ\text{C}$ at relatively low ambient temperature ($T_{j\text{min}}=40^\circ\text{C}$, $T_{j\text{max}}=120^\circ\text{C}$). Moreover, all railway modules are made with coating layer in the chip surface. So, despite lower temperature swings ($\Delta T_j=60^\circ\text{C}$) instead of 80°C , heel crack initiation was only observed in the presented tests. If we assume that bonding process are nowadays quite well optimized, this mechanism could be due to the higher temperature environment which can accelerate

the mechanism, or less probably to the lack of coating layer. These observations must be confirmed and further investigations will be done in order to understand these results.

An other usual observation has been made at the chip surface, it is the degradation of the chip metallization [10] due to visco-plastic behavior of aluminium grains during temperature cycling (Fig.8).

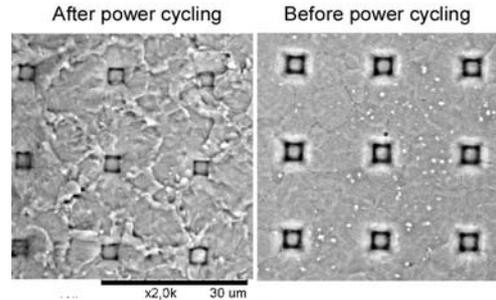


Fig.8: Chip metallization degradation (module B3).

4. Numerical estimation of chip stresses

In order to assess the thermo-mechanical constraints that IGBT chips have undergone during power cycling tests, 3D thermal and thermo-mechanical simulations (with ANSYS) have been carried out. So, the power module assembly and its heat-sink (figs.1 and 2) have been modeled. Some material data are given in table 1. Concerning, mechanical properties, DCB ceramic is considered as linear, copper metallization is considered non-linear material (elasto-plastic) and solder is considered visco-plastic (Anand model [11]). Moreover, the following simulation results take into account the module assembly initial stresses due to the solder process.

Materials	Thermal cond. (W/m.K)	CTE (10^{-6}K^{-1})	Specific heat (J/Kg.K)	Young modulus (GPa)	Mechanical properties
Si	150	2.6	700	170	elastic
Cu	400	16	400	130	plastic
Al_2O_3	30	6.8	780	270	elastic
Solder	50.6	24.7	180	60	Anand [11]

Table 1: Material parameters.

The experimental power cycling conditions were applied to the model: a thermal flux (102W) was injected in the active area of each IGBT chip (0.83cm^2) during 15s followed by 30s cooling phase. Ambient temperature was fixed at 90°C as a boundary condition at the bottom surface of the heat-sink (copper material).

As a result, the temperature evolution during a

complete cycle for a point near the location of maximum value at the chip surface is given in Fig.9. At the end of power injection phase, temperature reaches 153°C. At this time, we can see the temperature map within a DCB substrate in Fig.10 which shows a high coupling effect between dies.

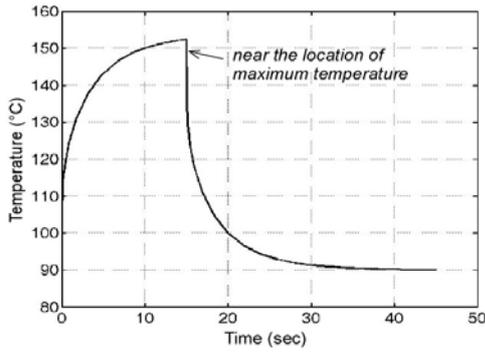


Fig.9: Temperature swing near the location of maximum value in IGBT surface.

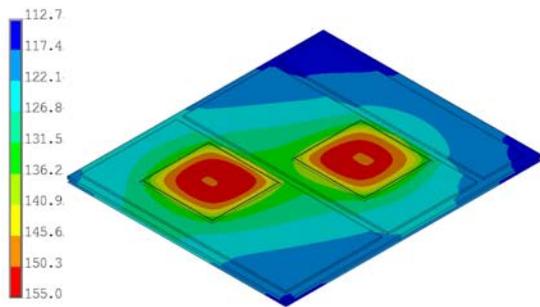


Fig.10: Temperature swing near the location of maximum value in IGBT surface.

Temperature distribution on the hottest chip along a path through the centre is drawn in Fig.11. The temperature hollow at the center corresponds to the gate pad. Clearly, the use of small IGBT³ chips in trench gate technology leads to high power density and consequently to very high spatial gradient of about 12°C/mm locally at the chip periphery. The calculated temperature swing of the hottest point of the chip is about $\Delta T_{jmax} = 64^\circ\text{C}$ whereas at the periphery it is about $\Delta T_{jper} = 49^\circ\text{C}$. So, there are high thermal constraints on the silicon chips and their constitutive materials.

The initial soldering process of the chip on the DCB substrate makes the chip to remain in a compressive stress state. Even in power cycling conditions at 90°C ambient temperature, the chips remain in a compressive stress state. This is shown in the stress map of Fig.12 which gives principal stress

σ_3 . The center of the chip is the most compressed area with stress values around 109 Mpa at the end of the power injection when temperature map is that of Fig.10. From this figure, it is clear that such compressive stresses are more crucial at low temperature, when power cycling are performed at low ambient temperature values. For comparative purpose, we have performed the same simulations at -40°C ambient temperature. Temperature results are not shown here but temperature maps in the assembly are similar than that for 90°C ambient, values are only shifted with a value of 130°C (from 90°C to -40°C). For example, maximum junction temperature reached at the end of power injection is around 25°C whereas it was 155°C for 90°C ambient. The reason is that we made the assumption that thermal material properties are not temperature dependant. In these conditions, temperature gradients are naturally the same.

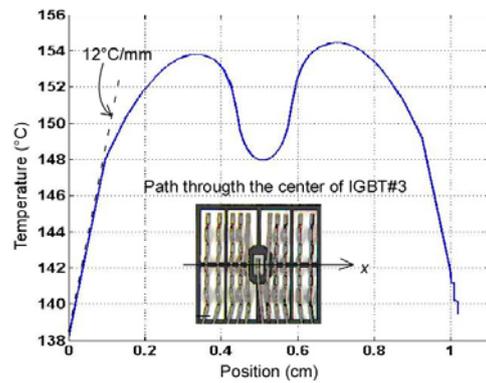


Fig.11: Temperature along a path on IGBT die.

Nevertheless, for these low temperature values, the principal stress σ_3 map in the IGBT surface at the end of power injection is significantly higher (Fig.13). The IGBT chip is considerably compressed and this last figure gives an estimation of the stress undergone by the chip at its center which is about 460 Mpa. The principal stress distribution along a path through the centre of the chip is given in Fig.14 at the end of the same injected power and for both 90°C and -40°C ambient temperature.

This last figure clearly shows the higher stress values and higher stress gradients for the low level ambient temperature case making the use of semiconductor dies mounted in DCB substrates more risky. Some authors have already shown effects of mechanical stress on IGBT characteristics [12], but obtained results show that we must certainly take into account the repetition of these severe mechanical

constraints on the chips to correctly understand degradation of chip characteristics.

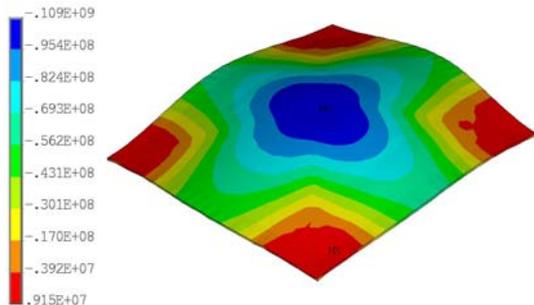


Fig.12: Principal stress (σ_3) in IGBT surface (MPa) (at end of power injection $T_{jmax} = 155^\circ\text{C}$ at $T_{amb} = 90^\circ\text{C}$).

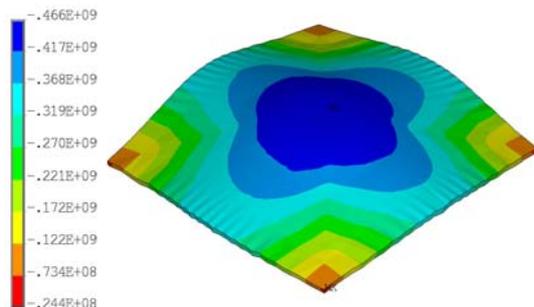


Fig.13: Principal stress (σ_3) in IGBT surface (MPa) (at end of power injection $T_{jmax} = 25^\circ\text{C}$ at $T_{amb} = -40^\circ\text{C}$).

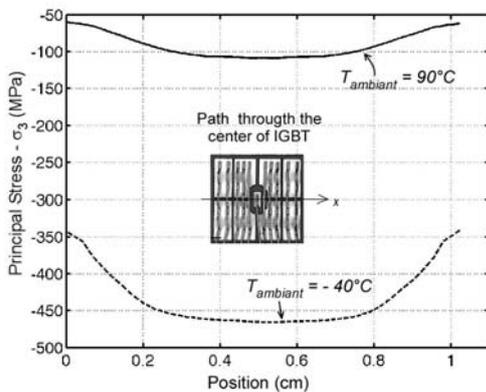


Fig.14: Principal stress (σ_3) along the path of an IGBT die surface (for high and low ambient temperature).

4. Conclusion

In order to understand failure mechanisms of power devices which can occur in automotive traction applications, power cycling tests have been conducted on 600V-200A power IGBT modules. First results of device degradation due to high ambient temperature of

90°C combined with 60°C ΔT_j are given and analyzed. Especially, gate threshold voltage shift, solder cracks as well as bond wire hell-crack initiation have been reported. Finally, assessment of mechanical constraints in IGBT chips, during power cycling, have been performed by means of thermal and thermo-mechanical simulations. It has been shown that chips are subjected to very high compressive stresses especially at low temperature levels.

Acknowledgements

This work is part of the EPO-Auto project funded by the French research program ANR-PREDIT.

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