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Accelerated Active Ageing Test on SiC JFETs Power Module with Silver Joining Technology for High Temperature Application

L. Dupont^{a*}, G. Coquery^a, K. Kriegel^b, A. Melkonyan^b

^a *LTN INRETS, INRETS, 25 allée des Marronniers – Satory - 78000 Versailles, France*

^b *SIEMENS Corporate Technology, Otto-Hahn-Ring 6, D-81739 Munich, Deutschland*

Abstract

This paper presents the accelerated active power cycling test (APCT) results on SiC JFETs power module dedicated to operate at high temperature. This study partly focuses on the new chip joining technology (LTJT), which permit to use SiC JFETs transistors at higher temperatures. We present the different die attachments tested with high temperature lead solder and silver sintering joining technologies. Active power cycling results for high junction temperature $T_{jmax}=175^{\circ}\text{C}$ with $\Delta T_j=80^{\circ}\text{K}$ to perform an evaluation of main damages during active test are carried out and a comparison between lead and silver chip joining technologies is presented.

1. Introduction

The ability of SiC devices to be used in high temperature environment has been demonstrated since few years [1-2], but the high level of power density and the high temperature calls for finding a technical solution, which is able to validate the life time duration and reliability performances in harsh conditions [3,5]. The objectives of this paper are to investigate the power cycling capability of the SiC JFETs power module assembly dedicated to operate at high temperature. In these terms, we have chosen to focus this paper on the evaluation of king damage during active power injection and a comparison between lead solder and silver sintering chip joining technologies. The work deals with power modules developed by SIEMENS in order to perform active power cycling test at high temperatures.

2. Presentation of the JFET power modules

SIEMENS Corporate Technology had developed power modules with a lead solder solution as well as with silver sintered joining technology in order to compare high temperature chip assembly. Power modules are designed in an ECONO³ package with a Copper-Molybdenum base plate in order to minimize the stresses in the base plate solder (Fig. 1).

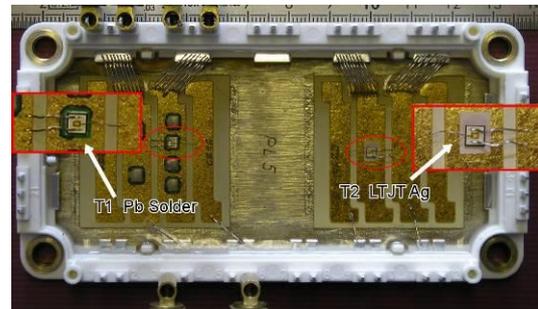


Fig. 1: Presentation of SIEMENS JFET power module.

* Corresponding author: laurent.dupont@inrets.fr
Tel: +33 (0) 1 30 84 39 84; Fax: +33 (0) 1 30 84 40 00

All modules include two JFETs transistors (1200V-6A) each of which is placed on a specific AMB ceramic substrate for thermal expansion coefficient adaptation. Each substrate has been soldered onto the base plate with a high temperature solder alloy.

In order to simplify the thermal resistance evaluation, two holes are realized in the base plate close to each JFET chip axis in order to acquire the case temperature with a type K thermocouple (Fig. 2).

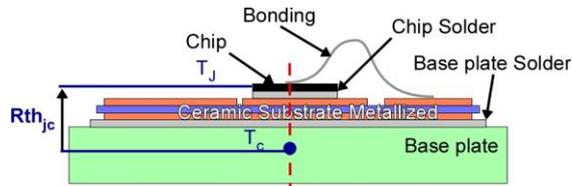


Fig. 2: Presentation of the module assembly.

The Table 1 presents the modules configurations which have been used in order to validate the test bench and perform active power cycling tests. The electrical and thermal decoupling of both JFETs in each power module helps to optimize the ageing test conditions. Nevertheless, the variation of some geometric parameters of the both solders induced some deviation of electro-thermal conditions.

Table 1: Details of tests vehicles configurations.

Module	Substrate	Chip Solder	Use
PL02	T1-CZ18	Lead Solder	Ageing test
	T2-CZ19	Lead Solder	
PL03	T1-CZ11	Silver sintered	Ageing test
	T2-CZ12	Silver sintered	
PL05	T1-CZ14	Silver sintered	Bench Calibration
	T2-CZ16	Lead Solder	

3. Description of the power cycling test bench

The active power cycling test bench is presented in the next figure (Fig. 3). Only cooling temperature, the duration of the power injection cycle and the injected current value are fixed at the beginning of the test in order to adjust the junction temperature variation. In these conditions the power injection is free versus junction temperature evolution. The threshold ageing criteria are arbitrary fixed as $V_{DS}+5\%$, $R_{thjc}+20\%$ and $T_{jmax}+10\%$ to perform future comparisons with conventional technologies previously tested [REF?]. Some thermal and electrical parameters are controlled continuously during the test for safety reasons for long time using.

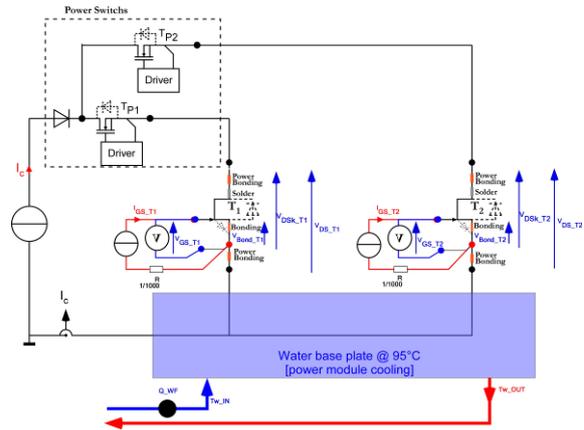


Fig. 3: Active Power Cycling Test Bench.

The figure 4 presents the long time recording during one power injection cycle. We can see the two square current injections (I_c) for the both JFETs transistors and electro-thermal parameters recording for T1 transistor. The power injection conditions are defined for each JFET with $T_{ON}=15s$ and $T_{OFF}=30s$ while keeping the thermal stress of chip solder close to the steady state electro thermal conditions (Fig. 4).

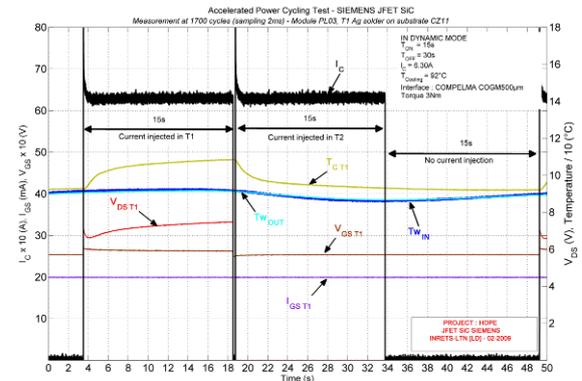


Fig. 4: Long time recording during cycle period (45s).

Electrical and thermal parameters, which are used for the ageing evaluation, are periodically recorded during the test as described in the chronogram presented in the Fig 5. Due to the thermal oscillation of the cooling circuit (Fig. 4 T_{W_IN} T_{W_OUT}), a median calculation of ageing parameters is realized for 15 successive cycles in order to limit the thermal effect on the recordings.

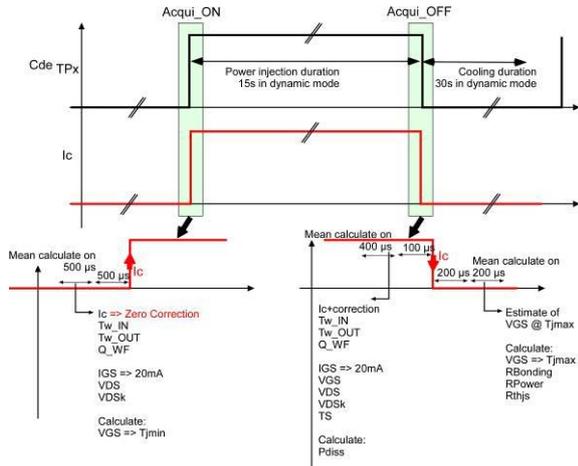


Fig. 5: Acquisitions during one power injection cycle.

In this study, the junction temperature is estimated with a low gate current injection (20mA) through the gate to source diode of each JFET after 200 μ s after the end of power injection (Fig. 5). A calibration campaign has been done for all tested components in the both laboratories (SIEMENS, INRETS) to validate the analytical function between V_{GS} drop voltage for 20mA gate current injection and junction temperature (Fig. 6).

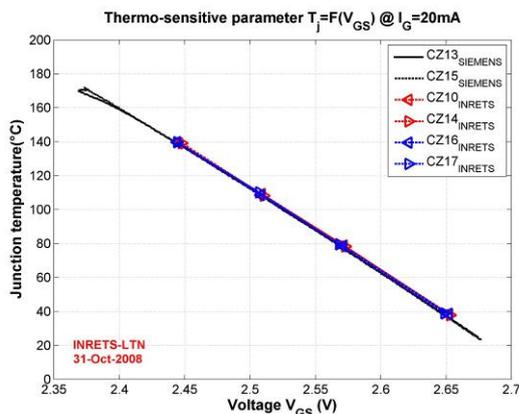


Fig. 6: Electro-thermal characterization $T_j = F(V_{GS})$.

Due to the large range of junction temperature excursion, the junction temperature is estimated during the tests with a polynomial relation in order to take into account the non linear evolution of the V_{GS} drop voltage. In contrast to the junction indirect estimation of IGBT or diode, the high drop voltage level of V_{GS} thermo sensible parameter forces to use a high accuracy measurement system in order to perform a good evaluation of the thermal resistance.

The independency of electrical and thermal performances for the both JFETs in each power modules helps us to optimize the ageing test

conditions. Nevertheless, some geometric parameters variations of the solders induced some variations of electro-thermal conditions.

The test bench has been developed for high temperature (up to 250°C of T_j) and large junction temperature excursion (ΔT_j over 110°C). For example, the figure 7 presents a high speed recording of electrical and thermal parameters at the end of the power injection for PL02 T2 transistor with a junction temperature estimated around 230°C.

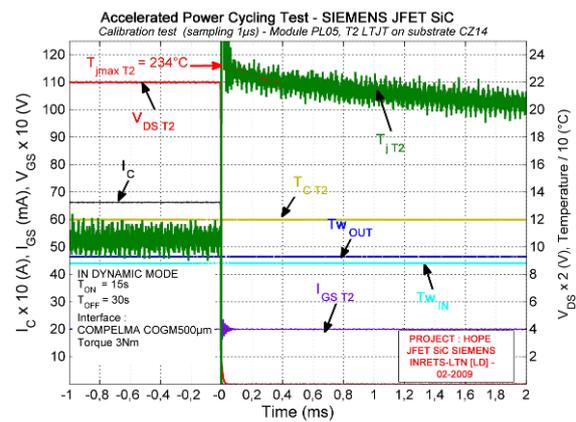


Fig. 7: Principe Active Power Cycling Test Bench.

The test bench calibration methodology over 200°C for the maximum junction temperature is defined in order to qualify other parameters like the thermal resistance evaluation versus junction temperature.

As we can see in the next figure (Fig. 8) the thermal resistance from junction to case of the silver solution is less sensitive to high temperature as lead solder solution.

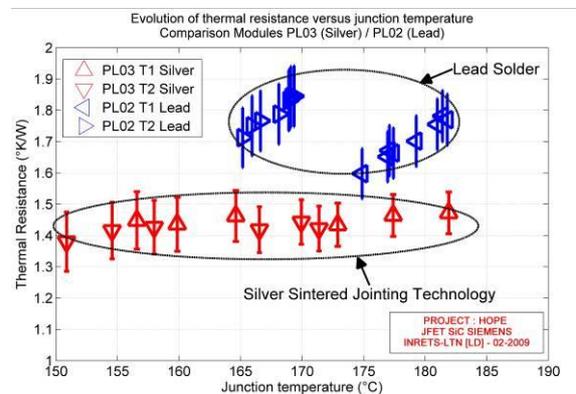


Fig. 8: R_{thjc} evaluation versus junction temperature.

In fact, the modifications of materials thermal properties of the copper and lead solder presents a thermal conductance dependency with the temperature,

especially where the using temperature is closer to the liquidous temperature (293°C / 500°C Ag nano). The differences between T1 and T2 transistors for the both technologies are due to the variations of the chip joining geometries and the variation of the thermocouples locations in the base plate.

During these calibrations in dynamic mode we can evaluate the electrical and thermal parameters of JFET assembly versus current injection level and cooling conditions. As we can see in the figures Fig.9 and Fig.10 the drop voltage evolution combined with the junction temperature induced a high sensibility with the injected current level, specifically for the lead solder joining technology. In these conditions it will be very difficult to use JFET transistors in high current density conditions with a conventional assembly [4, 5].

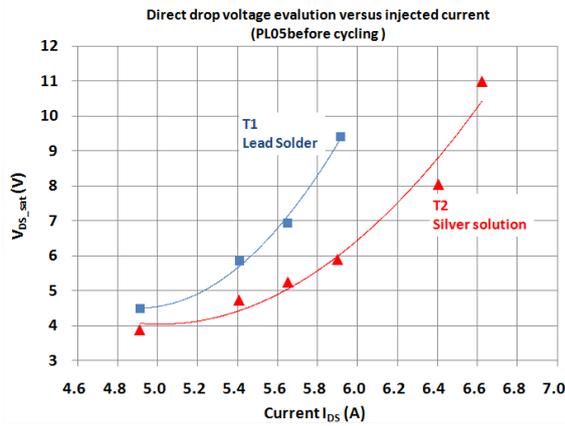


Fig. 9: $V_{DS\ sat}$ evolution versus injected current.

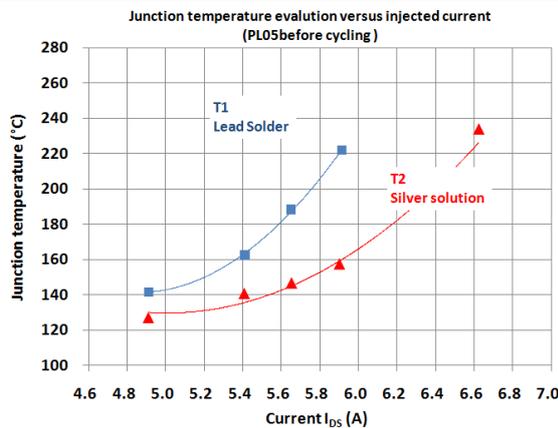


Fig. 10: T_{jmax} evolution versus injected current.

The active power cycling tests were conducted to limit the time duration of the tests with an adjustment of power injection level with respect to electrical capability of JFETs transistors. Nevertheless, the strong dependency of the JFET voltage drop with

current density leads to V_{DS} corrections versus current level and junction temperature as presented in the figure Fig.11 for the PL03 module (silver joining technology).

During the ageing tests, a correction of the $V_{DS\ sat}$ voltage is realized in order to control its evolution for a constant current value and for a specific junction temperature (175°C). So a calibration of the dependency between voltage drop ($V_{DS\ sat}$), current and the junction temperature has been performed to define the correction coefficients. These corrections help us to observe the degradation of the electrical connection without junction temperature effect induced by thermal resistance degradation during the active power cycling tests.

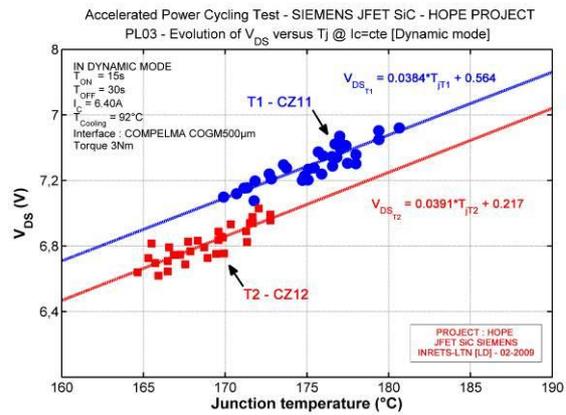


Fig. 11: $V_{DS\ sat}$ correction versus junction temperature.

4. Power cycling test results

Before the description of the active power cycling results, some specifications have to be presented. The accelerated active power cycling test induces extreme conditions for the JFET chip and the assembly:

- Power density: > 1000 W/cm² (Over ten times as Si IGBT active power cycling test)
- Current density: > 150A/cm² (Over three times as Si IGBT active power cycling test)

In order to compare lead solder and silver sintered joining technology for the small chip assembly dedicated to high temperature, the same active power cycling conditions are defined for the both technologies in terms of junction temperature variation between 95°C to 175°C (Fig. 4.1). Due to the thermal resistance differences between two technologies, we have adjusted the current level and the cooling temperature in order to keep the same cycling time duration.

- **PL02 module ageing test (lead solder):**

$I_C=5.86A$, $T_{Cooling}=95^{\circ}C$

$T_{jmax}=175^{\circ}C$, $\Delta T_j=80^{\circ}K$

$T_{ON}=15s$, $T_{OFF}=45s$

As shown in the figures (Fig.12a b), we can observe the increasing of the thermal resistance and the $V_{DS\ sat}$ after correction, especially for the T1 transistor, which have the higher junction temperature level. The first degradation criterion has been detected for T1 after 43000 cycles ($V_{DS\ sat}$ corrected +5%) and a second criterion on T1 again ($T_{jmax} +10\%$) has conducted to stop the test after 55000 cycles still being below the failure criteria I.

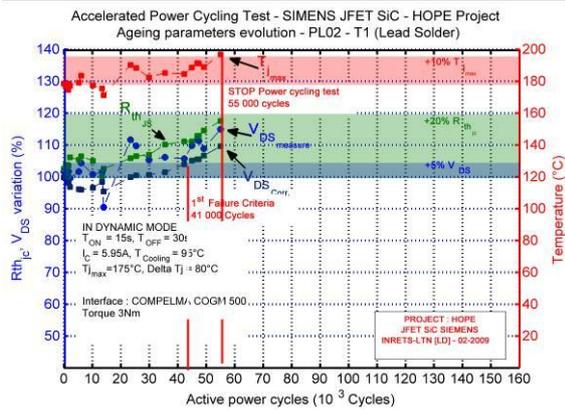


Fig. 12a: Evolution of PL02 T1 ageing parameters.

Even if the T2 ageing parameters have been increased during the test, no degradation criterion has been reached for this transistor (Fig. 12b).

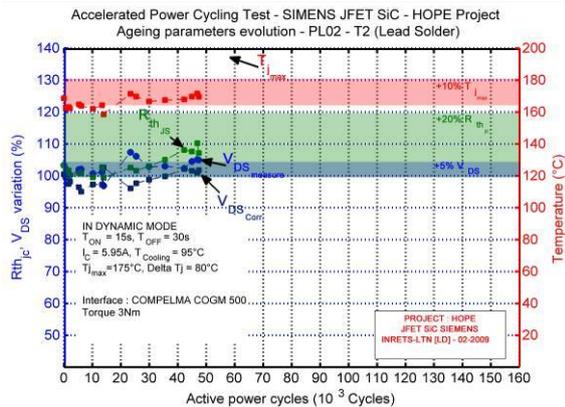


Fig. 12b: Evolution of PL02 T2 ageing parameters.

In correlation with these APCT results, some analysis confirm the solder degradation with some gas inclusions and a new damage aspect observed for T1 lead solder which is not a conventional delamination mechanism. At this time we perform new analyses in order to have a better understanding of this degradation

mechanism, which occurs at high temperature and high current density (electro-thermal migration?).

For the T2 lead solder transistor we can observe a delamination of the solder located close to the thermocouple drilling with some voids, which can correlate with the thermal resistance increase.

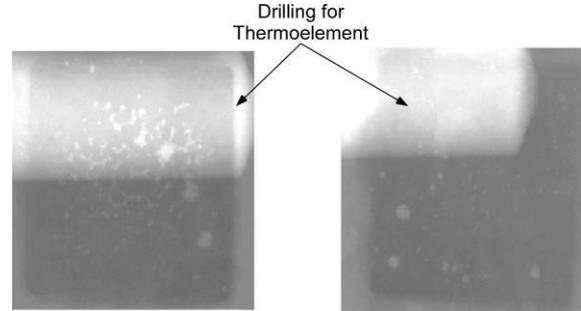


Fig. 13: PL02 X-ray analyses of the lead chip solders.

For the VDS increasing, optical analyses show a degradation of the chip metallization, especially for T1 transistor, where we cannot identify the elementary cells due to a large aluminum reconstruction (Fig. 14).

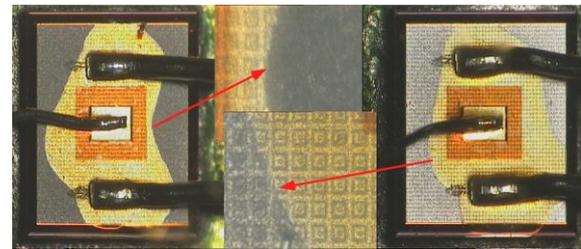


Fig. 14: Optical analyses of the chip metallizations.

On another hand, no wire-bonding degradation has been observed (Fig. 15).

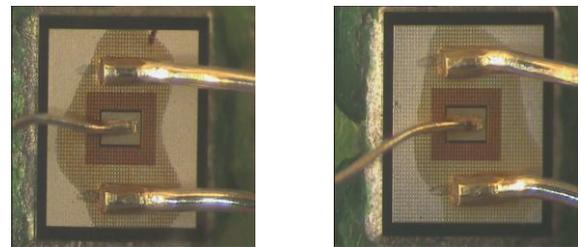


Fig. 15: Optical analyses of the wires bonding.

• **PL03 module ageing test (silver-sintering solution):**

$I_C=6.4A$, $T_{Cooling}=92^{\circ}C$
 $T_{jmax}=175^{\circ}C$, $\Delta T_j=80^{\circ}K$
 $T_{ON}=15s$, $T_{OFF}=45s$

In order to perform ageing test under the same conditions as for the lead soldered modules, we have adjusted the cooling temperature and injected current (<10%). Under these conditions, we can see in the figure 15 (a b) the ageing parameters evolution during the test. The last measurements show a reduction of the junction temperature due to a current limitation of the power supply for high ambient temperature (30°C). This APCT of silver joining technology module have been stopped after 155000 cycles due to a VDS increasing over the 5% criterion for T1 transistor (Fig. 15a) like PL02 module (Fig. 12a).

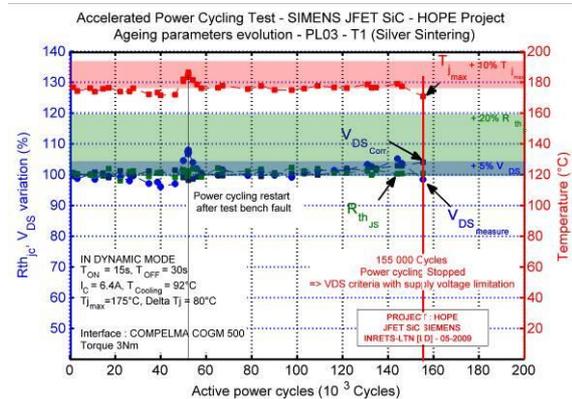


Fig. 15a: Evolution of PL03 T1 ageing parameters.

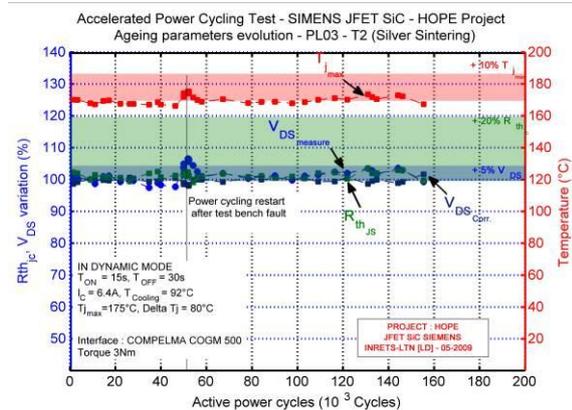


Fig. 15b: Evolution of PL03 T2 ageing parameters.

At this moment, we don't have the analysis results in order to identify the damages which could help us to perform the correlations with ageing parameters evolution previously presented (Fig.15a). Nevertheless, we can observe metallization damages for the T1 transistor.

5. Conclusion

The APCTs show interesting effects which were not expected:

- The silver sintering joining technology is much more stable and reliable than the high lead solder where we can observe a new degradation mode.
- This is documented by the continuous increase of the thermal resistivity in the case of the high lead solder. As a consequence the failure criteria for the thermal resistance is already reached at 43000 cycles, whereas in silver sintering case the first damage criterion for V_{DS} has been reached after more than 155000 cycles and with thermal resistivity remains constant.

The quality and reliability for the Al thick wire bonding corresponds to the state of the art of Si die bonding although bonding parameters and metallization technology have to be adapted to SiC devices.

Acknowledgements

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