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To cite this version:

T. Pham, A. Maréchal, P. Muret, D. Eon, E. Gheeraert, et al.. Comprehensive electrical analysis of metal/Al 2 O 3 /O-terminated diamond capacitance. Journal of Applied Physics, 2018, 123 (16), pp.161523. 10.1063/1.4996114 . hal-01701727

HAL Id: hal-01701727

https://hal.science/hal-01701727

Submitted on 13 Jul 2021

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Comprehensive electrical analysis of metal/Al_2O_3/O-terminated diamond capacitance

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(Dated: June 2017)

Metal oxide semiconductor capacitors were fabricated using $p-$type oxygen-terminated (001) diamond and Al_2O_3 deposited by atomic layer deposition at two different temperatures 250°C and 380°C. Current voltage I(V), capacitance voltage C(V) and capacitance frequency C(f) measurements were performed and analyzed for frequencies ranging from 1 Hz to 1 MHz and temperatures from 160 K to 360 K. A complete model for the MOSCAPs electrostatics, leakage current mechanisms through the oxide into the semiconductor and small *a.c.* signal equivalent circuit of the device is proposed and discussed. Interface states densities are then evaluated in the range of $10^{12} eV^{-1}.cm^{-2}$. The strong Fermi level pinning is demonstrated to be induced by the combined effects of the leakage current through the oxide and the presence of diamond/oxide interface states.

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I. INTRODUCTION

Diamond has been widely recognized as an ideal semiconductor for power devices[1,2] due to its superior physical properties. Recent progresses on diamond substrate, homoepitaxial growth, doping control and fabrication processing permit to consider the diamond power devices, e.g. Metal Oxide Semiconductor Field Effect Transistors (MOSFET). Most of the diamond MOSFET[3–5] reported in the literature were realized thanks to the two dimensional hole gas (2DHG) at the hydrogen terminated diamond (H-diamond) surface due to surface doping concept[6]. Performances of H-diamond MOSFETs are promising[4] and optimizations of the structures are still under investigations[5,7,8]. Recently, the first MOSFET transistor working in inversion regime has been reported[9]. In order to obtain such carrier inversion, $n-$type oxygen-terminated (O-terminated) (111) diamond epilayer has been used as substrate material in order to create a $p-$type channel MOSFET. These two MOSFETs architectures are opening the route for the fabrication of the next generation of diamond based MOSFETs for power electronics. However, a deep understanding of the oxide and interface properties of the gate transistor is still missing. In this work, we report an exhaustive analysis of metal oxide semiconductor capacitor (MOSCAP) fabricated on O-terminated diamond.

In order to examine the effectiveness of the gate control boron doped diamond, Chicot et al.[10] introduced the O-diamond/Al_2O_3 MOSCAPs test device. Strong leakage currents[10] and capacitance frequency dependence[11] were observed through the O-diamond MOSCAPs for Al_2O_3 deposited by ALD at 100°C. Kovi et al.[12] employed an identical structure using Al_2O_3 deposited by ALD at 250°C and reported similar electrical characteristics. Marechal et al.[13] employed the XPS measurements and determined the type I band alignment at O-diamond/Al_2O_3 interface with Al_2O_3 deposited by ALD at 250°C. However, in all mentioned reports, a complete understanding of the electrical characteristics of boron doped O-diamond/Al_2O_3 MOSCAPs was still lacking.

This work is devoted to investigate the diamond/Al_2O_3 interface and the origin of gate leakage current and capacitance-frequency dependence for O-diamond MOSCAP. In the first section, we briefly introduce the fabrication processes and the general electrical characteristic of the O-diamond MOSCAPs to illustrate the main issues. In the second section, we address the electrostatic properties of the O-diamond MOSCAPs and introduce an approach

to reliably perform the C(V) measurements and a method to quantify the semiconductor surface potential versus gate bias ($\Psi_S(V_G)$). Electrical charges properties such as semiconductor doping concentration, oxide charges and interface state charges are then quantified from C(V) measurements. The electrostatic band diagrams are built by taking into account the charge components of the MOSCAP test device. Electrostatics simulations are compared with experimental results $\Psi_S(V_G)$. In the third section, we propose a model for the leakage current mechanism under negative bias thanks to the electrostatics band diagram. From leakage current mechanism, we build the linearized equivalent circuit that complies with small signal measurements of the physical model. Approximated equivalent circuit based on different limiting processes is discussed. Current limiting process is identified thanks to different approaches. From the approximated equivalent circuit, the conductance method is adapted to our specific MOSCAPs and applied to quantify interface states density D_{it}. The impedance/admittance frequency dependence of the MOSCAP test device is empirically simulated by using the proposed equivalent circuit with all parameters extracted from experimental analysis. Finally, the paper is summarized.

II. MOSCAP FABRICATION AND TYPICAL ELECTRICAL CHARACTERISTICS

This section is dedicated to the description of the MOSCAPs fabrication process. Then, the typical I(V), C(V) and C(f) measurements done on these MOSCAPs will be illustrated and discussed.

A. Experimental details

The test devices composed of a stack of a heavily (p+ layer) and a lightly (p− layer) boron-doped homoepitaxial mono-crystalline diamond layer grown by using a microwave plasma assisted chemical vapor deposition (MPCVD) NIRIM type reactor on a 3×3 mm^2 Ib high pressure high temperature (HPHT) (001) diamond substrate. The cross-section structure is shown in Fig. 1 a). The optical plan view structure of one fabricated test device is shown in Fig 1b. The moderately boron-doped diamond layer ($N_A \simeq 3 \times 10^{17}$ cm^{-3}) is in contact with the gate oxide. The heavily boron doped ($N_A \simeq 5 \times 10^{20}$ cm^{-3}) metallic

diamond p+ layer acts as a low resistive ohmic contact electrode in order to reduce the series resistance. Vacuum ultraviolet (VUV) ozone treatment resulted in the Oxygen termination of the diamond surface[14]. The Al_2O_3 gate oxide was deposited by atomic layer deposition (ALD) on the whole sample surface using a Savannah 100 deposition system from Cambridge NanoTech. The precursor was Trimethylaluminium (TMA), and water was used as the oxidant. The pulse and exposure duration were 15 ms and 30 s, respectively, with typical base pressure of 1.3× 10^{-1}Torr. The ohmic contacts and gate contacts were defined by laser lithography (Heidelberg DWL66FS) and electron beam (ebeam) evaporation of Ti/Pt/Au (30/50/40 nm) followed by standard lift-off technique. The ohmic contact was deposited directly on p^+ layer prior to Al_2O_3 deposition. This structure offers the advantage of having both MIMCAPs and MOSCAPs on the same sample, as shown in Fig. 1a). The details of two representative samples are presented in table I. These two samples are chosen as their electrical characteristics are mostly similar in term of leakage current density, capacitance-voltage and capacitance-frequency behaviors. The only difference is the shift of flatband voltage due to charge in the gate oxide, as it will be discussed in the following sections.

Sample	t_{p^-} (nm)	t_{p^+} (nm)	t_{ox} (nm)	O-termination	T_{dep} of ALD (°C)	$T_{annealing}$ (°C)
#1	600	300	20	VUV	250	NA
#2	300	300	20	VUV	380	500

TABLE I. Sample structures details: thickness of moderately doped layer t_{p^-}, heavily doped layer t_{p^+}, oxide layer deposited by ALD t_{ox}, treatment for oxygen termination (VUV ozone treatment is defined as VUV), ALD deposition temperature T_{dep} and annealing temperature $T_{annealing}$.

The DC Current-Voltage I(V) characteristic was measured by Keithley 2611 source-ammeter. Small-signal measurements (C(V), $C(f)$, impedance, admittance) were performed with a constant a.c voltage of $V_{ac} = 20\ mV$ by Solartron Modulab impedance analyzer. Capacitance characteristics that will be introduced in the following section represent the measured capacitance of the equipment which is $C_m = \frac{1}{2\pi f Z}$ where Z is the modulus of the measured impedance. To perform conductance method, the parallel capacitance-conductance circuit ($C_p - R_p$) can be evaluated by using the real part and imaginary part of the measured impedance. Electrostatics simulation was performed using Nextnano[3] software. The band

alignment for electrostatics simulation is known from the XPS measurement introduced by Maréchal et al.[13]

B. Typical electrical characteristics

Typical electrical characteristics of O-diamond MOSCAPs can be summarized in Fig. 2. These results are measured from MOSC7 test device on sample #2 and in agreement with O-diamond MOSCAPs that have been previously fabricated and reported by our group[11,13] and the results published in literature[12].

Figure 2a) represents the I(V) characteristics. Under negative gate bias, leakage currents are systematically observed. Under positive bias, leakage currents are randomly observed among several test devices (in the current MOSCAP, leakage current under positive bias are below the apparatus detection limit). In the following sections, we will investigate the origin of leakage currents and capacitance-frequency dependence for the O-diamond MOSCAPs under negative bias. The origin of the random leakage currents and capacitance frequency dependence for O-diamond MOSCAPs under positive bias will be discussed in another work.

Figure 2b) represents the C(V) characteristics at different frequencies, ranging from 1 kHz to 1 MHz on the same MOSCAP test device and the same bias range with I(V) measurement. A strong capacitance-frequency dependence is observed when the more negative gate bias ($-4\ V \leq V_G \leq -6\ V$) is applied. For the high positive bias range, the capacitance-frequency dependence is not observed in this MOSCAP test device.

The capacitance-frequency dependence under negative bias can be further seen by C(f) measurements, as shown in Fig. 2c). From the $C(f)$ curves, three different regimes can be distinguished: *i*) *High frequency regime* (between 500 kHz and 1 MHz): There is a minor effect from series resistance which induces a slight capacitance increase versus f. However, in our pseudo-vertical MOSCAPs, series resistance contribution is almost negligible. *ii*) *Low frequency regime* (from 1 Hz to about 40 kHz for $V_G = -6\ V$; from 1 Hz to 4 kHz at $V_G = -4\ V$; from 1 Hz to 200 Hz at $V_G = -2\ V$; and almost negligible in the whole frequency range for $V_G = 0\ V$): the measured capacitance is strongly frequency dependent. Capacitance decreases with a slope of 20 dB/dec. Previous reports on O-diamond MOSCAPs[11,12] showed that the capacitance frequency dependence of the "low frequency range"is huge. In Kovi et al.[12], the "low frequency range" is even observed for the frequencies up to few MHz. *iii*)

Middle frequency regime (the regime between "high frequency"and "low frequency"): the measured capacitance is constant versus frequency. This frequency window is too low to be assigned to a series resistance effect and too high to be related to an interface states contribution. The C(V) measurement in this frequency window is considered as the proper C(V) characteristic of the MOSCAP. In other words, MOSCAP test device is in the ideal MOSCAP configuration i.e. oxide capacitor C_{ox} and semiconductor capacitor C_{sc} are in series. In this configuration, the measured capacitor of the MOSCAP writes: $C_{MOS} = \frac{C_{ox}C_{sc}}{C_{ox}+C_{sc}}$.

In the following section, we will employ this proper C(V) measurement to evaluate the key informations of our O-diamond MOSCAP test devices.

III. ELECTROSTATICS: ELECTRIC CHARGES, ELECTRIC FIELD AND POTENTIAL DISTRIBUTION

This section is dedicated to quantify different electric charge components and to establish the electrostatic band diagram of the O-diamond MOSCAP.

A. Proper C(V) measurement

As shown in the typical C(f) characteristics (Fig. 2c), capacitance measurement is affected by series resistance at high frequency regime and by other artifacts at low frequency regime. In our experiment, prior to perform C(V) measurements, the C(f) measurements have been systematically employed to determine the "middle frequency" window, which corresponds to each MOSCAP.

The open red circles curve in Fig. 3 represents the C(V) characteristics of MOS 12−sample #1 at $f = 100$ kHz, which is in the proper frequency window of this MOSCAP device. From the proper C(V) curve, notable behaviors can be noticed as:

i) Under negative bias, for bias lower than the flatband voltage of the MOSCAP, the accumulation regime is expected corresponding to $C_{MOS} = C_{ox}$. In our case, the measured capacitance is much lower than the oxide capacitance $C_m << C_{ox}$ even for $V_G = -8$ V. Measured capacitance can be normalized to the oxide capacitance $C_{ox} = 0.4\mu F.cm^{-2}$, measured from MIMCAP test devices on the same sample. A maximum measured capaci-

tance of $C_m = 0.135\mu F.cm^{-2}$ at $V_G = -8\ V$ is observed, corresponding to $C_m \simeq 0.35C_{ox}$. The systematic measurements demonstrated that this behavior is general for all measurable MOSCAPs on the same substrate[15].

ii) The measured capacitance for positive bias does not show the saturation of minimum capacitance C_{min}. Up to $V_G = +8\ V$, the measured capacitance monotonously decreases versus V_G corresponding to the deep depletion regime.

iii) By sweeping the bias voltage from $+8\ V$ to $-8\ V$ and then from $-8\ V$ to $+8\ V$, C(V) characteristics are almost identical. No sign of mobile oxide charges in this MOSCAPs test devices can be observed[15].

In summary, from the proper C(V) measurement, three different charge components in the O-diamond MOSCAP can be envisaged: semiconductor charges, oxide charges and interface charges.

B. Semiconductor charges

From proper C(V) measurement, the semiconductor doping concentration is extracted using the Schottky-Mott plot. The open black circle curve in Fig. 3 represents the Schottky-Mott plot (reciprocal square capacitance versus gate bias plot $\frac{1}{C^2}$ vs. V_G). The term $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ is used to eliminate the effect from oxide capacitance[16]. The $\frac{1}{C^2}$ (V_G) curve exhibits an almost perfect straight line for the gate voltage ranging from V_G=$-6\ V$ to $V_G = 8\ V$. From the slope of the curve, the doping concentration of the B-doped semiconducting diamond layer can be extracted by using the equation:

$$N_A = \frac{-2}{\varepsilon\varepsilon_0 A^2} \frac{1}{dC^2/dV} \tag{1}$$

with $\varepsilon = 5.7$ the diamond dielectric constant, ε_o the vacuum permittivity and A the area of the diode. A doping concentration of $N_A = 3 \times 10^{17}\ cm^{-3}$ is extracted from the $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G curve. This value is almost identical with the targeted value expected from the diamond growth parameters. Systematic measurements demonstrated the homogeneous and well-controlled dopant incorporation in B-doped diamond epilayer[15].

C. Oxide charges

One notable feature that can be seen from the C(V) curve and $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G curve is the shift of the curves toward negative bias, compared to the ideal case. In fact, this shift is possibly induced by the interface charges, the oxide charges and the work function difference between metal and semiconductor. However, since our C(V) measurements were performed at 100 kHz, we can exclude the a.c contribution from the interface charges. As the slope of $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ versus V_G in the range of examination has reliably reflected diamond doping concentration, the DC contribution of interface states is deduced to be negligible also for this gate voltage range. The experimental flatband voltage V_{FB}, corresponding to the voltage at which the extrapolated $\frac{1}{C_m^2} - \frac{1}{C_{ox}^2}$ straight line intercepts the horizontal axis, is equals to $-7.3\ V$. This value is larger than the theoretical one, i.e. $V_{FB} = \phi_M - \phi_{SC} = -2.6$ V where $\phi_M = 4.3\ eV$ is the work function of Ti metal and the semiconductor work function is $\phi_{SC} \simeq E_G + \chi_{sc} - E_F = -6.9\ eV$ with $\chi_{sc} = 1.7\ eV$ the electron affinity of O-diamond[17], E_G the diamond band gap and E_F the Fermi level in the neutral region of the B-doped diamond referenced from the valence band ($E_V = 0$). This experiment demonstrates that the measured flat band voltage includes a contribution of charges in the oxide Q_{ox}. By applying the equation[18]:

$$Q_{ox} = \frac{C_{ox}\left(\phi_{MS} - V_{FB}\right)}{qAt_{ox}} \tag{2}$$

A net positive oxide charge density of $Q_{ox1} = 1.2 \times 10^{13}\,(cm^{-3})$ is deduced for sample #1. The shift of flatband voltage in sample #2 is about $-5.4\ V$ where the oxide charge is calculated as $Q_{ox2} = 7 \times 10^{12}\,(cm^{-2})$.

D. Fermi level pinning effect due to a strong interface states density

MOSCAP is the suitable device to examine the efficiency of gate controlled semiconductor structure. As discussed by Vincent et al.[19], semiconductor surface potential Ψ_s is the critical quantity for this evaluation. Ψ_s corresponds to the electrical potential variation between the neutral part of the semiconductor, where the Fermi level is flat, and the semiconductor surface, i.e. at the oxide interface. When $\Psi_s = 0$ eV, the semiconductor is in the flatband regime. Therefore, flatband regime is the demarcation between accumulation regime and

depletion regime. In the flatband regime, the semiconductor charge $Q_{sc}\,(V_G = V_{FB})$ and consequently the semiconductor capacitance $\mathrm{C}_{sc}\,(V_G = V_{FB})$ is a function of the intrinsic semiconductor Debye length as:

$$C_{sc}\,(V_G = V_{FB}) = \frac{\varepsilon_{sc}\varepsilon_0}{\lambda_p} \tag{3}$$

where λ_p is the semiconductor intrinsic Debye length, which writes $\lambda_p = \left(\frac{\varepsilon_{sc}\varepsilon_0 kT}{q^2 N_A}\right)^{1/2}$.

With N_A extracted from the previous section, the semiconductor flatband capacitance $\mathrm{C}_{sc}\,(V_G = V_{FB})$ can be evaluated. Subsequently, the flatband capacitance of the MOSCAP $\mathrm{C}_{MOS}\,(V_G = V_{FB})$ is evaluated as:

$$\frac{1}{C_{MOS}(V_G = V_{FB})} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}(V_G = V_{FB})} \tag{4}$$

From these relationships, a MOSCAP flatband capacitance of $C_{MOS}\ (V_G = V_{FB}) = 0.279$ $\mu F.cm^{-2}$ is evaluated for MOS12 - sample #1. With the semiconductor doping concentration being homogeneous[15], this value is typical of the MOSCAP measured on the whole sample. As shown in Fig. 3, the maximum measured capacitance of O-diamond MOSCAP at $V_G = -8\ V$ ($C_m = 0.135\ \mu F.cm^{-2}$) is lower than the flatband capacitance C_{FB}. Therefore, it can be concluded that the diamond MOSCAP is always in depletion regime even for high negative bias ($V_G = -8\ V$). In previous reports, Chicot et al.[10,11] and Kovi et al.[12] measured similar C(V) characteristics and deduced that their MOSCAP reached the accumulation regime. However, the present study shows that this assignment is erroneous and the misunderstanding is induced by the parasitic frequency dependence.

Since diamond is always in depletion regime, semiconductor space charge region (SCR) width is proportional to the square root of the surface potential Ψ_s[19] in the whole voltage range ($+8\ V$ to $-8\ V$). Therefore, the semiconductor capacitance is also proportional to the square root of the semiconductor surface potential as[20]:

$$C_s = \sqrt{\frac{qN_A\varepsilon_o\varepsilon_s}{2\Psi_s}} \tag{5}$$

As the measured capacitance C_m and the oxide capacitance C_{ox} are determined, the semiconductor capacitance C_{sc} and the semiconductor surface potential Ψ_s can be calculated. By performing a simple mathematical derivation of equations 4 and 5, the surface potential

corresponding to a specific gate bias voltage can be written:

$$\Psi_s\left(V_G\right)=\frac{q^2 N_A \varepsilon_o \varepsilon_s\left(\frac{C_{ox}}{C_m(V_G)}-1\right)^2}{2C_{ox}^2} \tag{6}$$

In principle, by performing this calculation at different gate bias, we can establish the relationship between semiconductor surface potential versus gate bias voltage ($\Psi_s - V_G$), and so evaluate the efficiency of gate control semiconductor. For negative gate bias (V_G : down to -8V), Ψ_s stays positive showing that the Fermi Level Pinning Effect (FLPE)[21] is observed. The semiconductor regime at the interface approaches but never reaches the flatband voltage. This FLPE can be illustrated by the $\frac{1}{C_m^2}-\frac{1}{C_{ox}^2}$ values, which are saturating and tending to a positive value for gate bias lower than -6V.

The strong FLPE observed here is assumed to be due to the presence of interface states in the semiconductor forbidden gap[20,22]. An evaluation of their density can be done thanks to the quantitative analysis of the capacitance stretching due to FLPE. This is the main idea of the high frequency-capacitance method developed by Terman[22]. With $\Psi_s - V_G$ evaluated from eq.6, the interface states capacitance C_{it} versus Ψ_s is calculated by the high frequency capacitance method[20,22]:

$$C_{it}\left(\Psi_s\right)=C_{ox}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1}-1\right]-C_s\left(\Psi_s\right) \tag{7}$$

Subsequently, the interface states density D_{it} can be evaluated by[20]:

$$D_{it}\left(\Psi_s\right)=\frac{C_{it}\left(\Psi_s\right)}{q} \tag{8}$$

An interface states density of less than 10^{12} ($\mathrm{eV}^{-1}.\mathrm{cm}^{-2}$) is found in the midgap region and an abrupt increase up to 4×10^{13} ($\mathrm{eV}^{-1}.\mathrm{cm}^{-2}$) for the interface states near the valence band edge ($E_t - E_v \approx 0.6$ eV). We will see later that this method is not adapted to our case and overestimates the D_{it} values. Indeed, the leakage current through the oxide is too high to consider the interface under equilibrium.

E. Electrostatics simulation

We performed the electrostatics simulation by implementing the semiconductor charges qN_A extracted from the $\frac{1}{C^2}-V_G$ curve, oxide charges Q_{ox} extracted from the shift of V_{FB}

and interface charges $\sigma_{it}(V_G)$ extracted from Terman method. Interface states charge is evaluated by integrating the interface states density over the energy band gap.

The electrostatics band diagrams of O-diamond MOSCAP for a gate bias of -5V is shown in Fig. 4 a). One remarkable issue from electrostatics simulation, which is not obvious from C-V measurement is the potential distribution within the oxide. This electrostatic band diagram is essential to identify the origin of leakage current and capacitance-frequency dependence under negative bias.

IV. GATE OXIDE LEAKAGE CURRENT MECHANISM AND EQUIVALENT SMALL SIGNAL CIRCUIT

This section is dedicated to the analysis of the leakage current from metal to semiconductor and the corresponding equivalent small signal circuit.

A. Leakage current mechanism

In an ideal MOSCAP, the gate oxide prevents carrier transport between the gate metal and the semiconductor. Electrostatics gate control of carrier population at the oxide/semiconductor interface is crucial for semiconductor devices. However, in real situations, leakage currents are usually observed and perturb the carrier control.

In order to understand the origin of leakage currents, the source of transporting carriers must be determined. For a p-type MOSCAP under negative bias regime, currents are initiated from either the accumulated semiconductor majority carriers or gate metal carriers reservoir[23]. For O-diamond MOSCAPs, as evidenced from $C-V-f$ analysis and electrostatics band diagram, we concluded that leakage current under negative bias is initiated from carriers reservoir of metal gate and not from accumulated hole of diamond semiconductor. This conclusion is based on the fact that FLPE preserved diamond in depletion regime, even at high negative bias (e.g $V_G = -8$ V, MOS 12 - sample #1). No majority carriers (hole) are able to accumulate at the diamond-oxide interface. The transport due to accumulated majority carriers is therefore prohibited.

The next question to be addressed is, how do these carriers circulate in the MOSCAP system? Thanks to Nextnano electrostatics band diagram, we proposed a 5-steps current

mechanism, as shown in Fig. 4a). In step 1, carriers from gate metal are tunneling into the oxide trap states. Hopping between traps to traps through the oxide is taking place during step 2. In step 3, hopping carriers are captured by interface states. The charge transfer between interface states and valence band are taking place in step 4. Finally, these carriers drift through the diamond epilayer to the back gate contact (p^+) and complete the transfer process.

Potentially, the flow at each step may includes different processes in parallel. In principle, the process with highest rate (slowest time constant) dominates the flow at each step. On another hand, in order to complete a circulation, different steps in series could be involved. The step with the slowest rate (longest time constant) is the limiting process.

In the proposed current mechanism (Fig. 4a), interface states play a central role with a special interest. They are able to communicate with both the metal electrode and the semiconductor valence band. In principle, each charge transfer process is represented by its characteristic time constant τ. For the sake of simplicity and without losing the generality, we will firstly consider interface states as a single level state at energy $E_{it} - E_v$ and density N_{it}. In the following sections, we will discuss further the charge transfer between interface states with metal and semiconductor band edge.

Charge transfer between metal and interface states

The charge transfer between gate metal and interface states in a MOSCAP system was addressed by Dahlke and Sze[23]. The complementary theory was then developed by Freeman and Dahlke[24]. In their theory, interface states are modeled as a potential well and communicate with the gate metal by direct tunneling. The charge transfer is considered as an overlapping process of two wave functions. Kar and Dahlke experimentally studied the metal injection into interface states with a non-degenerate Si substrate and a moderate oxide thickness ($20 - 40$ Å) MOS capacitor system[25]. A noticeable possible consequence of carriers injection from gate metal to interface states is that these carriers are possibly accommodated by interface states and therefore modulating Schottky barriers height at metal-semiconductor contact[26–28] and metal-insulator-semiconductor interface as well.

In our case, the oxide is too thick to observe direct tunneling. Therefore, carriers injection from metal to interface states is suggested to be a process of two consecutive steps:

the carriers tunneling from gate metal to oxide trap states (represented by tunneling time constant τ_{tun}) and then carrier hopping between trap sites happens in the oxide (represented by hopping time constant τ_{hop}). The two consecutive processes must happen in series and so the tunneling time constant τ_T (from metal/oxide to oxide/semiconductor interface) writes:

$$\tau_T = \tau_{tun} + \tau_{hop} \tag{9}$$

Tunneling from metal to oxide trap states As shown in Fig. 4 a), electrons from gate metal are suggested to initiate the flow by tunneling into Al_2O_3 gate oxide layer. Even if there are many possible processes for a carrier from gate metal to be injected into the gate oxide[29], most of them are practically not possible in our case. It is either direct tunneling, thermionic emission (Schottky injection) or tunneling into many trap states in the oxide. Considering the oxide thicknesses of $10-40$ nm that were systematically used for O-diamond MOS capacitors, direct tunneling by overlapping wave functions (theoretically less than 1 nm)[23] is not possible. Thermionic emission is a thermal activation process where carriers from the gate metal have to reach a sufficient energy to jump over the metal-oxide barrier height and being injected into the oxide layer. Regarding an approximate 3 eV barrier height between Ti and Al_2O_3, this process is not realistic. Also, the tunneling of carriers from the gate metal into oxide trap states[30] of the gate oxide is the most realistic process.

Tunneling current from the gate metal to oxide trap states can be approximately described by[31]:

$$I = N_t q \nu_{tun} \tag{10}$$

where N_t is the density of nearest traps contributing to the conduction and ν_{tun} is the tunneling transmission rate. The tunneling transmission rate is:

$$\nu_{tun} = \frac{1}{\tau_{tun}} = v_o f_T T_{WKB} \tag{11}$$

with $v_0 \sim 10^{13}$ Hz the attempt frequency which represents the rate of escape of a particle from a confining structure by quantum tunneling through its outer barrier. f_T is the Fermi-Dirac function representing the occupancy probability of a trap state in the oxide. It can be expressed by:

$$f_T = 1/\left(1 + \exp\left(\frac{E_a + Fx}{kT}\right)\right) \tag{12}$$

where $E_a = E_b - E_t$ is the electron barrier between metal electrode and trap states, E_b is the electron barrier between metal electrode and oxide conduction band, E_t is the energy of the

traps in the oxide, F is electric field in the oxide and x is the distance from the metal/oxide to the trap where the electron is tunneling (Fig. 4a)). T_{WKB} is the Wentzel-Kramers-Brillouin (WKB) transmission coefficient and can be written as[32]:

$$T_{WKB} = \exp\left(-\frac{4}{3\hbar qF}\sqrt{2m^*}\left((E_t + qFx)^{3/2} - E_t^{3/2}\right)\right) \tag{13}$$

with $\hbar$ is the reduced Planck constant and m* the effective mass of electron in the oxide[31].

Hopping in the oxide Carriers transport in the oxide could be the sum of multiple parallel mechanisms[29,31]. One of two main mechanisms is the thermal activation from deep energy traps to oxide conduction band, which is generally called Poole-Frenkel emission. The second one is tunneling from traps to traps, also called hopping. In order to determine the dominant process, transfer rates of each process are necessary to be evaluated. The Poole-Frenkel emission rate is scaled versus T as $v_0 \exp\left(-\frac{E_c - E_t}{kT}\right)$ where E$_t$ is the energy of the traps in the oxide band gap[31]. In the case of Al_2O_3 oxide deposited by ALD, trap states are usually ascribed to the non-stoichiometry of the oxide. From first principle simulation, the oxygen vacancy is found to be the electron trap level which is the nearest from the conduction band as $E_c - E_t = 1$ eV[33].

The trap to trap tunneling rate is calculated as[31]

$$\nu_{hop} = \frac{1}{\tau_{hop}} = v_0 \exp\left(-\frac{2R}{\xi}\right) \tag{14}$$

with ξ the electron wave function localization length $\xi \simeq 0.3$ nm, R distance between trap sites[31]. Distance between trap sites could be obtained by fitting the DC non-linearity capacitance-voltage of MIMCAPs[34]. The distance between trap sites in our ALD Al_2O_3 is then estimated to be approximately 5 nm[15].

A rough evaluation shows that the tunneling rate from trap to trap is almost 150 times faster than Poole-Frenkel thermal activation rate from traps level to conduction band at room temperature[15]. In case that an oxide trap level is deeper from oxide conduction band, which will be found below, the injection rate in step I will be even slower. It is therefore possible to conclude that tunneling from trap to trap is the main transport mechanism in the oxide.

Carrier readjustment

In step III, carrier readjustment is taking place. The readjustment process is a transfer from the energy levels of the oxide traps to the quasi-Fermi level of semiconductor at semiconductor/oxide interface. As depicted in Fig. 4 a), interface traps include two main parts: Acceptor-like levels close to the conduction band and donor-like levels close to the valence band, defining a charge neutrality level (CNL). If the quasi-Fermi level is below the CNL (as shown in Fig. 4 a) donor-like levels will be positively charged between the quasi-Fermi level and the CNL. The other interface states will be neutral. In this case, the time for carriers readjustment, trapped by interface states (step III), will be neglected because its thermalization process is very fast compared to other processes[35].

Charge transfer between interface states and semiconductor band edges

In step IV, the trapped electrons at interface states emit to the semiconductor valence band. We will firstly consider the single level interface states model with density N_{it} and energy $E_{it} - E_v$ from the valence band.

The serial charge transfers from gate electrode to interface states and from interface states to semiconductor valence band can be described by the differential equation[24]:

$$N_{it}\frac{df_t}{dt} = -U_{cp} + \frac{j}{q}. \tag{15}$$

where j is the current injected from metal gate to interface states. U_{cp} is the charge transfer rate of trapped carriers at interface states to semiconductor valence band and can be described by[35]:

$$U_{cp} = N_{it}\sigma_p\langle\upsilon_{th}\rangle\left(fp_s - f_p p_1\right) \tag{16}$$

with σ_p is the hole capture cross-section of the trap states, v_{th} is the carriers mean thermal velocity, f and f_p are the occupation probabilities of a trap state by an electron and hole, respectively[35]. $p_s = p_b \exp\left(\frac{-e\Psi_s}{kT}\right)$ is the surface carriers density at thermal equilibrium with p_b the bulk carriers density. $p_1 = N_v \exp\left(\frac{E_v - E_{it}}{kT}\right)$ represents the carrier density that established at the trap states when the quasi-Fermi level equals the trap states level[24]. E_F is the quasi-Fermi level and N_v is the effective density of states of the valence band.

The current in and out interface states discussed above is then described by the interface

states occupancy f_{ss}[24,25] which is:

$$f_{ss} = (\tau_R f_m + \tau_T f_s) \,/\, (\tau_R + \tau_T) \tag{17}$$

where f_s and f_m are the bulk semiconductor and metal occupancies, respectively[24]. τ_R is the recombination time constant of majority carriers with interface states and to be calculated:

$$\tau_R = \frac{1}{\sigma_p \upsilon_{th} p_b} \exp(\Psi_s) \tag{18}$$

Drift in the diamond layer

The process of electron being emitted to the valence band is equivalent to the process of holes from the valence band to be captured by interface states. To replace the swept hole, a hole from the back side (p+ layer) will move to the diamond surface and be ready for a new capture event[36]. In the reverse direction, electrons are transferring to the back gate contact (p^+) and complete the circulation.

B. Equivalent circuit and approximation

Equivalent circuit

In order to model the measured impedance and admittance of a MOS capacitor, linearized equivalent circuit is a well-known concept. Lehovec and Sloboskoy[37] developed a comprehensive theory and derived a general equivalent circuit for the MOS capacitors. Nicollian and Goetzberger[38] paid special attention to the conductance of interface states in "thick oxide MOS capacitor": The meaning of "thick oxide" is that the interface states are in equilibrium and close communication with the semiconductor band edges. They also developed a model to evaluate the equivalent conductance G_P/ω that depends only interface states density and its time constant from the parallel capacitance-conductance ($\mathrm{C}_p - R_p$) circuit[38].

For the special case where interface states communicate with both gate metal and semiconductor band edges, Freeman and Dahlke[24] developed the theory as well as the corresponding equivalent circuits. Different possible limiting processes were also discussed. The approximated equivalent circuits corresponding to each limiting case were also proposed. Since then, there were different discussions about the possibilities and opportunities

to employ gate tunneling into interface states to measure a wide range of interface states density[25,39,40]. Kar and Dahlke[25] performed the experiments on Si/SiO_2 MOSCAPs with moderate oxide thickness and a non-degenerate Si semiconductor to investigate interface states thanks to gate carriers injected to interface states.

In an ideal case, where only the unavoidable series resistance of the drift layer is involved, the equivalent circuit of MOSCAP can be represented by Fig. 4b). In case of single level interface states involved in thick oxide MOSCAP (without leakage current), the equivalent circuit is represented as in Fig. 4c).

In our O-diamond MOSCAPs, corresponding to the current mechanism suggested in Fig. 4a), we introduce an equivalent circuit as in Fig. 4d). Non-perfect gate oxide with gate leakage currents is modeled by an oxide conductance G_{ox} and an oxide capacitance C_{ox} in parallel. The flow of carriers from metal to semiconductor is injected to the mid point of the interface states recombination circuit, as proposed by Freeman et al.[24].
This general equivalent circuit can be further simplified by the approximations corresponding to the leakage current limiting process.

Approximation

The O-diamond MOSCAP equivalent circuit will be simplified to the approximated equivalent circuits depending on the limiting transport processes of the leakage current. We remind that the equivalent circuit in the general case is shown in Fig. 4c. In the theoretical model of Freeman and Dahlke[24] and in the experiments and analysis of Kar and Dahlke[25], different limiting processes and their corresponding approximations were discussed. We will briefly reintroduce these approximations here for the purpose of clarification.

As the carriers readjustment to interface states (step III) and drift in semiconductor (step V) are expected to be much faster compared to two other processes, we will only consider the interface states recombination limited and the oxide tunneling limited.

Interface states recombination limited The interface states recombination is limited when the interface states recombination time constant is much longer than the oxide tunneling time constant ($\tau_R >> \tau_T$). In other words, the oxide tunneling rate is much higher than the interface recombination rate. The interface states will thus be in equilibrium with the metal gate. In this case, the interface states recombination limited was found to modify the

Schottky barrier height due to the charge accumulated at the interface states[26–28]. Therefore, a self-consistent calculation is necessary to be performed in order not to violate the Gauss's law equations, as discussed by Werner et al.[27]. The rigorous self-consistence calculation was done by Muret[28] and also Werner et al.[27] for Schottky diodes with a thin oxide layer.

In case of a MOSCAP system, the approximated equivalent circuit for the interface recombination limited was introduced by Freeman and Dahlke[24] and Kar and Dahlke[25]. The approximated equivalent circuit is shown in Fig. 5a) where interface states recombination is in equilibrium with with the metal gate and interface states at the same potential as the oxide potential. In this circuit, G_{it} is equal to $\frac{1}{R_{it}}$. One important notice is that, in case of interface states recombination limited, the measured conductance is frequency independent[24,25].

Oxide tunneling limited When the oxide tunneling time constant is much longer compared to the interface states recombination time constant $\tau_T >> \tau_R$, the limiting process is the oxide tunneling. This means that interface states are considered to be in equilibrium with the semiconductor[24,25] and so, the injection from metal to interface states is approximated by an injection from the metal gate to the semiconductor. Interface states therefore will play a similar role as in the "non-leaky thick oxide" model where the interface states are in equilibrium and close communication with semiconductor band edges. In this circuit, G_{dc} is approximated to G_{ox} in Fig. 4b. The approximated equivalent circuit for oxide tunneling limited is shown in Fig. 5b).

A major difference between *interface states recombination limited* (Fig. 5 a) and *oxide tunneling limited* (Fig. 5b) is the measured conductance-frequency characteristics. For the purpose of comparison, the measured conductance circuit is the parallel conductance-capacitance $C_p - R_p$ circuit in Fig. 5f). In case of oxide tunneling limited, the measured conductance is frequency dependent, as shown in Fig. 5b). For the case of interface states recombination limited (Fig. 5a), the measured conductance is frequency independent[25].

Considering the O-diamond MOSCAPs of this work, the measured conductance frequency dependence[15] indicates that the oxide tunneling process is the limiting process. The interface states recombination limited is possibly responsible in case of high injection MOSCAPs (e.g. current density ≥ 1 A/cm^2 at -8 V). In that case, the carriers injection from metal gate is sufficient to preserve interface states in equilibrium with the metal gate. The sample MOS #4 in Chicot et al.[10] and the sample 4×10^{19} cm^{-3} boron doped diamond in Kovi et al.[12] are most probably interface states recombination limited.

As a consequence from the previous analyses, the oxide tunneling process was identified as the limiting process in our MOSCAP test devices. However, since oxide tunneling is indeed a two step process, a further approximation is needed. Bearing in mind that the limiting process for oxide tunneling is either bulk oxide limited (hopping between traps to traps) or interface limited (tunneling from metal gate to oxide trap states). The difference is due to the nature of the contact between metal and oxide, i.e. an ohmic contact or an unsaturated contact[41]. Ohmic contact indicates the strong injection of carrier from metal electrode to oxide layer. Unsaturated contact indicates the low injection of carrier from metal electrode to oxide layer. Depending on the nature of metal/oxide contact, I(V) characteristics will exhibit a specific power law of $I = AV^{\alpha}$. Therefore, in order to examine the power law of MOSCAPs and the contact nature at metal/oxide interface, we introduce the I(V) curves in the log-log plot. Figure 6 a) and Figure 6 c) represent the power law of two typical MOSCAPs: low injection MOSCAP (MOS50 - sample #1) and high injection MOSCAP (MOSA1 - sample #1), respectively.

For the low injection MOSCAP at RT (Fig. 6 a)), the $I \sim V^5$ law indicates that the metal-oxide contact in this device is the unsaturated contact. The interface-limited traps assisted tunneling[42] mechanism is probably governing this low injection MOSCAP at RT.

To study the thermal activation process, we measured the I(V) characteristic of the low injection MOSCAP at different temperatures, ranging from 160 K to 360 K. Figure 6b) represents the Arrhenius plot current density versus temperature of the low injection MOSCAP, measured at three different gate bias: $V_G = -8\ V$, $-6\ V$ and $-4\ V$. From the slope, the thermal activation energy at different gate bias can be evaluated. The thermal activation energies are varying from $E_A = 260\ meV$ at $V_G = -4V$ to $E_A = 208meV$ at $V_G = -4V$. As suggested from the generalized thermionic trap assisted tunneling model[42], this thermal activation energy is assigned to the barriers between metal and Fermi-Dirac occupancy function of the oxide trap states (Fig. 4a). This thermal activation energy variation with gate bias is in agreement with eq. 12.

For high injection MOSCAP (MOSA1 - sample #1), the I(V) characteristics at different temperatures from 160 K to 360 K are shown in Fig. 6c). At RT, the $I \sim V^2$ of Child law for Space Charge Limited Current (SCLC)[43] is identified (Fig. 6c). This power law indicates that the metal-oxide contact of this MOSCAP is an Ohmic contact at RT and the limiting process is the trap-to-trap hopping process in the bulk of the gate oxide.

Figure 6d) represents the current density measured at $V_G = -8$ V versus temperature of the high injection MOSCAP. The J-T curve is well fitted by a $e^{(\frac{T_0}{T})^{1/4}}$ law, which is characteristic of variable range hopping (VRH)[44]. This further confirms the trap-to-trap hopping space charge limited current in the high injection MOSCAPs.

In summary, this analysis demonstrates that one of the most important reason of the leakage current in O-diamond MOSCAPs relies on the presence of trap states in the gate oxide. To improve the gate controlled diamond semiconductor, the gate oxide leakage current must be minimized by introducing a new process that could limit both the metal/oxide interface injection and traps to traps hopping in the bulk of the oxide layer.

V. INTERFACE STATES OF AL_2O_3/O-TERMINATED DIAMOND

This section is dedicated to the investigation of interface states properties at Al_2O_3/O-terminated diamond interface. Thanks to the small signal equivalent circuit discussed above, we will be able to use a corrected conductance method in order to determine the interface traps density and their energy location within the diamond bandgap.

A. Equivalent conductance G_p/ω

The conductance of interface states ($G_{it} = \frac{1}{R_{it}}$ where R_{it} is the one of Fig. 4c represents the energy loss due to carrier transfer between semiconductor band edge and interface states after a disturbance of a small *ac* signal. In more details, it can be understood as the small ac signal in both halves of the alternative voltage which causes the disturbance of the trapped carrier population and drives the system between semiconductor band edge and interface stated out of equilibrium. Therefore, there are carriers transferred between interface states and band edge. However, the carrier transfer is not instantaneous after the signal was supplied but lag behind and caused the loss. The losses are minimized or the conductance is maximized when the signal frequency matches the reciprocal time constant of interface states. With the applied frequency lower than the reciprocal time constant of interface states, carriers are stored at the capacitance of the interface states but not transferred. Subsequently, the conductance of the interface states is decreased. Therefore, the conductance of interface states which is bearing the information of interface states should

have a bell shape. In the conductance method, the goal is to obtain the equivalent interface states conductance from measured conductance and capacitance ($C_p - R_p$).

In order to obtain the equivalent interface states conductance, measured parallel conductance and parallel capacitance are necessary to be corrected in order to eliminate the series resistance, the DC current and gate oxide capacitance. In this work, the circuit transformation follows the procedures introduced by Kar and Dahlke[25] and by Vogel et al.[45].

From the measured conductance and capacitance, the corrected conductance with series resistance of Fig. 5f) is given by:

$$C_c = \frac{C_p}{(1 - G_p R_s)^2 + \omega^2 C_p^2 R_s^2} \tag{19}$$

and the corrected capacitance by:

$$G_c = \frac{\omega^2 C_p C_c R_s - G_p}{G_p R_s - 1} \tag{20}$$

Then, G_{ac} in Fig. 5e) is obtained by:

$$G_{ac} = G_c - G_{dc} \tag{21}$$

where the conductance G_{dc} is determined from the slope of the DC current versus DC voltage curve at a given gate bias voltage $\left(\frac{dI_{dc}}{dV_{dc}}\right)_{V_G}$. Then, the ac conductance G_{ac} must be corrected with the gate oxide capacitance C_{ox} to obtain the equivalent conductance G_P/ω by using the equation:

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_{ac}}{G_c^2 + \omega^2 \left(C_{ox} - C_c\right)^2} \tag{22}$$

For the purpose of comparison the interface states density with Terman's method, we will present here the data measured on the MOS 12 on sample #1). The equivalent conductance at different gate bias are shown in Fig. 7a). The equivalent conductance shows the clear bell shape feature with a clear maximum $\left(\frac{G_P}{\omega}\right)_{\max}$ peak. As mentioned above, the frequency corresponding to the $\left(\frac{G_P}{\omega}\right)_{\max}$ is equivalent to the reciprocal time constant of interface states. By varying the gate bias from $-8\ V$ to $-4\ V$ (MOS 12 - sample #1), the $\left(\frac{G_P}{\omega}\right)_{\max}$ are gradually moving toward the lower frequency since the Fermi level is moving away from the valence band.

B. Interface states properties

From the equivalent conductance G_P/ω, the interface states density can be calculated as[38]:

$$N_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}/q \tag{23}$$

with $\left(\frac{G_P}{\omega}\right)_{\max}$ the maximum of the $\left(\frac{G_P}{\omega}\right)$ curve. The open red circle curve in Fig. 7b) represents the interface states density extracted by conductance method versus the corresponding energy of the trap states in diamond band gap. The energy level of the trap states is then calculated by using the equation:

$$E_{it}\left(V_G\right) - E_v = \Psi_s\left(V_G\right) + \phi_p \tag{24}$$

where $\Psi_s\left(V_G\right)$ is extracted in the previous electrostatics section and $\phi_p \simeq \left(\frac{kT}{q}\right)\ln\left(\frac{N_v}{N_A}\right)$, which is assumed to be 0.37 eV in the case of moderate boron doped diamond.

A notable difference of the interface states density extracted from the conductance method compared to the interface density extracted from Terman's method (the open black circle curve in Fig. 7b)) appears near the valence band. While Terman's method gives an increasing interface states density up to $4 \times 10^{13}\,(cm^{-2})$ at $\mathrm{E}_{it} - E_v = 0.6$ eV, the results from the conductance method are approximately one order of magnitude lower in the same energy range.

This discrepancy is attributed to the gate leakage current and subsequently, the potential drop in the gate oxide. In Terman's method[22], the variation of semiconductor surface potential Ψ_S with gate bias V_G is completely attributed to the interface states at the semiconductor/oxide interface. It is true when leakage current through the oxide is negligible. However, when the DC current is sufficient, the potential drop in the gate oxide is non-negligible. Therefore, in high injection regime, Terman's method highly overestimates the interface states density and cannot be used to evaluate the interface trap density.

In the conductance method, the contribution of DC current is actually excluded by equation 21. The final interface states density will therefore exclude the contribution from DC current. Electrostatic simulations $\Psi_S - V_G$ using the interface states density extracted from Terman's method and from the conductance method have further demonstrated the accuracy of the conductance method[15]. We conclude that the interface states density extracted from the conductance method is more reliable than Terman's method.

By assuming that the interface states are single level states[38], i.e. Dirac energy distribution for the density of the trap, the equivalent conductance G_P/ω can be simulated by using the equation:

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1+\omega^2\tau^2} \tag{25}$$

where τ is the characteristic time constant of interface states and is determined at $\left(\frac{G_P}{\omega}\right)_{\max}$, where $\omega\tau = 1$. The interface states capacitance C_{it} can be determined from the peak of the equivalent conductance G_P/ω as $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$. Knowing all parameters, the measured equivalent conductance can be simulated using equation 25 for the single level interface states model. The simulation curves by using single level interface state model and the parameters extracted from the conductance method are in agreement with the experimental curves for the bias range -4V $\leq V_G \leq -8V$[15], as depicted in Fig. 7a). We conclude that the single level interface state model is sufficient to describe the interface states at the O-diamond/Al_2O_3 interface. Similar results are also obtained for sample #2. The origin of the interface states is not known at the moment. However, the excess dangling bonds at diamond surface is a good candidate. Nevertheless, the interface states density of $10^{12}\,(eV^{-1}.cm^{-2})$ is not so high. Even if the optimization of the oxide interface with O-diamond is needed, the gap to fill for diamond devices fabrication is reasonable.

VI. CAPACITANCE-FREQUENCY DEPENDENCE

This section is dedicated to reproduce the capacitance-frequency characteristic of the O-diamond MOSCAPs by using the small-signal equivalent circuit introduced in the previous section (Figure 5b). The impedance simulation is performed with LTSPICE software.

One can note that all the parameters of the equivalent circuit have been experimentally extracted. The oxide capacitance C_{ox} was measured by using the MIMCAP. The semiconductor capacitance $C_{sc}\,(V_G)$ was evaluated from MOSCAP capacitance measurements at "middle frequency regime"(f = 100 kHz), as described in section III. Series resistance R_s can be determined from the "real part" of impedance measurements in the "high frequency regime" $f = 1$ MHz[15]. The DC conductance is obtained from the statics I-V characteristics of the test device by using $G_{dc} = \frac{dI_{dc}}{dV_{dc}}$. It must be noticed that $G_{dc}\,(\omega) = G_{ox}\,(\omega) + \frac{1}{R_{it}}$ is frequency dependent due to the hopping process which is represented by $G_{ox}\,(\omega)$. However, from MIMCAP measurements, a negligible frequency dependence was measured in this fre-

	MIM	HF MOS	G_p/ω	τ_{it}	DC I-V
V_G(V)	C_{ox}(pF)	C_{sc}(pF)	C_{it}(pF)	R_{it}(MΩ)	$G_{dc}(\mu S)$
-8	70.8	35.8	24.2	2.6	0.64
-7	70.8	31.2	15.7	4.07	0.50
-6	70.8	26	20.9	4.8	0.33
-5	70.8	18.2	23.5	10.7	0.153
-4	70.8	13.36	32.2	19.68	0.05

TABLE II. Input parameters for the LTSPICE simulation and the corresponding extraction method.

quency range. The G_{ox} variation from MIMCAP is lower than 10 nS for frequencies ranging from $1Hz$ to $1kHz$[15]. Finally, interface states capacitance C_{it} and interface states resistance R_{it} were evaluated by conductance method $\left(\frac{G_P}{\omega}\right)$ with $C_{it} = 2\left(\frac{G_P}{\omega}\right)_{\max}$ and $R_{it} = \frac{\tau_R}{C_{it}}$ where τ_R is extracted at $\left(\frac{G_P}{\omega}\right)_{\max}$.

Table II summarizes the parameters extracted by various methods at different gate bias for the impedance simulation.

The LTSPICE simulation results are plotted in Fig. 8 along with the capacitance-frequency dependent curves measured from MOS 12 - sample #1. The simulations using the proposed equivalent circuit and all extracted parameters reproduce very accurately the measured capacitance-frequency dependence of the O-diamond MOSCAP. We conclude that the capacitance-frequency dependence of the O-diamond MOSCAPs is originated from the complex charge transfer process from metal to oxide and recombination with diamond valence band at the interface states.

In summary, the comprehensive electrical characterization, analysis and simulations have demonstrated that the complex charge transfer process from metal gate to gate oxide, traps to traps hopping in bulk oxide and the interface/valence band recombination fully explains the parasitic leakage currents, FLPE and capacitance-frequency dependence observed in the O-diamond MOSCAPs. Therefore, in order to eliminate these drawbacks, it is very important to improve the oxide crystallinity, to increase the oxide thickness, to decrease the hopping rate and to improve the interface of the O-diamond/Al_2O_3 interface.

VII. CONCLUSION

In summary, the comprehensive electrical characterization, analysis and simulations have demonstrated that the complex charge transfer process from metal gate to gate oxide, traps to traps hopping in bulk oxide and the interface/valence band recombination are consistently the reasons for the parasitic leakage currents, FLPE and capacitance-frequency dependence observed in the O-diamond MOSCAPs. Thanks to this complete understanding, we established a method that allows the determination of all the physical mechanisms and associated parameters in gate controlled O-diamond MOSCAPs. This will open a route toward gate controlled diamond MOS devices for power electronic applications.

ACKNOWLEDGMENTS

T.T.PHAM acknowledges the AGIR 2013-2016 project from Institut polytechnique de Grenoble for the PhD funding. Part of the research leading to these results has been performed within the GreenDiamond project (http://greendiamond-project.eu/) and received funding from the European Communitys Horizon 2020 Programme (H2020/2014-2020) under grant agreement n 640947. The authors acknowledge Chloé Rivière (Institut NEEL) for fruitful discussions.

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FIG. 1. Structure of the test device that includes ohmic contact, MIMCAPs and MOSCAP a) Cross-section; b) Top view.

FIG. 2. Typical electrical characteristics of O-diamond MOSCAPs. Data shown here is measured from MOSC7, sample #2 (surface area A=1.77×10^{-4} cm^2): a) I(V) characteristics; b) C(V) characteristics measured at different frequency, ranging from 1 kHz to 1 MHz; d) C(f) characteristics measured by fixing gate bias at V_G=0V, -2V, -4 V and -6V and sweeping frequency from 1 Hz to 1 MHz.

FIG. 3. Proper C(V) measurement indicates that diamond are in depletion regime even for $V_G = -8V$. Doping concentration of diamond epilayer is extracted from $\frac{1}{C^2}(V_G)$ curve (MOS12 - sample #1).

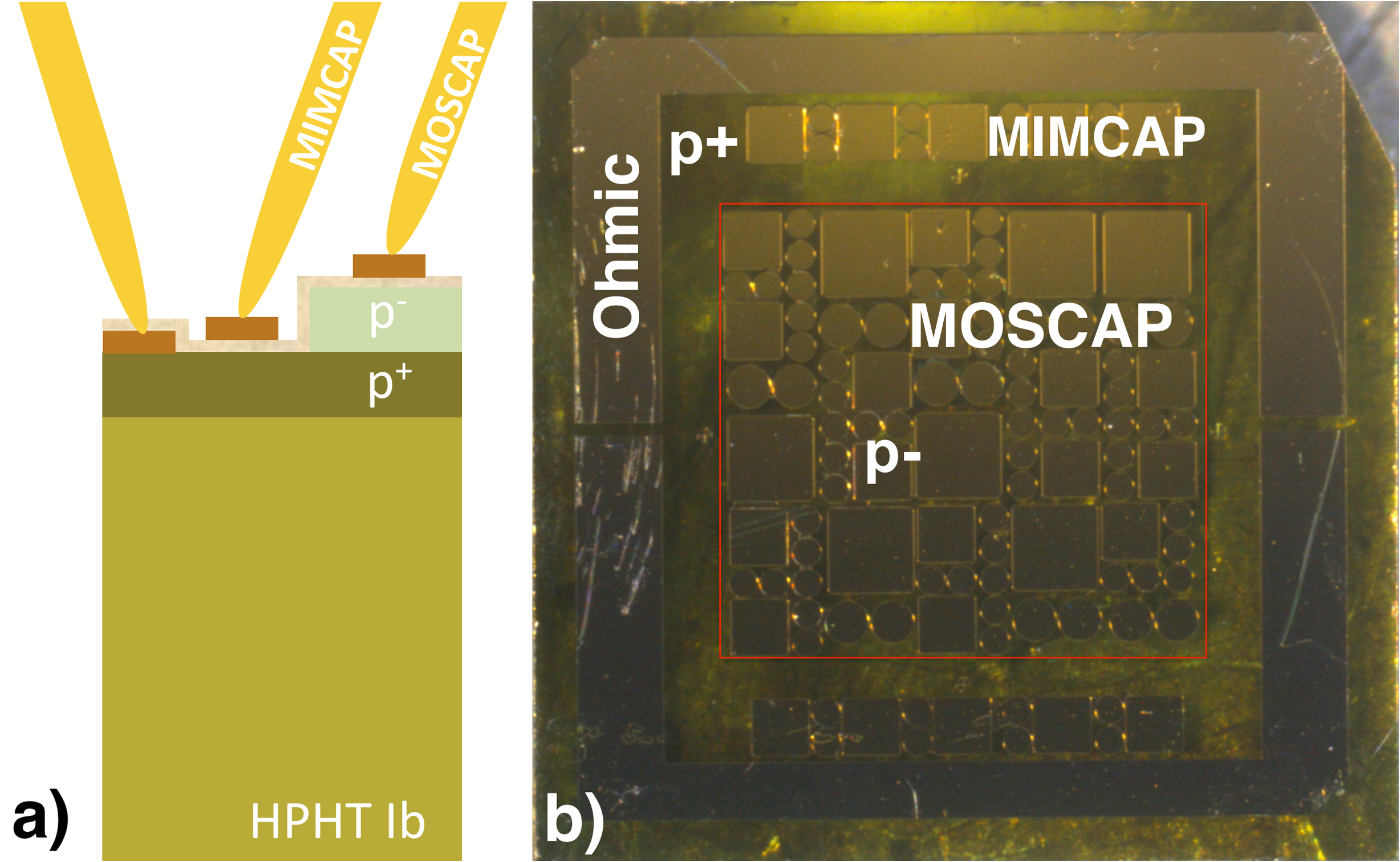
FIG. 4. (a) Finite element calculation of MOSCAP band diagram under negative gate bias $V_G = -5V$. The arrows illustrate the proposed current path mechanism including five steps: I. Electron tunneling from metal gate electrode to oxide gate, II. Hopping from traps to traps in the oxide, III. Recombination to surface trap states, IV. Electron from surface states emit to valence band or hole from valence band captured to interface states, V. Carriers drift in diamond epilayer to the back gate contact. (b) Equivalent circuit of a MOSCAP without interface states and leakage current; (c) Equivalent circuit including interface states and a gate oxide without leakage current (d) Equivalent circuit where the injected carriers from metal to interface states and the charges transfer between interface states and valence band are taken into account.

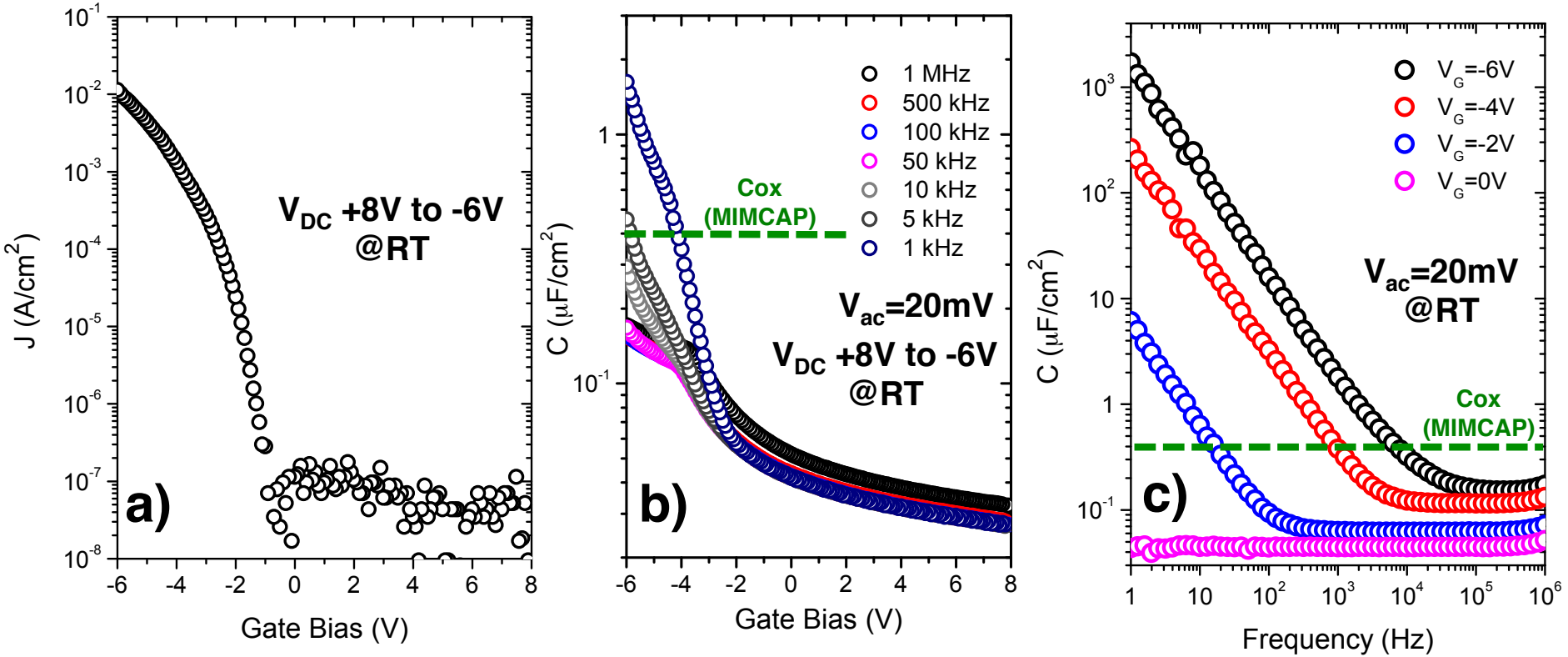
FIG. 6. (a) Experimental log-log plot I(V) characteristics of the low injection MOSCAP (MOS 50 - Sample #1). (b) Arrhenius plot current density versus Temperature at different gate bias: V_G=-8V, -6V and -4V, indicates the thermal activation energy of the low injection MOSCAP. (c) Log-log plot I(V) characteristics of high injection MOSCAP (MOS1-sample #1); (d) Current density at $V_G = -8V$ versus versus $\frac{1}{T^4}$ indicates the variable range hopping in the high injection MOSCAP.

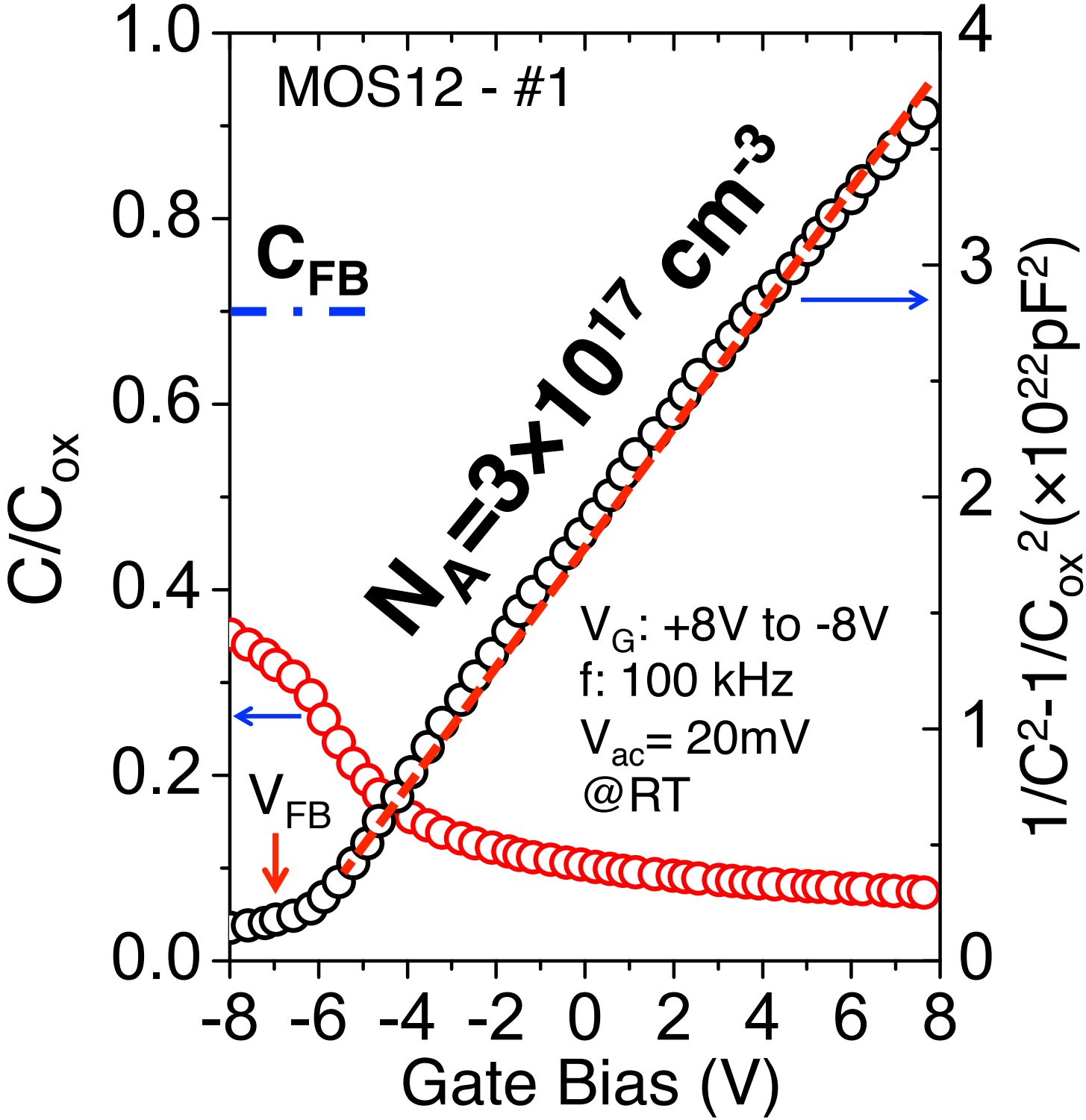
FIG. 5. Equivalent circuit for the O-diamond MOSCAP corresponding to the approximation: (a) approximate equivalent circuit for the interface states recombination limited case ($\tau_R >> \tau_T$) where $G_{it} = \frac{1}{R_{it}}$; (b) approximated equivalent circuit for the oxide tunneling limited case ($\tau_T >> \tau_R$) where $G_{dc} \approx G_{ox}$.; (c) Circuit (b) transformed to include a continuum of interface states.; (d) Circuit (c) transformed to show capacitance corrected for series resistance (C_c) and the a.c. conductance (G_{ac}); (e) Circuit (d) transformed to show C_c and conductance corrected for series resistance (G_c): (f) Circuit (e) transformed to show measured capacitance (C_p) and measured conductance (G_p):

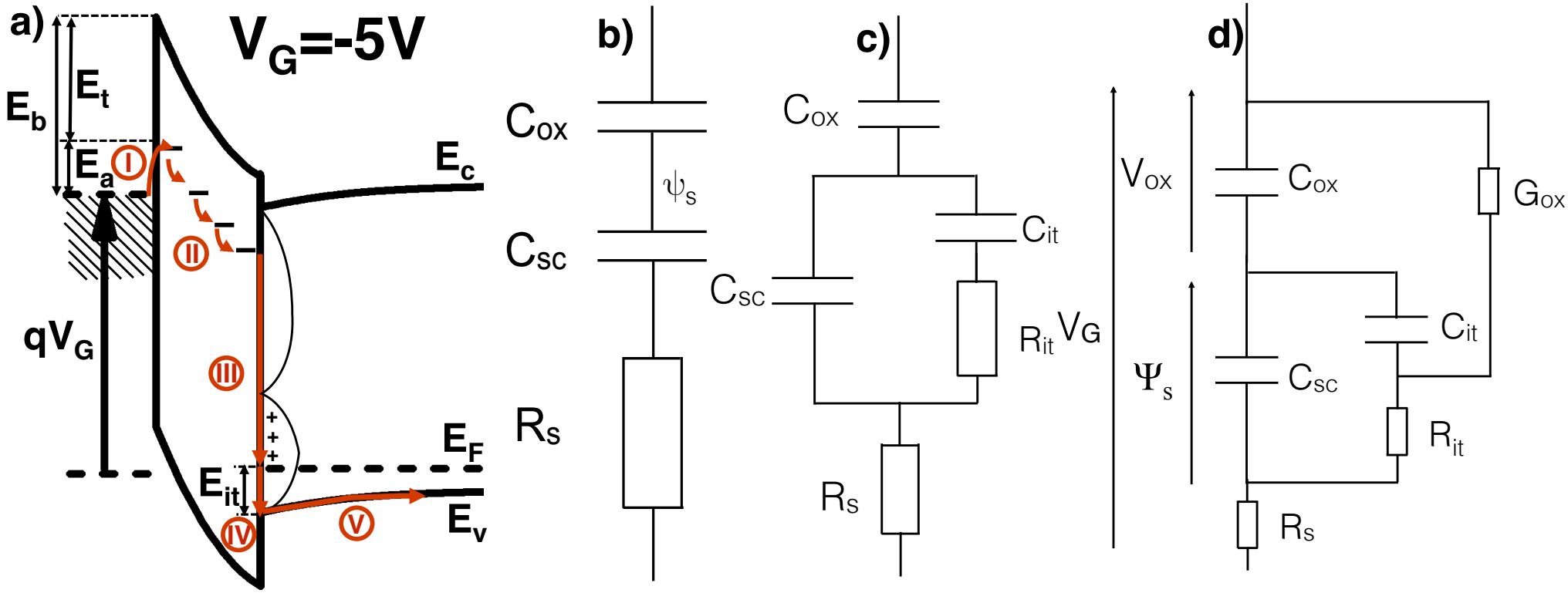
FIG. 7. (a) Equivalent conductance G_p/ω at different gate bias ranging from -4V$\leq V_G \leq -8V$ of the MOS 12 - Sample #1, measured at RT. The single level interface state model is employed to simulate the equivalent conductance and demonstrate a good agreement; (b) Interface states density at O-diamond/Al_2O_3 interface measured by conductance method (open red circle curve) and by Terman method (open black circle curve).

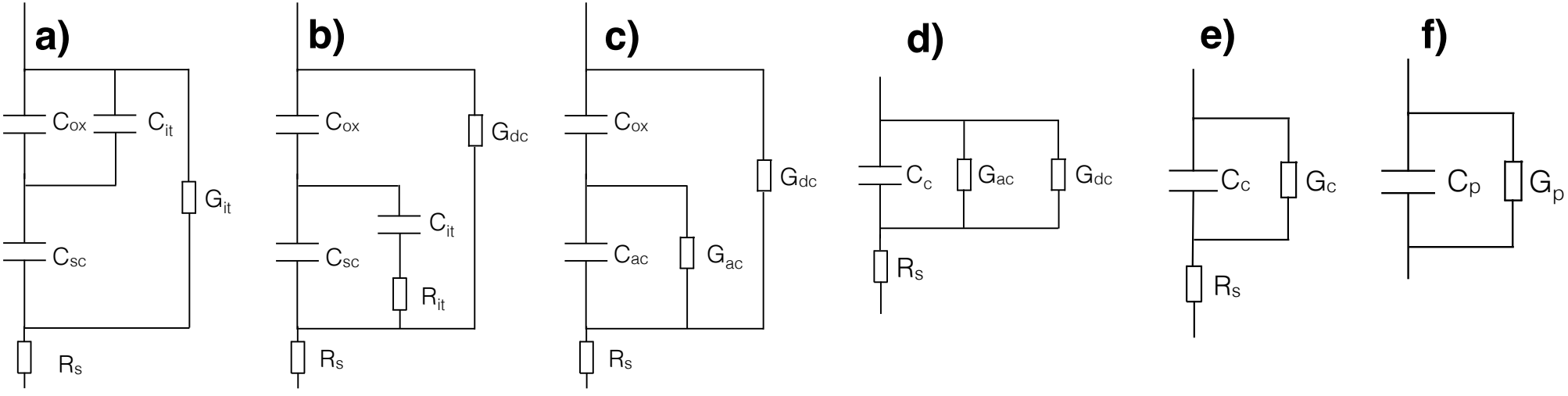
FIG. 8. Measured Capacitance-frequency dependence of the MOSCAP test device is reproduced by LTspice simulation with all the parameters extracted experimentally.

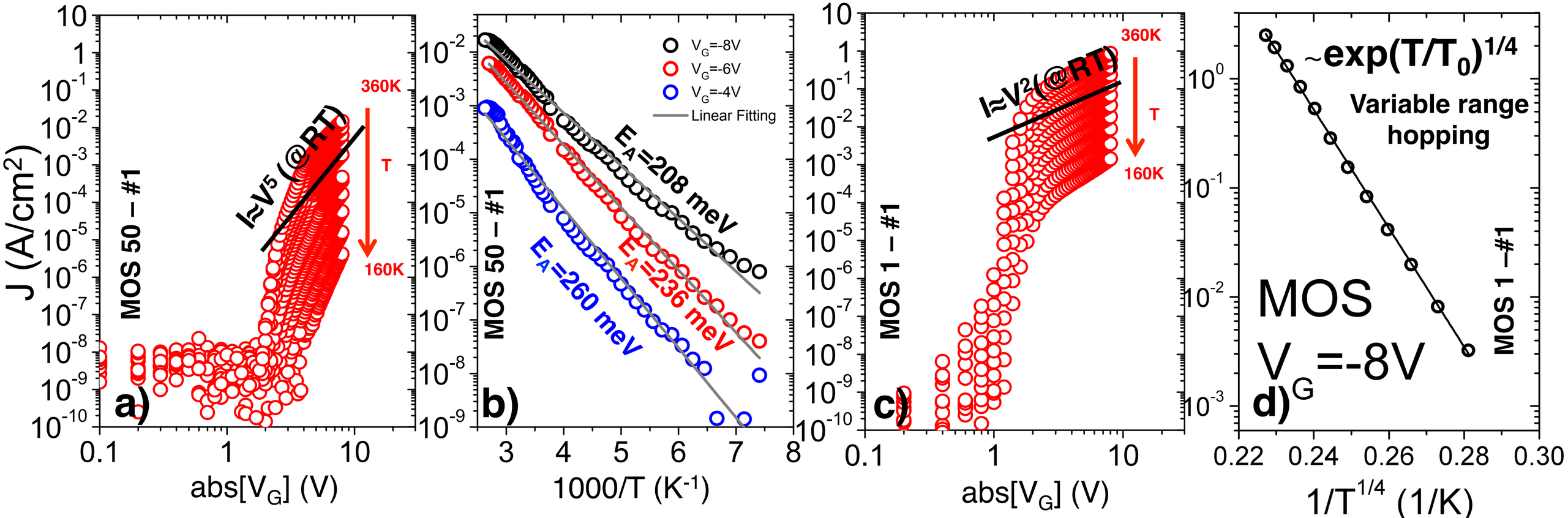

MIMCAP
MOSCAP
p-
p+
HPHT Ib
a)
Ohmic
p+
MIMCAP
MOSCAP
p-
b)

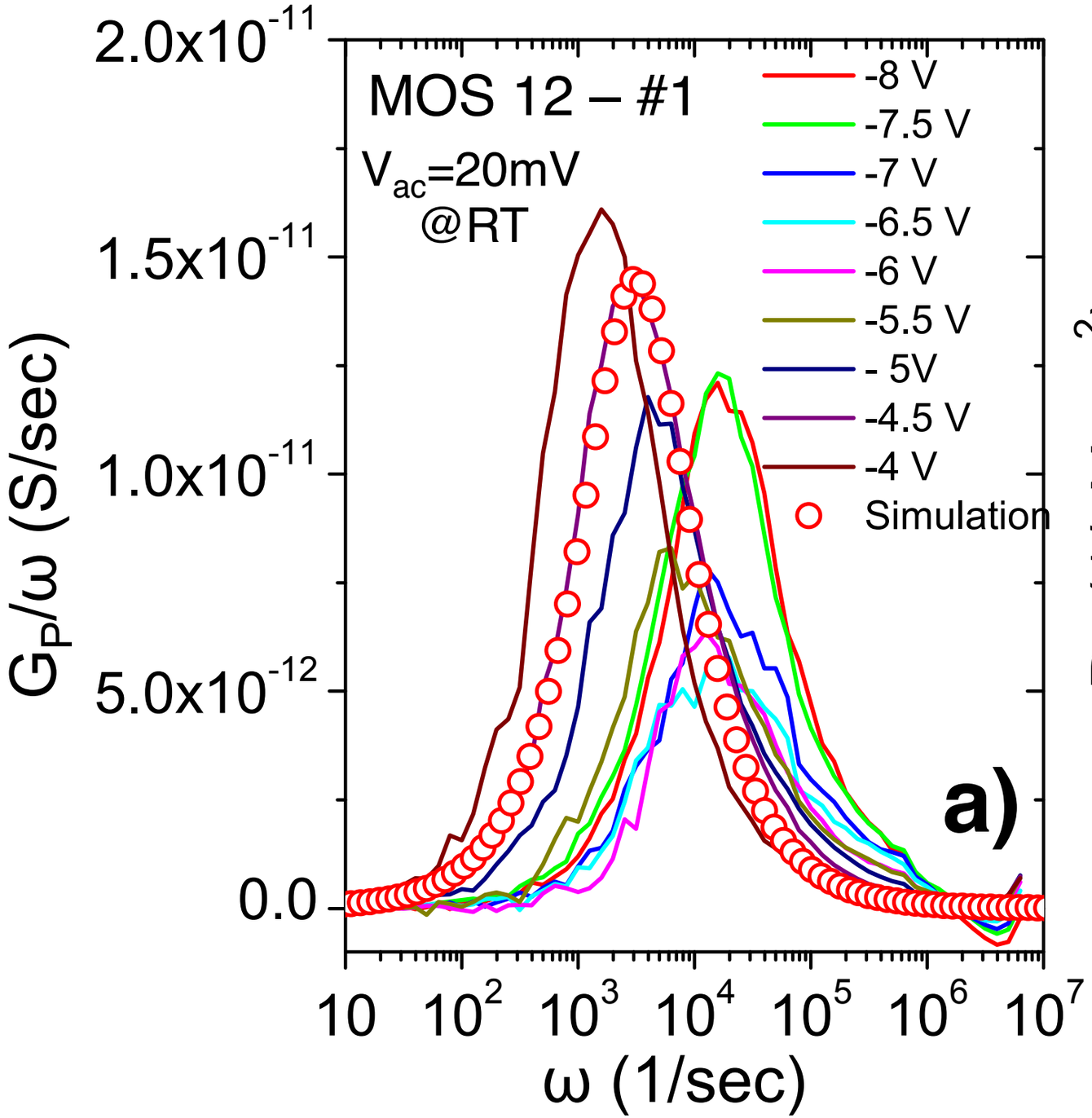

a)
J (A/cm^2)
Gate Bias (V)
V_{DC} +8V to -6V
@RT
b)
C (μF/cm^2)
Gate Bias (V)
1 MHz
500 kHz
100 kHz
50 kHz
10 kHz
5 kHz
1 kHz
Cox
(MIMCAP)
V_{ac}=20mV
V_{DC} +8V to -6V
@RT
c)
C (μF/cm^2)
Frequency (Hz)
V_G=-6V
V_G=-4V
V_G=-2V
V_G=0V
V_{ac}=20mV
@RT
Cox
(MIMCAP)

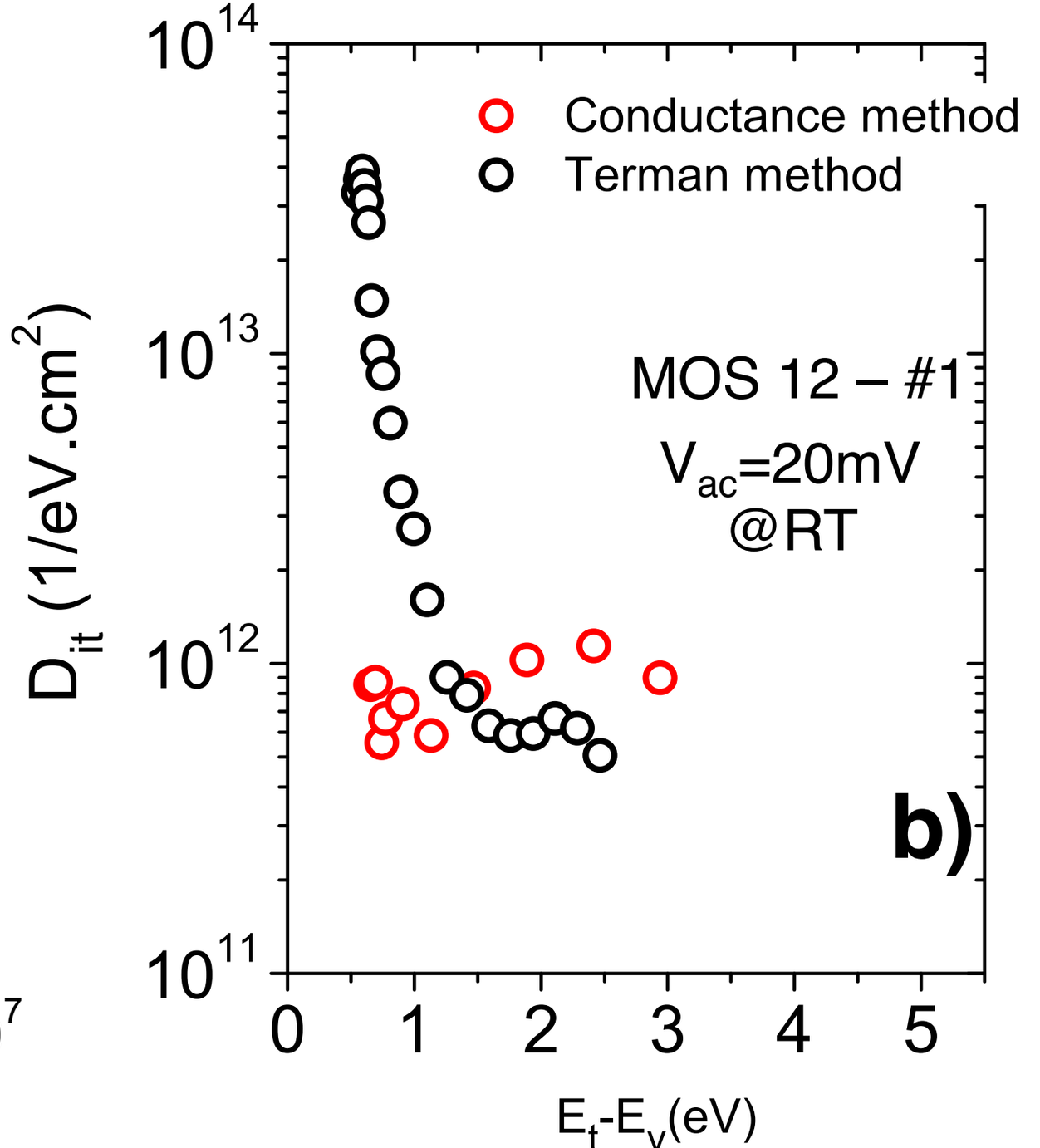

MOS12 - #1
C_{FB}
N_A=3x10^{17} cm^{-3}
V_G: +8V to -8V
f: 100 kHz
V_{ac}= 20mV
@RT
V_{FB}
C/C$_{ox}$
1/C^2-1/C$_{ox}^2$(x10^{22}pF^2)
Gate Bias (V)
1.0
0.8
0.6
0.4
0.2
0.0
4
3
2
1
0
-8
-6
-4
-2
0
2
4
6
8

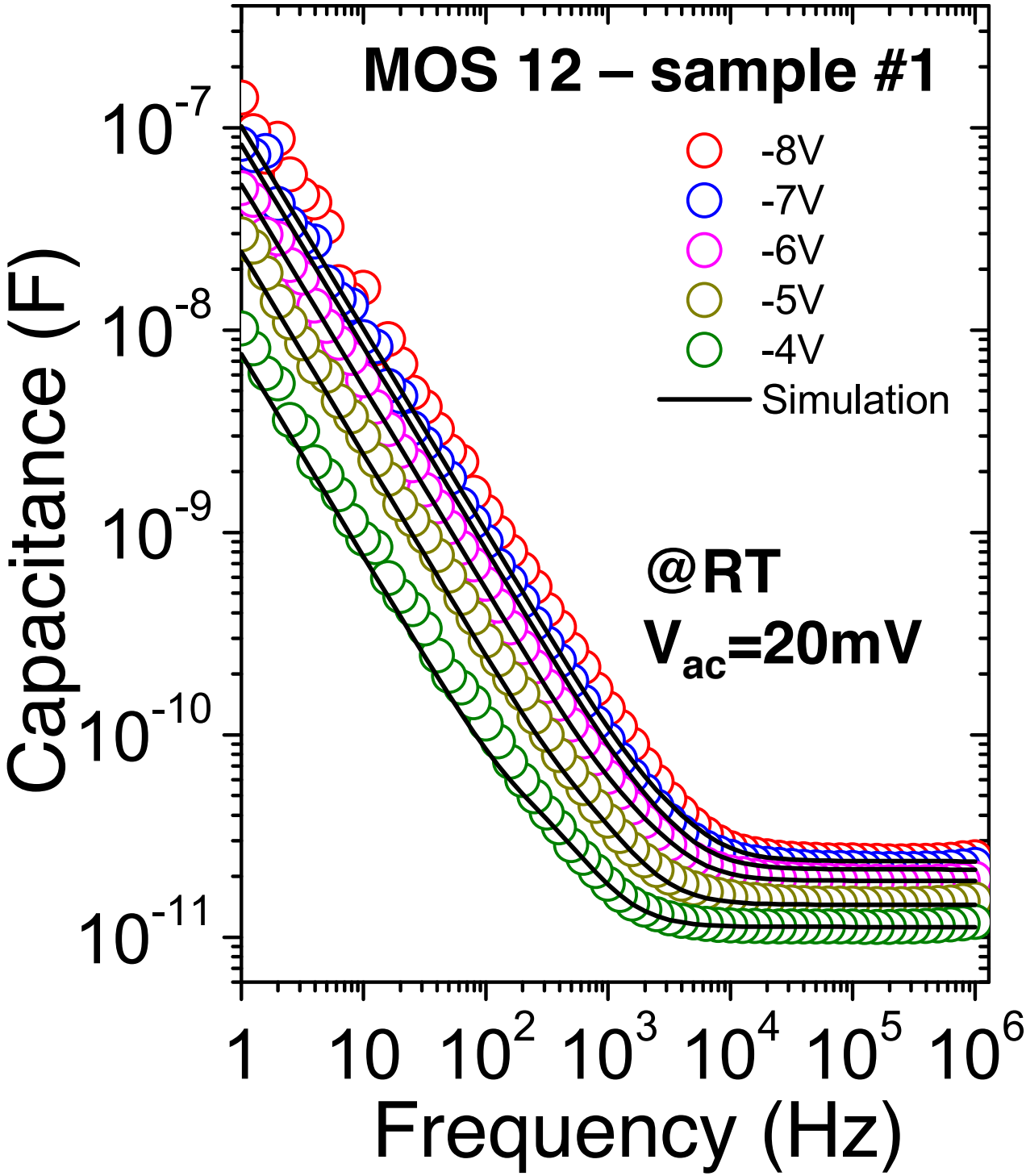

a)
V_G=-5V
E_b
E_t
E_a
I
II
III
IV
V
E_c
qV_G
E_F
E_{it}
E_v
b)
C_{ox}
ψ_s
C_{sc}
R_s
c)
C_{ox}
C_{it}
C_{sc}
R_{it}
V_G
R_s
d)
V_{ox}
C_{ox}
G_{ox}
C_{it}
Ψ_s
C_{sc}
R_{it}
R_s


a)
Cox
Cit
Git
Csc
Rs
b)
Cox
Gdc
Cit
Csc
Rit
Rs
c)
Cox
Gdc
Cac
Gac
Rs
d)
Cc
Gac
Gdc
Rs
e)
Cc
Gc
Rs
f)
Cp
Gp


a)
MOS 50 – #1
I≈V⁵ (@RT)
360K
T
160K
J (A/cm²)
abs[V_G] (V)
b)
MOS 50 – #1
V_G=-8V
V_G=-6V
V_G=-4V
Linear Fitting
E_A=208 meV
E_A=236 meV
E_A=260 meV
1000/T (K⁻¹)
c)
MOS 1 – #1
I≈V²(@RT)
360K
T
160K
abs[V_G] (V)
d)
~exp(T/T_0)^1/4
Variable range hopping
MOS
V_G=-8V
MOS 1 –#1
1/T^1/4 (1/K)


MOS 12 – #1
V_{ac}=20mV
@RT
-8 V
-7.5 V
-7 V
-6.5 V
-6 V
-5.5 V
- 5V
-4.5 V
-4 V
Simulation
a)
G_P/ω (S/sec)
ω (1/sec)
2.0x10^{-11}
1.5x10^{-11}
1.0x10^{-11}
5.0x10^{-12}
0.0
10
10^2
10^3
10^4
10^5
10^6
10^7


Conductance method
Terman method
MOS 12 – #1
V_{ac}=20mV
@RT
b)
D_{it} (1/eV.cm^2)
E_t-E_v(eV)
10^{14}
10^{13}
10^{12}
10^{11}
0
1
2
3
4
5


MOS 12 – sample #1
-8V
-7V
-6V
-5V
-4V
Simulation
@RT
V_{ac}=20mV
Capacitance (F)
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
1
10
10^2
10^3
10^4
10^5
10^6
Frequency (Hz)