

Top-down 3C-SiC NWFETs

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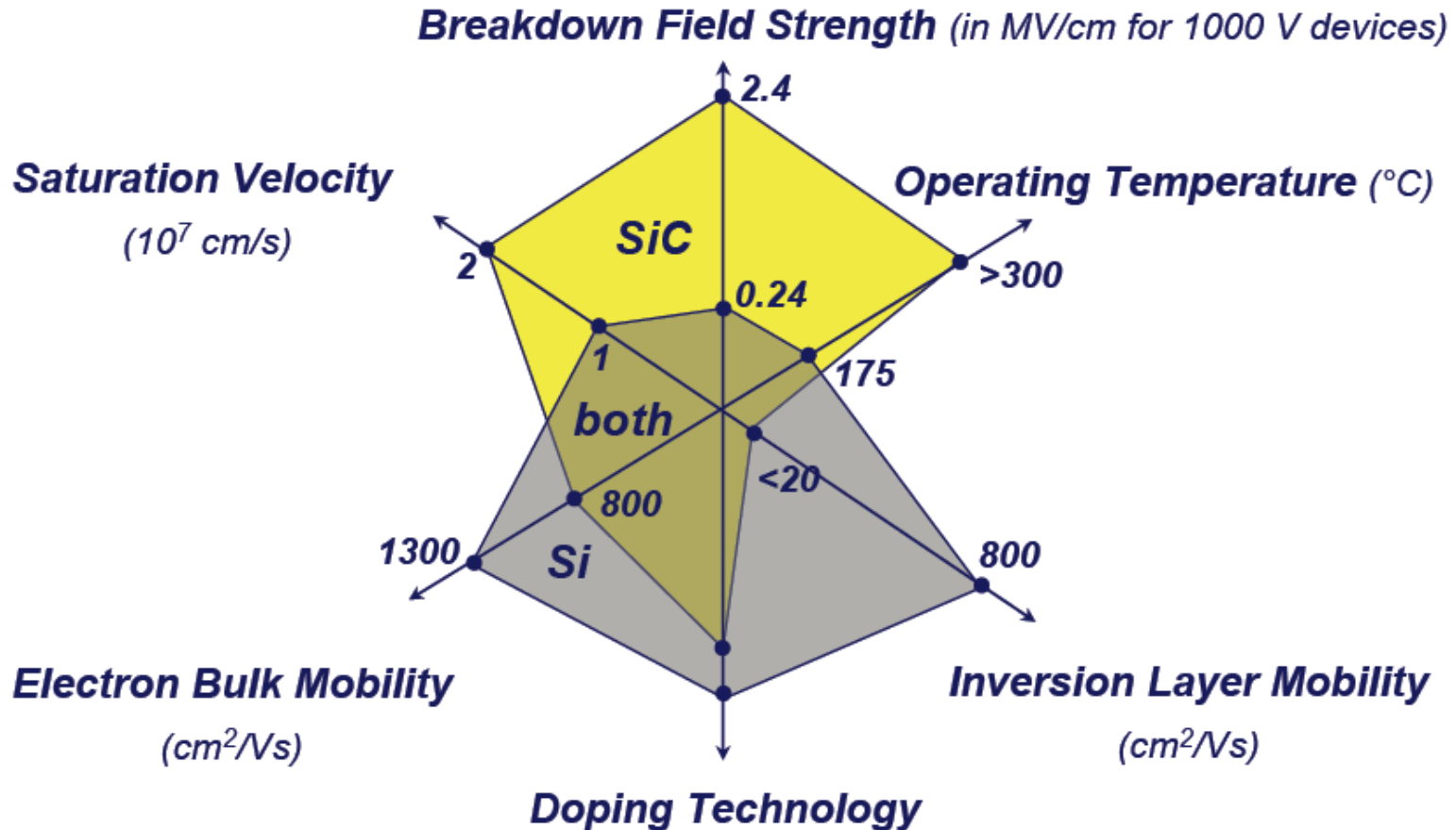
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Interest for NWs

- **1D nanostructures:** smallest dimension structure that can efficiently transport electrical carriers
- **1D transport:** New device concepts with enhanced performance (lower capacitance, higher mobility)
- **NWs:** interconnects and/or active components
- **1D channel transistors:** better electrostatic control, higher packing density, 3-D integration.
- **High surface to volume/aspect ratio:** new physical properties (optical, thermodynamic), higher sensitivity of functionalized surfaces.



Interest for SiC



- **In addition:** native SiO₂, high value of λ , chemical inertness and increased biocompatibility.

Interest for SiC NWs

- **Combination of NWs and SiC properties**

High-temperature sensors

Field emission displays (as cathodes)

Biosensors

High temperature (“operating voltage”) FETs

- **SiC NWFETs with increased operation temperature can substantially increase packing density.**

Simulation of 3C-SiC & Si-based NWFETs

- Simulations for the following transport regimes:

Ballistic ($d=3\text{nm}$, $l=9\text{nm}$)

Strong confinement ($d=6\text{nm}$, $l=20\text{nm}$)

Drift-diffusion ($d=10\text{nm}$, $l=200-700\text{nm}$ / $d=20-100\text{nm}$, $l=0.5-4\mu\text{m}$)

K Rogdakis et al Nanotechnology 20 (2009) 295202

K. Rogdakis et al IEEE Trans. Electron Dev., 55 (2008) p. 1970

K. Rogdakis et al Nanotechnology 18 (2007) 475715

Electrical performance of 3C-SiC NWFETs is comparable to that of Si NWFETs

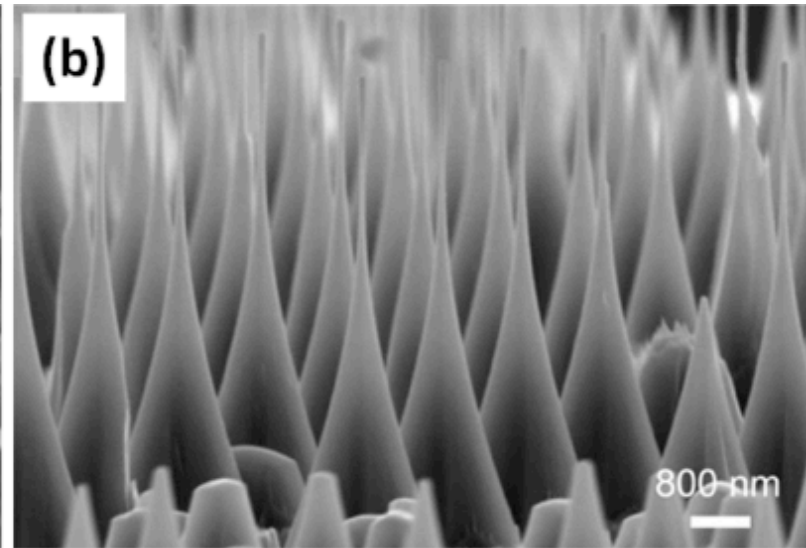
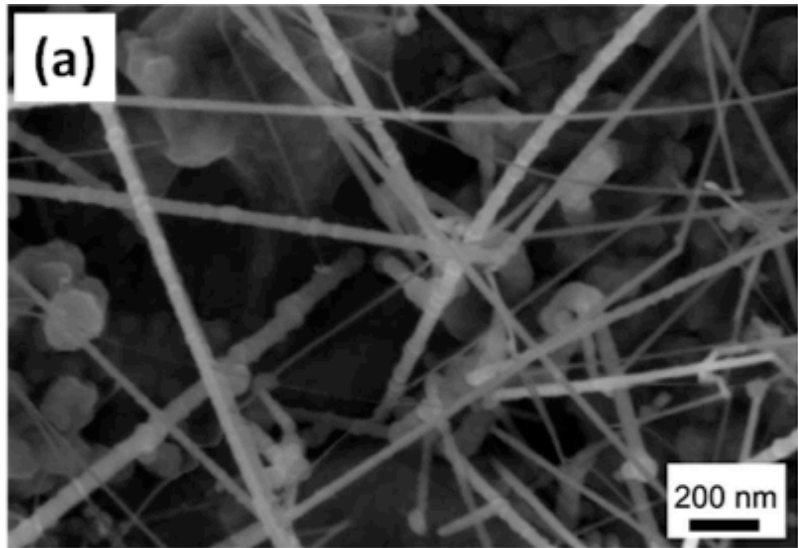
Previous results on bottom-up SiC NWFETs

- **Weak gating effect ($g_m < 1$ nS) and switch-off not achievable.**
- **Proposed explanations: high residual doping and bad interface with gate oxide.**
- **Schottky barrier contact 3C-SiC-NWFETs exhibit better I-Vs for the actual SiC NW quality.**
- **Ohmic contact 3C-SiC-NWFETs anticipated to perform better.**

Interest for top-down SiC NWFETs

- Starting from good crystalline material.
- More compatible with microelectronics fabrication.
- Require good control of plasma etching.
- **Purpose of the study:** Compare bottom-up and top-down SiC NWFETs

SiC NW fabrication



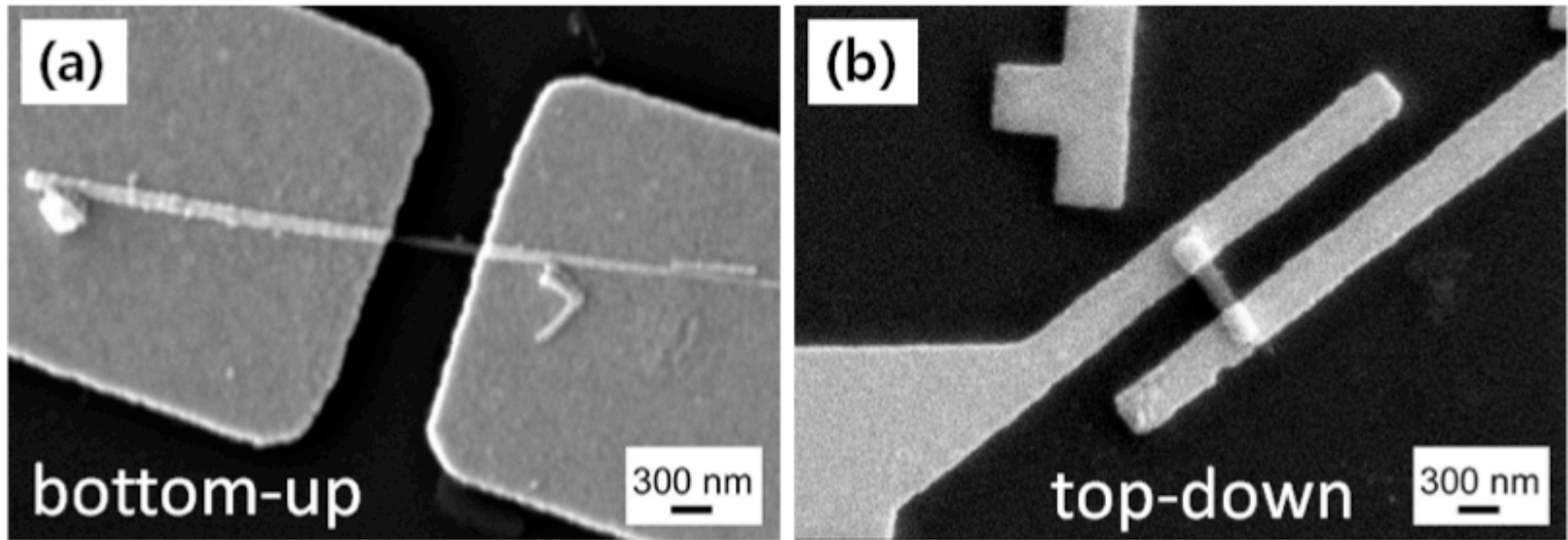
Bottom-up approach (Fig. a)

- VLS growth in CVD reactor.
- Removed, diluted in ethanol, ultrasonic.

Top-down approach (Fig. b)

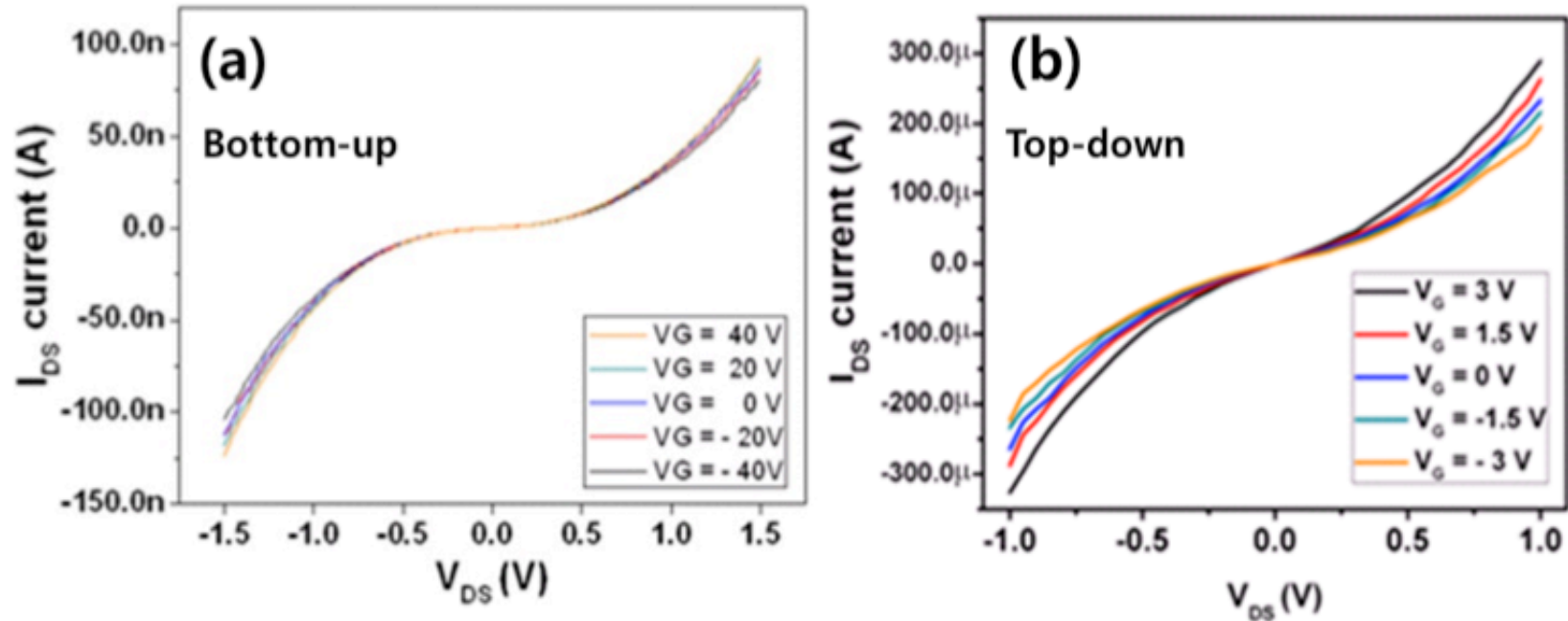
- ICP of 3C-SiC epis on Si (100).
- Tapered shape: mask lateral etch.
- Tip removal by sonication in IPA solution.

Back-gated transistor fabrication



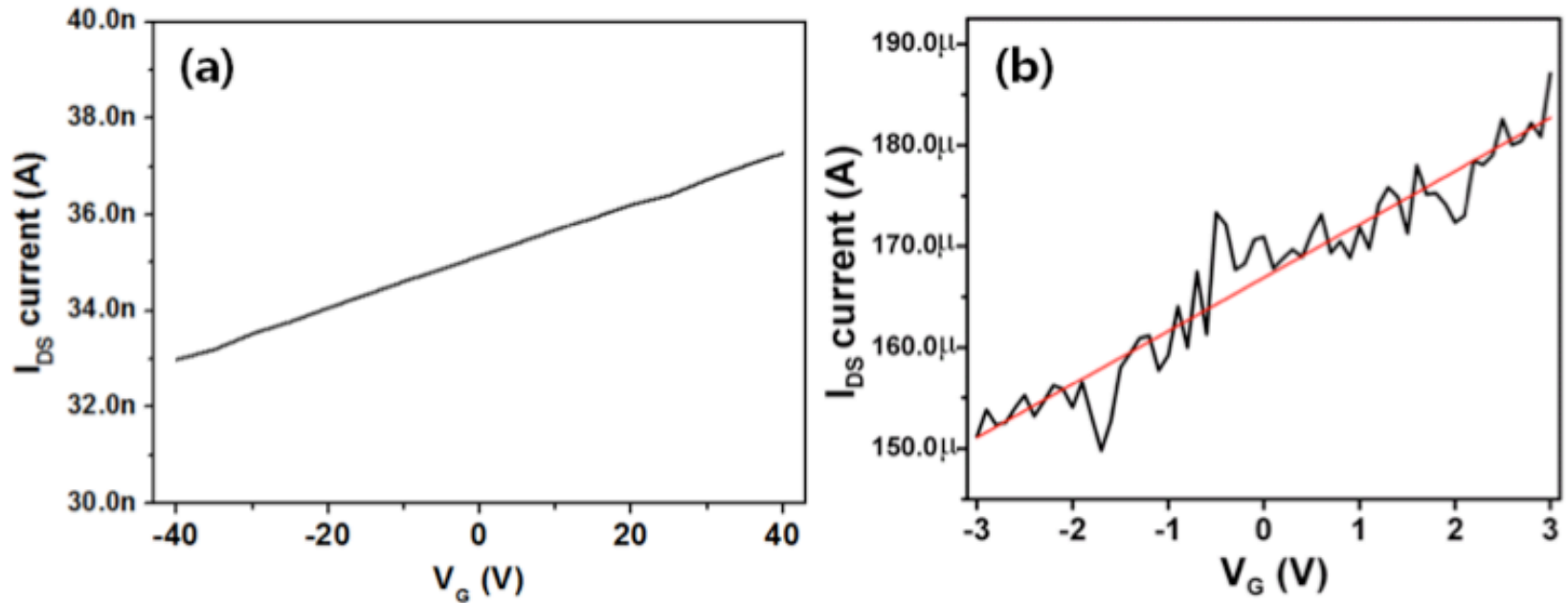
- Same process for bottom-up (Fig.a) & top-down (Fig.b).
- Si/SiO₂ substrate on which metal interconnect lines to pads are formed.
- NW dispersion and AFM-based location.
- E-beam top contacts between NW & interconnects.

SiC NWFETs characterization (1)



- **Three orders of magnitude higher current for top-down transistors.**

SiC NWFETs characterization (2)



- $g_m = 0.05$ nS (bottom-up) 5.3 μ S (top-down)
- Both transistors do not switch-off.

Extracted parameters

	C'_{ox}	μ' ($\text{cm}^{-2} \cdot \text{V}^{-1} \text{s}^{-1}$)	Doping density (cm^{-3})
Bottom-up SiC NWFET	0.02 fF	0.03	Estimated: 2.92×10^{19}
Top-down SiC NWFET	0.05 fF	411.6	Measured: 5×10^{16}

- **The material quality (mobility, carrier density) of top-down NWs is not responsible for the non switching-off.**
=> Interface with dielectric has to be improved.

Conclusions

- **Top-down SiC NWFETs exhibited increased output currents and transconductance value than their bottom-up counterparts.**
- **Improvement due to channel doping control: residual for bottom-up and epi-growth controlled for top-down.**
- **To further improve the device performance of NWFET, it is strongly needed to control the gate dielectric/NW channel interface.**
- **Towards this purpose a NW embedded top-gate geometry and eventually reliable high-k material deposition are necessary.**

Acknowledgments

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Thank you for your attention!

