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Power Modeling for Fast & Early Power Estimation of FPGA-based Communications Systems

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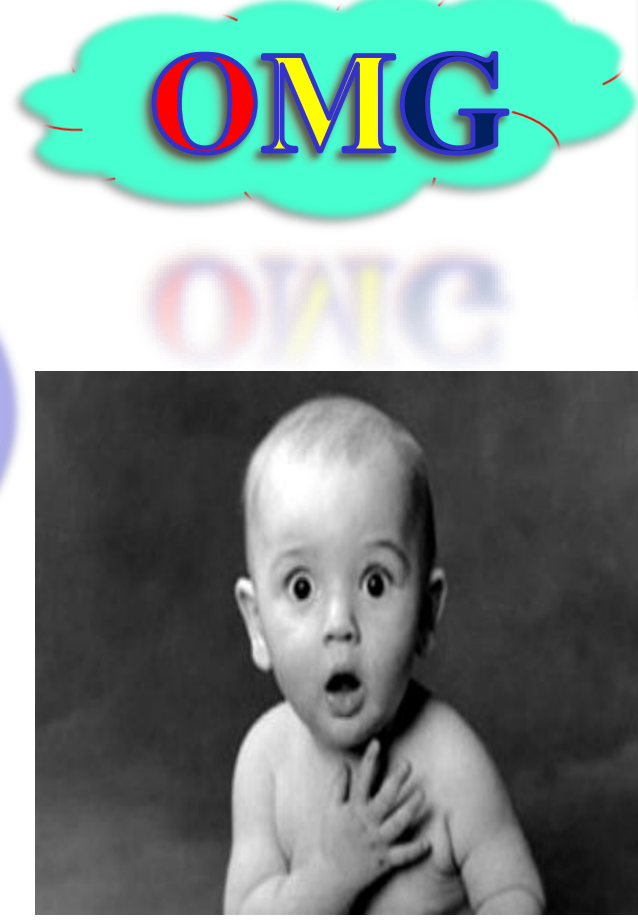
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1. Background

- Communicating devices are widespread
- IoT is everywhere
- Forecast: 50 billions devices available by 2020
- Huge impact on the world energy consumption
- FPGAs are parts of these communicating devices
- Energy estimation is a key point

1 Google search = ?
Same energy as 11-watt light bulb for an 1 hr.
Emit 7g CO2
There are 0.4B+ Google searches daily



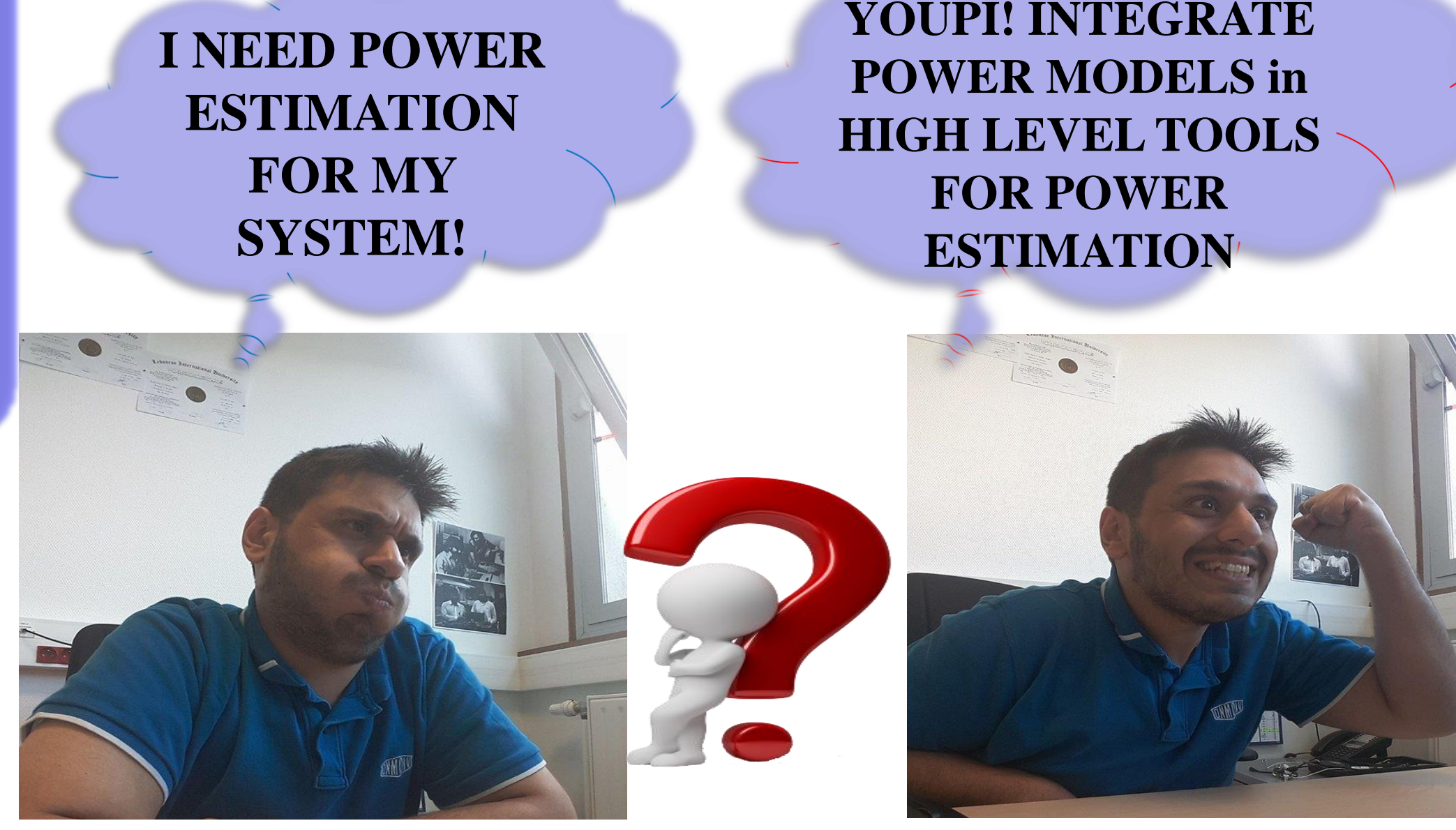
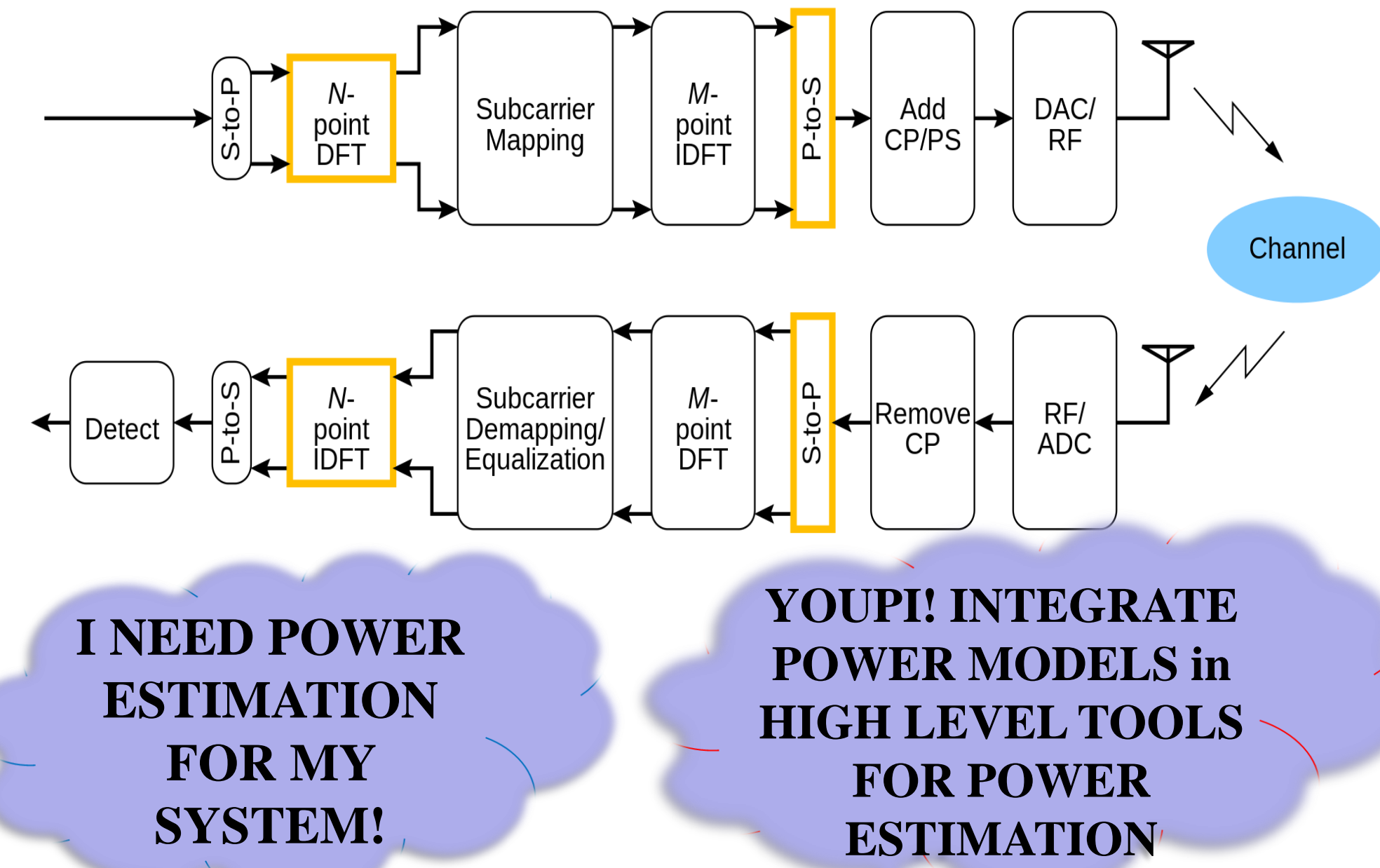
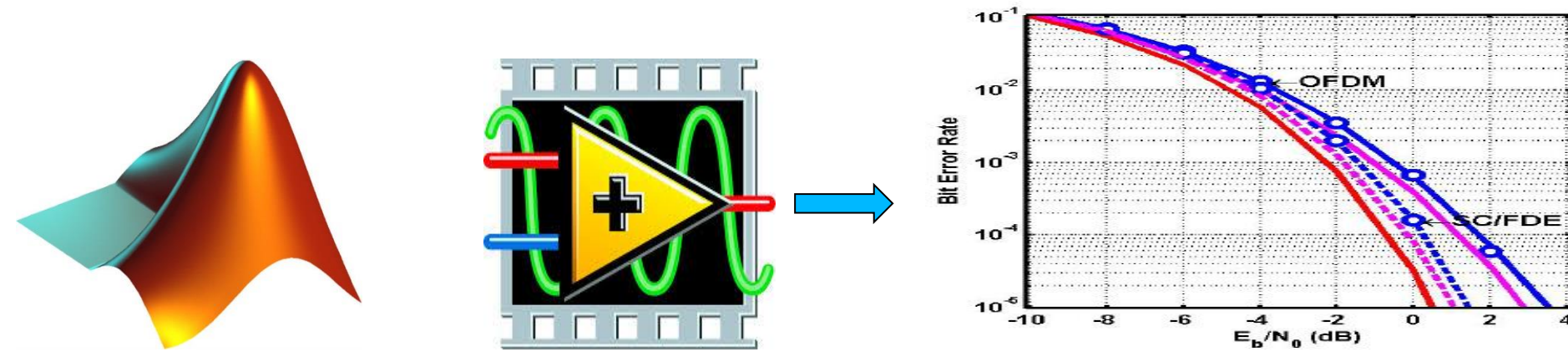
2. Motivation & Goals

Motivation:

- First step toward power reduction is power estimation
- FPGAs: Flexible, low cost & low time-to-market
- FPGAs: Consume 10x more power than ASICs.
- FPGAs: used as a final end product.

Goals:

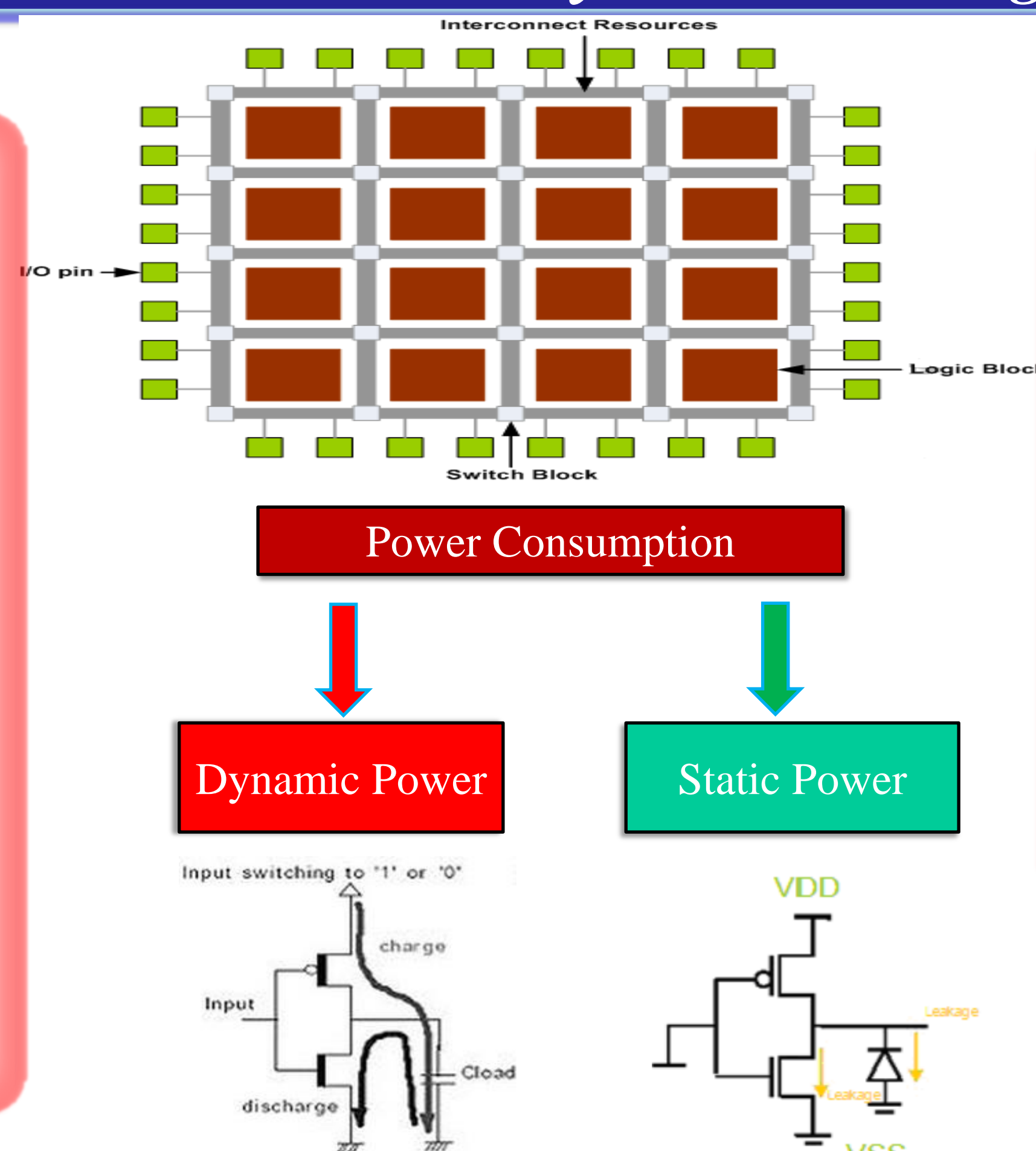
- Design exploration for low power DSP algorithms
- High-Level power estimation strategy
- Accurate, early and fast power estimation



3.1 Theoretical Study

- $P_{Total} = P_{Dyn} + P_{Stat}$
- Static Power is technology dependent.
- Dynamic power is data dependent.
- $P_{Dyn} = SR \cdot C \cdot V^2$
- $SR = Signal Rate = \frac{Number\ of\ transitions(1 \rightarrow 0\ or\ 0 \rightarrow 1)}{T_{clock}}$
- SR is highly correlated to the input patterns.
- P_{Dyn} is highly correlated to the SR
- %high or static probability is the % of logic 1
- $P_{Dyn} = f(SR, \%high)$
- α : Input SR, P: Input static probability
- β : Output SR, h: Output static probability

3. Theoretical Study & Methodology



3.2 Methodology

- Digital system seen as a set of basic operators
- Each operator's power consumption is evaluated according to test_benches
- Use statistical information of the input patterns
- Provide low level power information to high level simulation tool
- Activity propagation throughout all operators for power estimation
- Evaluation of the global power consumption

Power Equation

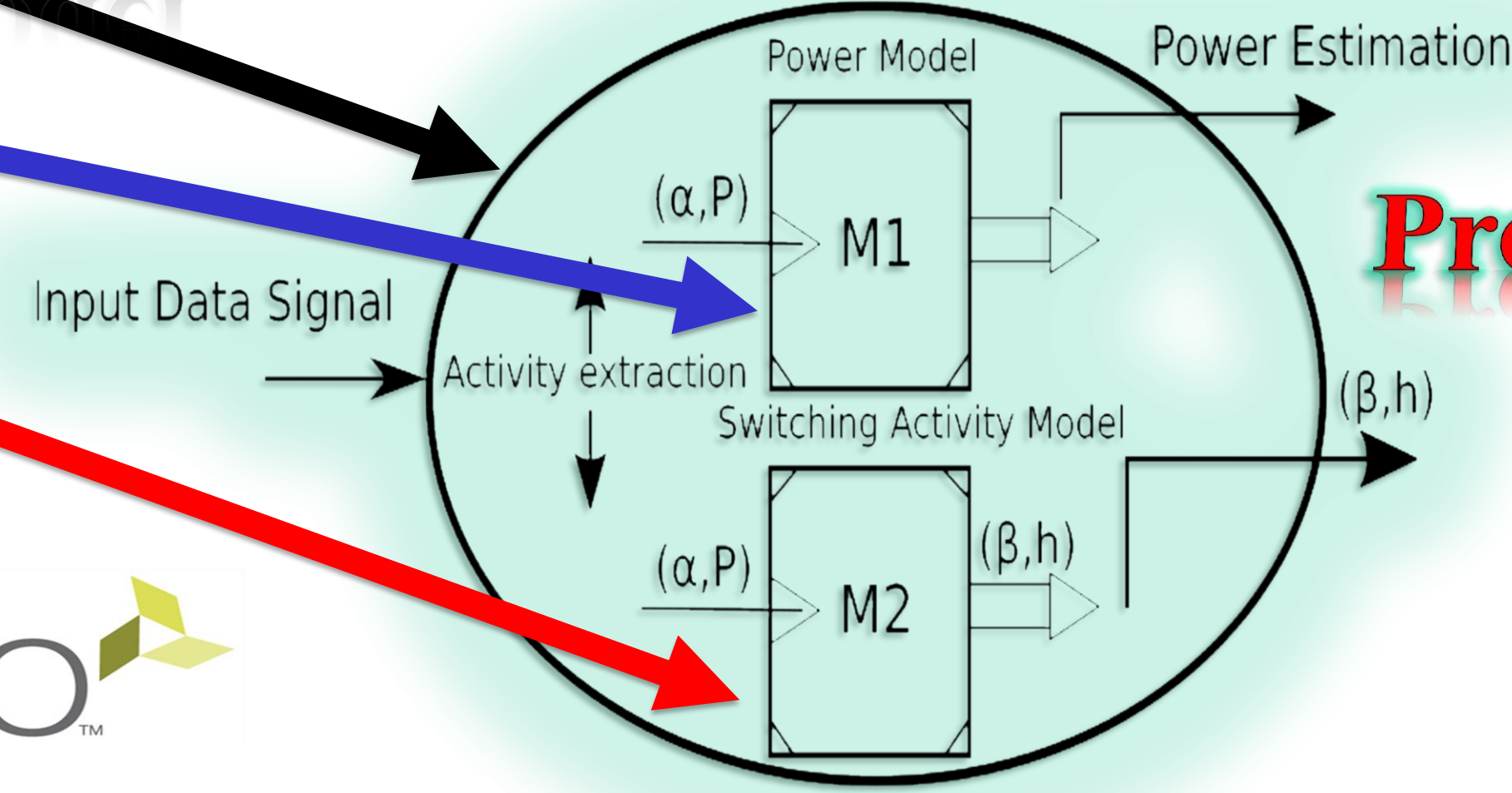
$$P_{Global} = M_{1,1}(\alpha_1, p_1) + \sum_{i=2}^{N-1} M_{1,i}(\beta_{i-1}, h_{i-1})$$

Digital Operator Model

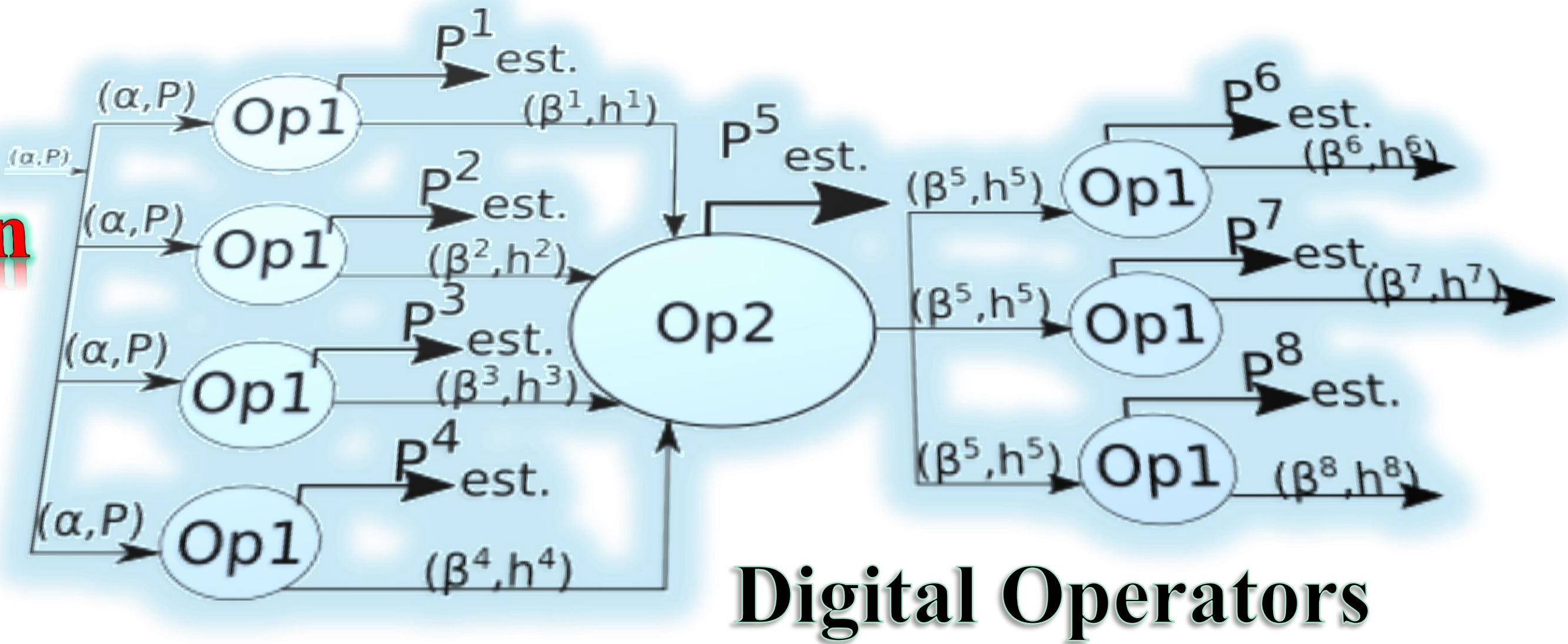
Power characterization

M1: Power Model

M2: SR & %high Model



Propagation



4. Case Study & Results

- Case study: Neural network implemented on FPGA
- Use of MAC (Multiply and accumulate) & Parallel to serial
 - MAC to achieve the multiplication & addition
 - P2S send the data serially to the next MACs
- NN Power Estimation (Vivado) : $P = 239mW$
- Our Methodology : $P = 221mW$
- Vivado based on default toggle rate : $P = 166mW$
- Error :
 - 8% (comparing to our Methodology)
 - 30,5% (comparing to default toggle rate)



5. Conclusion & Future Work

- Methodology for fast & accurate power :
 - Low level characterization of operators
 - Fast high-level simulation
- Exploration of communication system design
 - Speed up of the design process
 - Test of multiple scenarios for power assessment
- Library of predefined operators
- As Future work
 - Generalization to other FPGA families
 - Take real measurements into consideration



I AM READY TO WORK HARD FOR THE FUTURE