# A new methodology to build the Internal Activity Block of ICEM-CE for complex Integrated Circuits

Chaimae Ghfiri, Alexandre Boyer, André Durier, Sonia Ben Dhia

# A new Methodology to build the Internal Activity Block of ICEM-CE for complex Integrated Circuits

C. Ghfiri, A. Boyer, A. Durier, S. Ben Dhia, *Member, IEEE*

***Abstract*—End-users of integrated circuits need models to anticipate and solve conducted emission issues at board level in a short time. The standard IEC62433-2 ICEM-CE has been proposed to respond to this demand. Although the standard proposes methods to extract circuit models from measurements, they cannot provide activity dependent models and may lead to inaccurate results for large and complex circuits. This paper describes a new methodology of construction of the internal activity block of an ICEM-CE model adapted to large digital integrated circuits and validated on a FPGA. The method is based on a predictive approach using the estimation tools of the dynamic power and the data path delays proposed by the manufacturer of the integrated circuit.**

***Index Terms*— Integrated circuits, conducted emission, modeling, internal activity, ICEM-CE standard, FPGA.**

## I. Introduction

INTEGRATED circuits (IC), such as microprocessors, system-on-chips (SoC) or Field-Programmable Gate Array (FPGA) are major contributors of electromagnetic noise at printed circuit board (PCB) level. The evolution of IC technology and their complexity through the increase of the number of transistors and the miniaturization of electronic components has a huge effect on the dynamic power consumption and the increase of parasitic electromagnetic emissions. Thus, there is a crucial need to construct models to predict the noise generated by large and complex digital IC, which creates tight constraints on PCB routing and decoupling capacitor budget to meet power integrity (PI) and EMC requirements. For this purpose, IC end-users need circuit models that predict with a reasonable accuracy the main characteristics of power supply voltage fluctuation (e.g. peak-to-peak amplitude) and conducted emission (CE) spectrum (e.g. the upper envelope) according to the circuit configuration. In order to be included within industrial design flow efficiently, these models must remain simple enough to ensure rapid simulations and compatible with usual simulation tools.

Existing standards such as ICEM-CE (Integrated Circuit Emission Model – Conducted Emissions) known as IEC62433-2 standard [1] have been developed to respond to these requirements. It provides an equivalent model of the circuit which predicts CE at PCB level due to the switching of internal logic blocks (core) and input-output (IO) interfaces of ICs, while it preserves the confidentiality of IC internal structures. The structure of the model is illustrated in Fig. 1 and is based on two main parts:

- the internal activity (IA) block which describes the current induced by the switching of internal structures of the circuit. It is related to the dynamic power consumption of the circuit, and thus to the clock frequency, the power supply voltage or the internal configuration of the circuit.
- the passive distribution network (PDN) which models the filtering effect brought by the die and package interconnects. This block is supposed independent of the internal activity of the circuit.

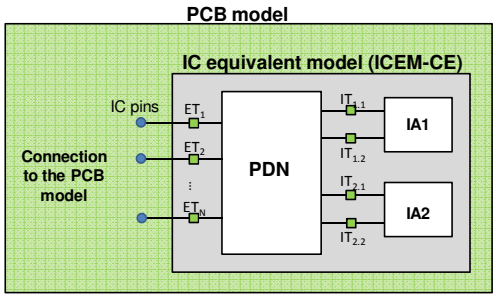


Fig. 1. Structure of ICEM-CE model

However, ICEM-CE is rarely delivered by IC manufacturers. This situation leads IC end-users to look for efficient methods to construct their own ICEM-CE models. The standard [1] and several publications describe measurement methods based on vector-network analyzer (VNA) to extract PDN block with a good accuracy, done either on a specific board or directly on the IC package [2] [3] [4]. Electrical equivalent models can be synthesized from these measurement results. The construction of the IA block

Manuscript received August 31, 2017. This work is supported by the IRT Saint-Exupéry Robustesse Electronique project sponsored by Airbus Operations, Airbus Group Innovations, Continental Automotive France, Hirex Engineering, Nexio, Safran Electrical & Power, Thales Alenia Space France, Thales Avionics and the French National Agency for Research (ANR).

C. Ghfiri, A. Boyer, S. Ben Dhia are with LAAS-CNRS, 7 avenue du colonel Roche, F-31077 Toulouse Cedex 4, France (e-mail: chaimae.ghfiri@laas.fr, alexandre.boyer@laas.fr, sonia.ben.dhia@laas.fr).

C. Ghfiri, A. Durier are with IRT Saint-Exupéry, 118 route de Narbonne, CS 44248, Toulouse, France (e-mail: chaimae.ghfiri@irt-saintexupery.com, andre.durier@irt-saintexupery.com).

remains a challenging task for IC end-users, especially the modelling of core noise. In [4], it is shown that IO noise can be accurately simulated with IBIS model [5] which is a widespread standard. Several methods have been proposed for the construction of the IA core block. As suggested by the standard, it can be extracted from an inverse method based on the measurement of the transient current flowing through the ground or power supply pins and the modelling of the PDN [3][4][6]. The main drawback of this measurement-based approach is that the IA extraction result depends on the PDN extraction. It is extremely sensitive to any measurement errors, which may become excessive for complex power multi-domain ICs, as it will be explained in section II. The IA core block can also be constructed from the simulation of the transistor netlist, with transistor model library and standard cell models [7][8][9]. However, this approach requires considerable simulation time and relies on unavailable data for IC end-users, making this method only adapted to IC designers. The IA block may also be roughly estimated from basic technological information about the technology and IC characteristics (e.g. CMOS technological node, number of logic gates, die surface…) [10], but the main drawbacks of this approach are the precision and the lack of consideration of the actual hardware or software configuration of the IC done by the end-user.

Manufacturers of ICs such as FPGA, SoC or low-power microcontrollers propose tools to compute the power consumption according to the circuit configuration. For example, FPGA design tools provide accurate estimation of the average dynamic power estimation from post-placement and routing simulations. Vector-based simulations allow the calculation of instantaneous power consumption, and thus the extraction time-domain profile of the dynamic current consumption [11] which can be used to build IA core block. However, this type of approach requires long simulation times, whose results are dependent on the input test vectors.

To overcome this issue, we propose to estimate the IA core block of a FPGA from vectorless power estimation and static timing analysis applied on post-placed and routed design. Compared to the vector-based approach, this solution is able to provide rapidly a reasonably accurate estimation of the IA core block in a very short time from a reduced set of data available to the end-users. Compared to extraction method based on measurements, it does not require long and tedious optimization of model parameters which may limit an industrialization process. Moreover, the proposed approach is able to take into account the time-dependent activity of the circuit.

In this paper, the methodology of construction of the IA block of a complex programmable digital circuit is presented and validated through several examples. A FPGA is used as case study in this paper. The results are also compared with those of the extraction methodology proposed by the IEC62433-2 standard. The principle and the limitation of the IA extraction methodology described in IEC62433-2 are explained in Section II. Section III is devoted to the presentation of the proposed methodology of construction of the IA core block. Then, the case studies are exposed in Section IV. Section V presents the comparison between measurement and simulation of the conducted emission produced by different case studies. Finally, the performances and accuracy of the methodology are compared with those of the extraction methodology proposed by the standard IEC62433-2.

## II. Description and Limitation of the Standard Methodology to Extract IA Block

ICEM-CE standard proposes a method of extraction of the IA based on a measurement of the RF current flowing outside the circuit, for example with a 1 Ω method [12]. This standard method uses an algorithm based on an inverse problem method, whose principle is described in Fig. 2. It consists in measuring in time domain the voltage $V_{ext}(t)$ due to the RF current flowing through the VSS pins with the 1 Ω probe. Then, the signal is converted to the frequency domain with a FFT. This voltage is an image of the IC internal current $I_{int}(t)$ filtered by PCB, package and die interconnects and decoupling. This effect can be modeled by a transfer function H(f). This function cannot be directly measured since there is no internal access in the die. An estimated transfer function is derived from the PDN block of the circuit and the PCB model. Finally, the internal current $I_{int}(f)$ can be computed using (1) and converted to time domain using an inverse FFT.

$$I_{\text{int}}(f) = V_{ext}(f).H(f)^{-1} \quad (1)$$

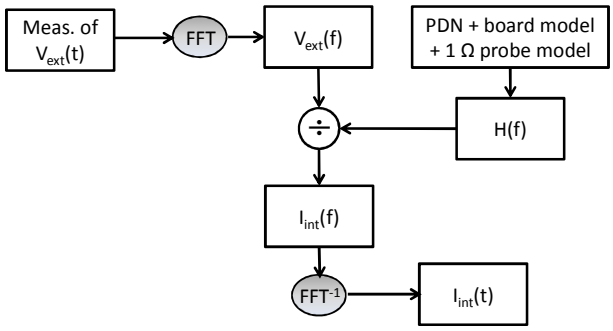


Fig. 2. Workflow of construction of IA with the standard methodology

This method requires the development of a specific test board to perform 1 Ω measurements, which may add cost and delay in the prototyping phase. But the main drawbacks of this approach are the dependency on the PDN measurement and extreme sensitivity to measurement errors. Furthermore, the standard provides no criterion to verify the consistency of the extracted IA. Although this method is reproducible and provides accurate simulation of the current flowing through the Vss pins, it does not ensure a good estimation of the internal current because of intrinsic weakness of inverse problem method, and the frequency behavior of IC and PCB interconnects.

In order to illustrate it, we can approximate the error $\Delta I_{int}$ made on the internal current estimation due to the errors on

$V_{ext}$ measurement $\Delta V_{ext}$ and estimation on the transfer function $\Delta H$. The absolute uncertainty on the internal current is obtained from the partial derivatives method applied on (1). (2) can be expanded by computing the expressions of the partial derivatives, as given by (3).

$$\Delta I_{\text{int}}(f) = \left|\frac{\partial I_{\text{int}}}{\partial V_{ext}}\right| \Delta V_{ext} + \left|\frac{\partial I_{\text{int}}}{\partial H}\right| \Delta H \tag{2}$$

$$\Delta I_{\text{int}}(f) = \frac{\Delta V_{ext}}{H} + V_{ext}\frac{\Delta H}{H^2} \tag{3}$$

There are two contributions to the uncertainty of the internal current, which are amplified when the modulus of H becomes small. It is the typical issue in inverse problem. In practice, the PDN has a low-pass filtering effect, except around some anti-resonance frequencies, so |H| is usually less than 1. The second term of (3) is linked to the estimation error on the transfer function and becomes dominant when |H| becomes small. Errors on internal current may become excessive either in high frequency since |H| tends to decrease with frequency, and close to resonant modes of the PCB and IC interconnects. Any errors on poles or zeros of H may result in very large error on H and thus on the internal current around these frequencies.

This problem is particularly pronounced in large and complex digital ICs with multiple power domains and mounted in high density package (e.g. BGA or PoP). The interactions between the multiple power domains and the large number of measurements required to extract the PDN model increase the error on the estimation of H and hence on the IC internal current estimation.

## III. Internal Activity Construction Based on Dynamic Power Consumption Estimation

To overcome the issues of the standard method, the extraction of the IA block must be independent on the PDN. It may rely on data that can be predicted rapidly with an acceptable accuracy, or measured simply on a prototype without specific test board. The CE of a synchronous digital circuit is related to the instantaneous current consumption, i.e. the charge transfer from the power supply to internal logical gates synchronized by a clock signal. Thus, the dynamic power consumption constitutes a valuable parameter to build the IA block, which presents two advantages: it is a common and critical parameter for IC end-users, and it constitutes a criterion to assess the physical consistency of the IA. In this part, the proposed method to build the IA core block of a complex IC is presented and applied on a FPGA (Spartan 6 from Xilinx). This methodology can be extended to other families of FPGA.

### *A. Influence of the instantaneous current consumption waveform on emission spectrum*

In digital synchronous circuits, current consumption appears mainly during transitions from logical state 0 to 1. The time domain profile of the instantaneous current is a periodic series of short pulses whose period is equal to the clock period Tc. As explained in [13], the characteristics of the power supply noise can be predicted if the charge consumed at each clock transition is determined correctly. It is directly linked to the dynamic power consumption. The waveform of the current i(t) delivered by the IA block must reproduce this charge quantity, given by:

$$q = \int_0^{\tau} i(t)dt \tag{4}$$

where q is the transferred charge during a clock cycle and $\tau$ is the duration of the charge transfer or the current pulse. The respect of this criterion leads to the correct prediction of the power supply noise spectrum in low frequency whatever the waveform of i(t). The transition time of this waveform sets the cut-off frequency and above it the spectrum rolls off rapidly. Too sharp transitions may lead to an overestimation of the noise spectrum in high frequency. If the duration $\tau$ is known approximately, a canonical waveform such as triangular pulse with transition time bounded by $\tau$ can be chosen and will provide a correct prediction of the envelope of the noise spectrum above the cut-off frequency. Whatever the waveform of the instantaneous current consumption, if the transferred charge and transfer duration are respected, the overall trend and magnitude of the CE spectrum may be determined, which is acceptable for the fast evaluation of the CE required by IC end-users. The proposed methodology relies on the evaluation of both of these criteria.

### *B. Presentation of the IA construction methodology for a FPGA circuit following a deterministic approach*

The charge quantity transferred at each clock cycle can be determined from measurements or the evaluation of the average dynamic power consumption $P_{dyn\_avg}$ by a design tool. It is given by (5):

$$P_{dyn\_avg} = F_C \sum_{i=1}^{N} \alpha(i) q(i) \cdot V_{DD} \tag{5}$$

where N is the number of internal logical nodes in the circuit, $\alpha(i)$ is the average number of transitions on node i per clock cycle (toggle rate), q(i) is the quantity of charge associated to node i, $V_{DD}$ is the power supply voltage and $F_C$ is the clock frequency of the circuit.

For its Spartan 6 family, Xilinx provides inside its ISE design suite the Xilinx Power Analyzer (XPA) module which gives a detailed estimation of the power consumption of the clock tree, the signals and logic blocks, and the IOs after post-placement and routing [14]. XPA also gives a fast vectorless estimation of the toggle rates and average dynamic power of all the internal logic signals after placement and routing step, which is a common feature of FPGA design tools. The average quantity of charge Q transferred to logic blocks during a clock cycle can be calculated from (6), where $T_C$ is the clock period and $I_{avg}$ is the average dynamic current consumption.

$$Q = \sum_{i=1}^{N} \alpha(i) q(i) = I_{avg} \cdot T_C \quad (6)$$

Moreover, ISE Xilinx tool performs a static timing analysis which gives a detailed report about the slack and the data path delays at the fast and slow Process/Voltage/Temperature corners. This analysis provides bounds for the propagation times of logic and clock signals within the circuit rapidly. For the construction of the IA, the pulse duration τ is considered to be the average value of the interval bounded by the maximum data path $\tau_{max}$ and the minimum data path $\tau_{min}$ given by the static timing report (7). The average dynamic current associated to a periodic pulsed waveform i(t) is calculated using (8).

$$\tau = \frac{\tau_{max} + \tau_{min}}{2} \quad (7)$$

$$I_{avg} = \frac{1}{T_C} \cdot \int_0^{\tau} i(t) \cdot dt \quad (8)$$

In the next paragraphs, we consider that the dynamic current consumption waveform is a symmetrical triangular pulse. The peak amplitude of the pulse $I_{max}$ is given by (9). From equations (7), (8), and (9) the maximum amplitude of the IA waveform is calculated using (10). Fig. 4 summarizes the steps to get the required data from a FPGA design tool to solve the equation (10) and construct the IA block.

$$I_{max} = 2 \cdot I_{avg} \cdot \frac{T_C}{\tau} \quad (9)$$

$$I_{max} = \frac{2.P_{dyn\_avg}}{F_C.\tau.V_{DD}} \quad (10)$$

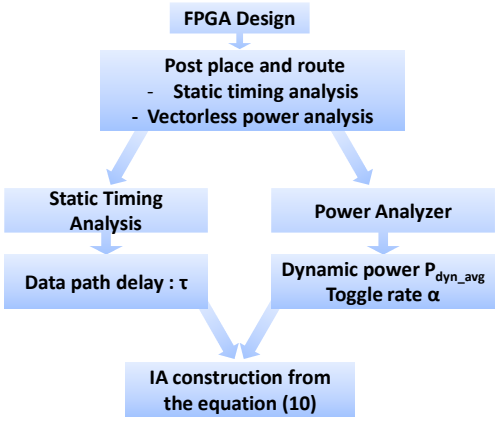


Fig. 3. Construction workflow of the Internal Activity block for FPGA circuit following a deterministic approach

The proposed workflow of construction of the IA is based on the average dynamic power consumption; hence, the approach proposed is deterministic. The amplitude of the IA is constant at each clock cycle. In practical cases, the IA profile is random due to the variation of the toggle rate and the power consumption of the active logic blocks. Thus, the peak-to-peak amplitude of the IA in the time domain could be underestimated and the envelope of the emission spectrum inaccurate. In the next part, an alternative approach is proposed for the construction of a random IA.

### C. *Statistical method for construction of a random IA*

The construction of a random IA block is possible with a vector based simulation [11] but it requires long simulation time. However, the power analysis tool XPA gives the switching probability (toggle rate $\alpha_i$) and the dynamic power consumption of each logic block and routed signal. The probability density function (PDF) of switching of each logic block of the circuit can be calculated and thus the PDF of the transferred charge to each logic block per clock cycle. Although the logic states of each logic block are partially dependent, we neglect these interdependencies. Assuming that each logic block of the circuit switches independently from the others, the PDF of the transferred charge to the circuit is the convolution product of the PDF of the transferred charge of each logic block. Statistical parameters such as the average and standard deviation can be calculated, and the most representative statistical law can be determined. In practice, due to the large number of switching logic nodes, the distribution tends to be Gaussian.

Under this assumption, the probability that a charge quantity $q_i(j)$ is transferred to a logic node i per clock cycle during a transition j is given by $p_i(j)$. Hence, the average transferred charge quantity $\overline{q_i}$ to each logic node is calculated using (11), where M is the number of transition types. In the binary case, M = 2. (11) can be simplified as shown in the rightmost expression, with $q_i$ the transferred charge during transitions. The expected variance $\sigma_i^2$ is given by (12), allowing the calculation of the PDF of each logic node i.

$$\overline{q_i} = \sum_{j=1}^{M} q_i(j).p_i(j) = \alpha_i \cdot q_i \ \ if\ M = 2 \quad (11)$$

$$\sigma_i^2 = \sum_{j=1}^{M} p_i(j) \cdot \left(q(j) - \overline{q_i}\right)^2 = \alpha_i(1-\alpha_i) \cdot q_i^2 \ \ if\ M = 2 \quad (12)$$

The PDF of the transferred charge to the circuit follows the normal distribution $N(Q,\sigma^2)$, where Q is the average transferred charge quantity (13), $\sigma^2$ its variance (14) and N the number of logic blocks of the circuit.

$$Q = \sum_{i=1}^{N} \overline{q_i} \quad (13)$$

$$\sigma^2 = \sum_{i=1}^{N} \sigma_i^2 \quad (14)$$

Finally, in order to generate a SPICE compatible IA source, a series of random charge quantity Q(k) is generated at each clock cycle k according to the determined PDF. Considering a symmetric triangular pulse, the amplitude $I_{max}(k)$ of the IA is given by (15). The IA is then modelled using a current source based on PWL file. Fig. 5 summarizes the approach of construction of the random IA.

$$I_{max}(k) = \frac{2 \cdot Q(k)}{\tau} \quad (15)$$

### D. *Development of an IA generator tool*

The proposed methodology for the construction of IA core block is based on the dynamic power and static timing analysis reports provided by the design tool. The hand-analysis of these reports could take a long time so a dedicated tool was constructed to automate the generation of the IA of the FPGA (ICEM Generator). It integrates the algorithm described previously for the generation of a constant and a random IA. The workflow of CE simulation using ICEM Generator tool is described in Fig. 5. This tool analyzes the power analysis report (.pwr) and the static timing analysis report (.twr) provided by Xilinx design tools after synthesize and post placement and routing simulation of a specific configuration. The generation of these reports does not require extra steps in the FPGA design process. The tool determines the different clock and power domains, associates current sources to the different functional parts of the FPGA and computes the parameters of these current sources. The IA can be combined with the PDN block to build the ICEM model of the circuit. Finally, a SPICE compatible sub-circuit is generated and can be exported for CE simulation.

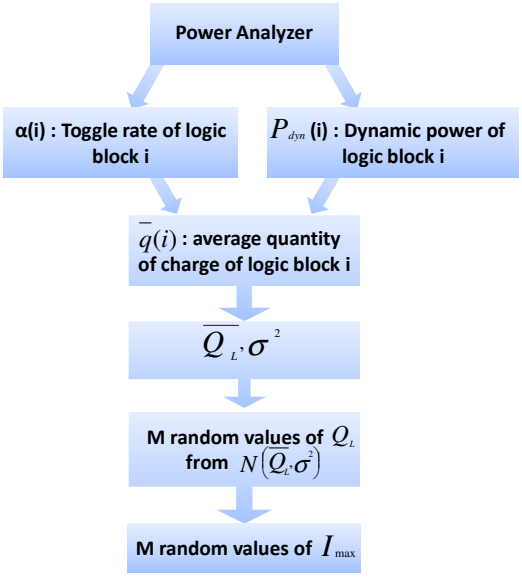


Fig. 4. Workflow of the IA construction using the statistical approach

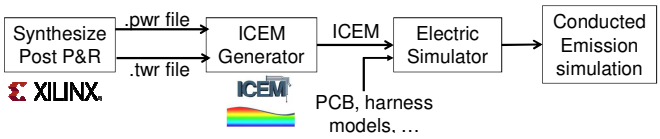


Fig. 5. Workflow of CE simulation using ICEM Generator tool

## IV. PRESENTATION OF THE CASE STUDIES

### A. *The circuit under test*

The circuit under test is a XC6SLX16-FT256 Spartan 6 Xilinx FPGA, manufactured in CMOS 45-nm process. The circuit includes 9152 configurable logic blocks (CLB) and up to 186 user IOs. It is mounted in a Fine pitch Thin Ball Grid Array 256 balls (FTBGA256). The internal structure of this component is complex. It comprises six different power supply domains:

- $V_{CCINT}$ dedicated to the CLB (1.2 V)
- $V_{CCOx}$ (x = 1 to 4) dedicated to the I/O organized in four banks (3.3 V)
- $V_{CCAUX}$ dedicated to the JTAG configuration (3.3 V)

### B. *Description of the test board*

A specific test board has been designed for the external voltage measurements and the validation of the constructed IA and ICEM model. It consists of a six layer board with complete power and ground planes compliant to the IEC61967-1 standard. Several test points have been placed for CE measurements and characterization of the board impedance. A 1 Ω probe, as defined by the IEC61967-4 standard has been placed between the ground pins of the FPGA and the ground reference of the test board in order to measure the return current flowing outside the circuit. Moreover, 150 Ω probes [12] have been placed on the different power supply domains to characterize CE and validate the constructed IA. The test configuration is described in Fig. 6.

Models of the PDN of the FPGA and of the test board have been constructed from S parameter measurements and electromagnetic simulations and validated previously [4].

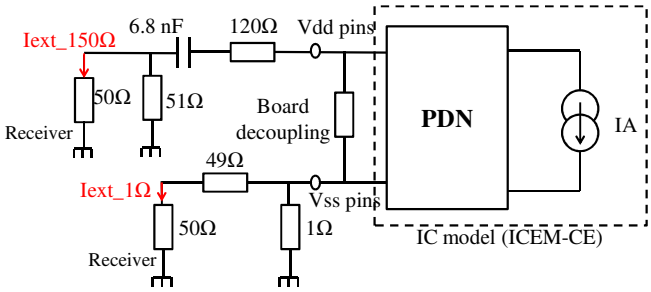


Fig. 6. Test configuration using a 1/150 Ω probe

### C. *Configurations*

The workflows presented in part III are verified for different case studies of synchronous digital designs. The clock frequency is set to 16 MHz for the different case studies. For the different cases, no output buffer is switching. Hence, CE measurements and simulations show only the contribution of the internal logic blocks and the clock tree activity of the FPGA.

Fig. 7 shows the structure of the first case study: a delay line. For optimum dynamic power consumption, 90 delay lines have been cascaded in series, each delay line includes N = 100 inverters. Due to its regular structure, its dynamic power consumption is deterministic i.e. the number of switching gates remains identical at each clock transition.

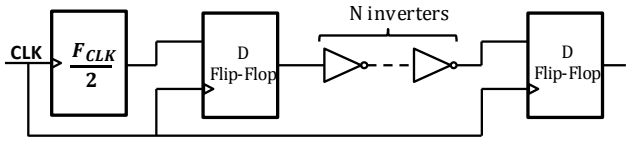


Fig. 7. Structure of a delay line case study

As another validation case, a configuration with a random number of switching gates is tested, with a Pseudo Random Number Generator (PRNG) blocks. The structure of the 5-bit PRNG is presented in Fig. 8. 200 identical PRNG have been cascaded in parallel to maximize the dynamic power consumption.

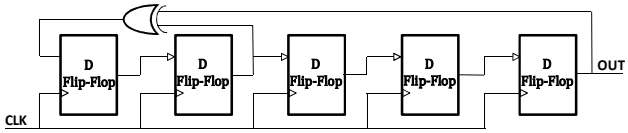


Fig. 8. Structure of the 5-bit PRNG case study

The last case study has more practical interest for embedded applications and is referred as industrial application. It consists in a digital finite impulse response filter followed by a real-time FFT. As presented in Fig. 9, this application uses a various types of internal structures of the FPGA (CLB, digital clock module, RAM, DSP blocks). Table I summarizes the dynamic power consumption, data path delay and the average toggle rate collected from the design tools of Xilinx for these three case studies.

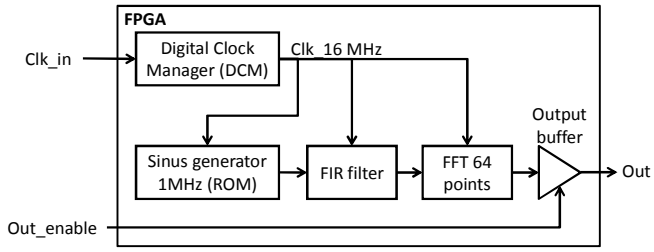


Fig. 9. Structure of the industrial application case study

TABLE I. ESTIMATED PARAMETERS FOR THE TESTED CONFIGURATIONS

| Configuration | Dynamic Power (mW) | | Data path delay (ns) | | Average toggle rate (%) |
|---|---|---|---|---|---|
| | Logic | Clock | Logic | Clock | |
| Delay Line | 24 | 1,5 | 40 | 0,75 | 100 |
| 5-bit PRNG | 3,11 | 1,5 | 1,5 | 0,75 | 38,75 |
| Industrial Application | 13,26 | 5,9 | 5 | 0,8 | - |

## V. CONSTRUCTION OF THE INTERNAL ACTIVITY BLOCK

### A. *Case study 1: Delay Line*

The toggle rate is 100 % because all the signals are switching at the rising edge of the clock. The clock tree presents non-negligible dynamic power consumption, its toggle rate is about 200 %. Hence, the signals representing the clock tree consumes energy at both rising and falling transitions of clock signal. Therefore, the internal activity of the clock tree is separated from the internal activity of the signals and the logic blocks. Fig. 10 describes the structure of the IA block: two current sources are used to represent the activity of the clock, and one current source represents the activity of the signals and logic blocks. The IA waveform is supposed as a symmetric triangular pulse. The parameters are calculated from the resolution of the equations given in part III.

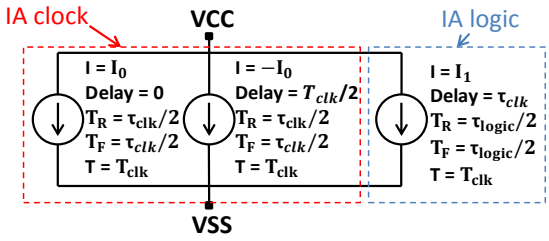


Fig. 10. Internal Activity block structure for Delay Line and 5-bit PRNG case studies

#### 1) *Validation of the model using 1 Ω probe measurement*

The constructed IA block is combined to the PDN and the board equivalent model. A transient simulation using ADS is performed to simulate the CE produced by the FPGA and captured by the 1 Ω probe. The time-domain simulation and measurement results are compared in Fig. 11. The simulated and measured peak-to-peak amplitude of the voltage fluctuation are similar: 9 mV and 11 mV respectively.

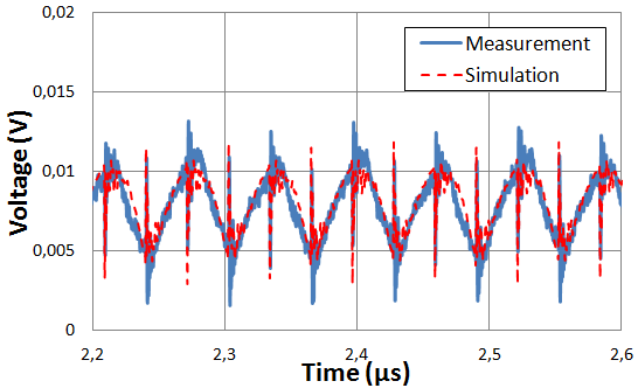


Fig. 11. Comparison between the measured and simulated external voltage using a 1 Ω probe in time domain (Delay Line configuration)

Fig. 12 shows a comparison between the measured and simulated spectrum of voltages with a 1 Ω voltage. The overall trend of the CE spectrum is correctly simulated with a RMS error of 5,15 dB calculated up to 2 GHz. This error may be considered as high, but the simulation predicts correctly that the frequency content of CE falls down above 1.2 GHz. Another recent and standard approach to compare measurement and simulation datasets, such as IEEE P1597 - Feature Selective Validation (FSV) technique [15] [16] [17], has been tested. It gives also a fair result. However, in spite of some discrepancies, the simulation gives prediction results with a sufficient accuracy to detect non-compliance risk.

Moreover, as the results are obtained directly from the IA block extracted by ICEM Generator and without any optimization process, they are produced very rapidly. It is an important requirement for IC end-users.

*1) Validation of the model using the 150 Ω probe measurement*

Fig. 13 shows a comparison between the measured and simulated spectrum of the external voltage using the 150 Ω probe. The figure presents a good correlation between the measurement and simulation up to 1 GHz with a RMS error of 4,95 dB.

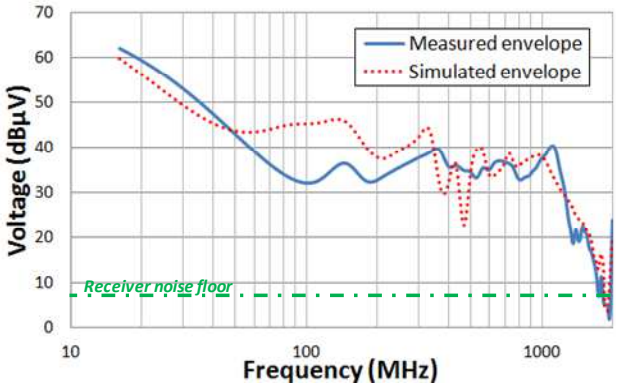


Fig. 12. Comparison between the measured and simulated external voltage using a 1 Ω probe in frequency domain (Delay Line configuration)

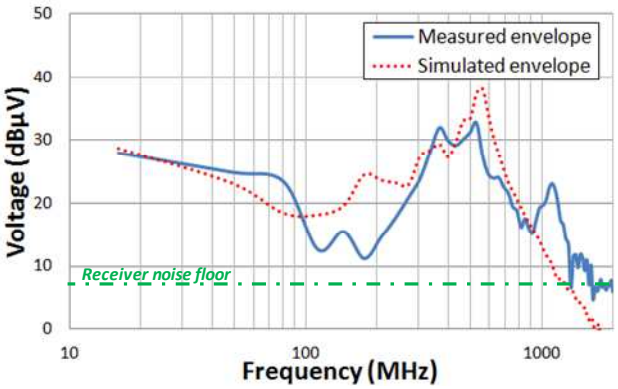


Fig. 13. Comparison between the measured and simulated spectral envelope CE with a 150 Ω probe on 1.2 V power plane (Delay Line configuration)

## B. Case study 2: 5-bit PRNG

The structure of the IA block for the 5-bit PRNG configuration is similar to the one of the Delay Line configuration (Fig. 10). Only the current source parameters change.

*1) Modelling with the deterministic approach*

The case of the PRNG presents pseudo-randomly switching bits every clock cycle. Thus, the dynamic power consumption will vary following the variation of the toggle rate of the active logic blocks. As a first approach, an IA is constructed following the deterministic approach for the CE simulation. Fig. 14 shows the comparison in the time domain between the simulation and the measurement of the external voltage fluctuation using a 1 Ω probe. The simulated peak-to-peak amplitude of 5,2 mV underestimates the measured maximum peak-to-peak amplitude of 7 mV. Although the simulation gives an approximate estimation of the average amplitude, it does not represent the variable character of the CE.

Fig. 15 presents the Fast Fourier Transform (FFT) of the previous comparison. The first harmonics are under-estimated, but globally, the simulated CE shows a good correlation with the measurement. The RMS error is 5,89 dB.

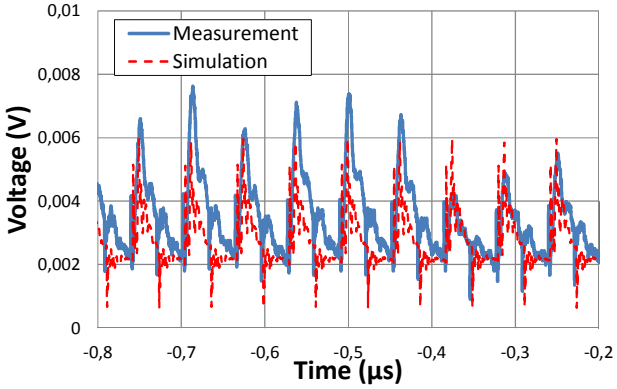


Fig. 14. Comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain using the deterministic approach (5-bit PRNG configuration)

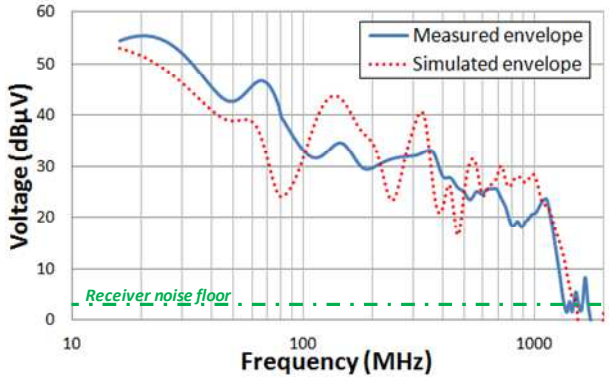


Fig. 15. Comparison between the measured and simulated external voltage using a 1 Ω probe in the frequency domain using the deterministic approach (5-bit PRNG configuration)

*2) Modelling with the statistical approach*

To improve the relevance of the results of the simulated CE in the time domain presented in the previous part, a random IA is constructed using the statistical method presented in part III.C. Fig. 16 shows the simulated and the measured external voltages using a 1 Ω probe. The simulated and measured maximum peak-to-peak amplitude of the voltage fluctuation are in accordance: 7.1 mV for the simulation and 7 mV for the measurement. The CE spectrum is improved partially with a RMS error of 5.26 dB.

The constructed IA block is also verified using the 150 Ω probe mounted on the power plane $V_{CCINT}$. Fig. 17 presents a comparison between the measured and simulated spectral envelope of the CE. Overall, the comparison shows a good correlation between the measurement and the simulation up to

1 GHz with a RMS error of 8,1 dB. Some differences between the measured and simulated envelope can be noticed between 100 and 300 MHz. It could be related to our assumptions about the IA waveform, but also to the PDN or the board model construction errors.

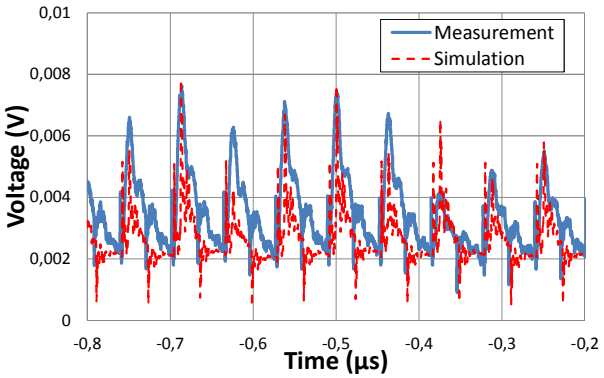


Fig. 16. Comparison between the measured and simulated external voltage using a 1 Ω probe in the time domain using the statistical approach (5-bit PRNG configuration)

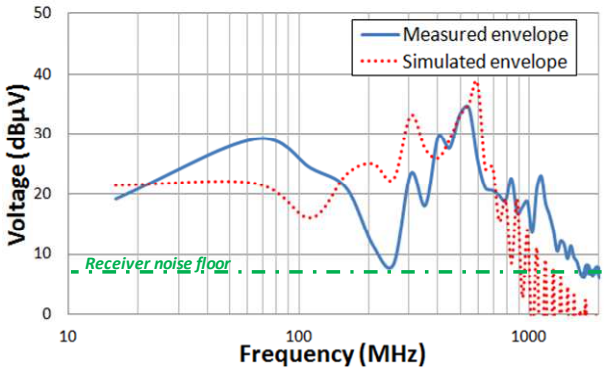


Fig. 17. Comparison between the measured and simulated spectral envelope CE with a 150 Ω probe on 1.2 V power plane (5-bit PRNG configuration)

These results demonstrate that the statistical approach increases the relevance of the simulated CE mainly in the time domain. The statistical approach takes into account the variability of the peak-to-peak amplitude of CE and thus does not lead to an underestimation of the maximum peak-to-peak amplitude of the ripple voltage. However, there is no clear improvement in the simulated spectrum in the frequency domain between the deterministic and the statistical approaches. The variable internal activity of circuit leads to a spreading of the spectrum around each harmonic frequency of the IC clock and thus to a small decrease of the emission level. This decrease is weakly predictable without the exact knowledge of the time-domain evolution of the IC internal activity. With only a statistical model, this spectrum spreading effect is not modelled accurately. Only the trend of emission level decrease is reproduced.

### C. *Case study 3: Industrial application*

Fig. 18 presents a comparison in time domain between the measured and simulated external voltage with the 1 Ω probe. The simulated peak to peak amplitude (14,2 mV) is in good agreement with the measured peak to peak amplitude (14 mV).

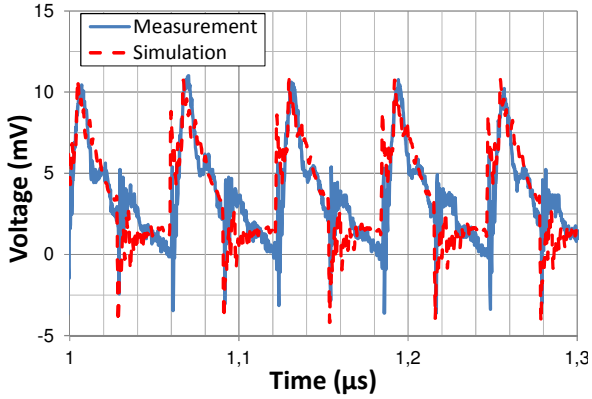


Fig. 18. Comparison between the measured and simulated external voltage with a 1 Ω probe in the time domain (Industrial Application)

The simulated and measured envelopes of the CE spectra of the signals shown in Fig. 18 are plotted in Fig. 19. Measurement and the simulation results correlate in the overall frequency range with RMS error of 5,62 dB. Some differences between the measured and the simulated envelope could be due to any existing error on the different blocks of the ICEM-CE model. The comparison between the measured and simulated spectral envelope of CE using the 150 Ω probe on the power plane $V_{CCINT}$ is presented in Fig. 20. As for the previous case studies, some differences could be noticed between the measurement and the simulation. However, the overall trend of the CE spectrum is correctly simulated up to 1 GHz with a RMS error of 8,92 dB.

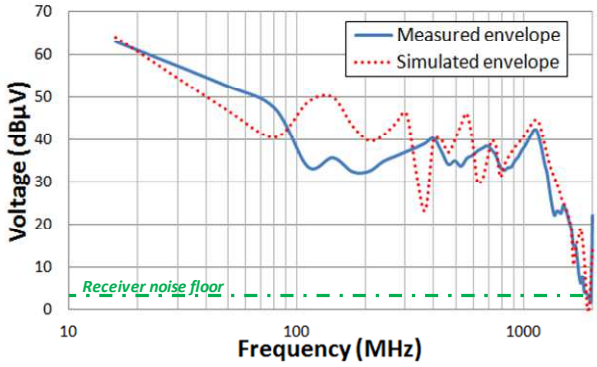


Fig. 19. Comparison between the measured and simulated spectral envelope of the external voltage using a 1 Ω probe (Industrial Application)

## VI. Comparison between the Proposed and the Standard Methodologies of IA Construction

For the different case studies, an IA block was also constructed following the standard method, and then compared to the IA extracted with the new methodology. Table II summarizes the comparison between the amplitude of the IA extracted with both methods. The comparison shows that the amplitudes of the IA constructed with standard method are always greater than those extracted following our

new methodology. This has a direct impact on the dynamic power consumption which is overestimated for the IA constructed with the standard method as presented in the rightmost columns of Table II. Although IA block is directly related to IC current consumption, the standard approach does not guarantee the physical validity of the IA block, in contrary to the proposed method which uses the current consumption as an input parameter to construct the IA block. This is one of the weakness of the standard method suggested by ICEM standard.

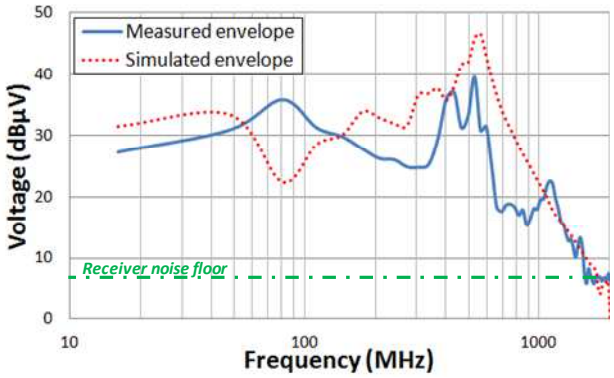


Fig. 20. Comparison between the measured and simualted spectral envelope CE with a 150 Ω probe on 1.2 V power plane (Industrial Application)

TABLE II. SUMMARY OF THE CONSTRUCTED IAS WITH THE DIFFERENT METHODS AND COMPARISON BETWEEN THE DYNAMIC POWER CONSUMPTION FOR THE DIFFERENT IA EXTRACTION METHODS

| | Amplitude of IA current source (mA) | | Dynamic power (mW) | | |
|---|---|---|---|---|---|
| | Std method | New method | Meas. | Std method | New method |
| Delay line | 450 | 340 | 26,8 | 38,16 | 24 |
| 5-bits PRNG | 618,45 | 550 | 4,8 | 6,17 | 3,11 |
| Industrial application | 628,8 | 424 | 24 | 40 | 23 |

It is also interesting to compare the transient current waveforms extracted with both methods. Fig. 21 shows an example with the Delay Line configuration. The IA extracted with the new method presents a canonical waveform. Even if it is probably simpler than the actual one, the contribution of clock and logic blocks switching is clearly visible. However, the waveform of the IA extracted by the standard method looks like a superimposition of the IA extracted by the new method with a high frequency noise, which is certainly unrealistic. As explained in section II, this noise is the result of the errors on PDN estimation and the wrong compensation of its filtering effect in high frequency.

The results of 1Ω and 150 Ω CE simulations obtained with both methods are summarized in Table III, where the RMS errors are given for the three case studies. The RMS errors on the spectrum of the CE captured with 1 Ω probe are almost similar with both methodologies. It is not a surprise. For the standard method, a low RMS error computed between the simulated and measured CE with the 1 Ω probe is expected since the IA extraction is based on an inverse method using the 1 Ω probe. For the new methodology, a low RMS error is reassuring on the proposed assumptions and methodology. This is shown in Fig. 22 which compared the measured and simulated CE using the 1 Ω probe according to the standard and the new IA extraction method.

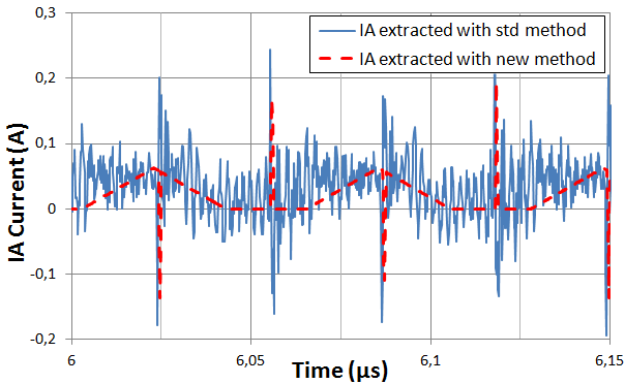


Fig. 21. Comparison between the waveform of the IA current extracted by the standard and the new IA extraction methods (Delay Line configuration)

TABLE III. THE RMS ERROR OF CE USING 1 Ω AND 150 Ω PROBE

| | RMS error of CE with 1 Ω probe (dB) | | RMS error of CE with 150 Ω probe (dB) | |
|---|---|---|---|---|
| | Standard method | New method | Standard method | New method |
| Delay line | 5,27 | 5,15 | 15,68 | 4,95 |
| 5-bits PRNG | 5,34 | 5,26 | 15,02 | 8,1 |
| Industrial application | 5,39 | 5,62 | 13,44 | 8,92 |

However, Table III shows that the standard method leads to a far larger error on the prediction of the 150 Ω CE than the new method. It is illustrated in Fig. 23, where the simulations of CE spectrum obtained with both methods in Delay Line configuration are compared with measurement. The simulated emission level with the standard extraction method exceeds largely the measured level above 100 MHz, with differences that reach up to 30 dB. Once again, it is due to the influence of errors on PDN estimation on the IA extraction process.

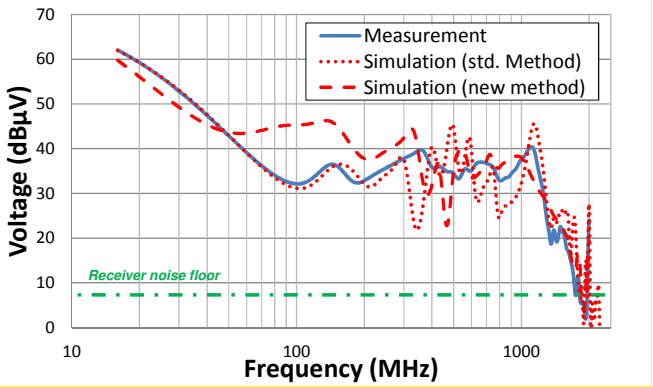


Fig. 22. Comparison between the measured and simulated spectral envelope CE with a 1 Ω probe according to the standard and new IA extraction method (Delay Line configuration)

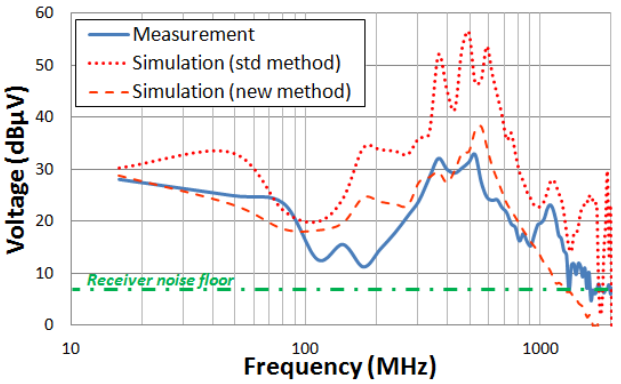


Fig. 23. Comparison between the measured and simulated spectral envelope CE with a 150 Ω probe according to the standard and new IA extraction method (Delay Line configuration)

## VII. Conclusion

In this paper, a new methodology of construction of the IA block for ICEM-CE model for complex digital IC has been presented. It aims at responding to the needs of IC end-users in terms of rapid but accurate prediction of PI and CE issues at board level. Contrary to the method proposed in ICEM-CE standard, our approach uses fast estimation tools of dynamic power consumption and switching times provided by IC manufacturers to build an approximate profile of the IC internal current. This approach has been tested through several case studies on a FPGA and provides correct estimation of the amplitude of power supply voltage fluctuation and CE spectrum envelope. This approach can be easily implemented by IC end-users in their design flow to obtain rapid but reliable prediction of PI and CE issues before board manufacturing. Compared to the standard approach, which is a measurement-based inverse problem method, it does not need transient current measurement done on the different configurations of the circuit and is not subjected to errors intrinsic to inverse problem method. This methodology can be extended to other FPGA since manufacturers provides in their design suite some estimation tools of power consumption and delays. As power consumption if a critical criterion for embedded applications, this approach could also be extended to other types of ICs (e.g. SoC, low-power microcontrollers) if manufacturers provide such estimation tools.

## References

[1] IEC62433-2:2017 - EMC IC modelling – Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE) - Edition 2.0, January 2017, IEC.

[2] C. Labussière-Dorgan, S. Bendhia, E. Sicard, J. Tao, H. J. Quaresma, C. Lochot, B. Vrignon, "Modeling the Electromagnetic Emission of a Microcontroller using a single Model", IEEE Trans. on EMC, vol. 50, no. 1, Feb. 2008.

[3] S. Serpaud, J. L. Levant, Y. Poiré, M. Meyer, S. Tran, "ICEM-CE Extraction Methodology", EMC Compo 2009, Toulouse, France.

[4] C. Ghfiri, A. Durier, A. Boyer, S. Ben Dhia, C. Marot "Construction of an Integrated Circuit Emission Model of a FPGA", 2016 Asia-Pacific Int. Symp. on EMC (APEMC 2016), Shenzhen, China, May 2016.

[5] IBIS I/O Buffer Information Specification - https://ibis.org/ver6.1/ver6_1.pdf - Ratified Sept. 11, 2015.

[6] J. L. Levant, M. Ramdani, R. Perdriau, "ICEM Modeling of Microcontroller Current Activity", 3rd Int. Workshop on EMC of ICs, Nov 2002, Toulouse, France.

[7] Hyun Ho Park, Seung-Hyun Song, Sang-Tae Han, Tae-Sun Jang, Jin-Hwan Jung, Hark-Byeong Park, "Estimation of Power Switching Current by Chip-Package-PCB Cosimulation", IEEE Trans on EMC, vol 52, no 2, May 2010.

[8] J. P. Leca, N. Froidevaux, P. Dupré, G. Jacquemod, H. Braquet, "EMI Measurements, Modelling, and Reduction of 32-Bit High-Performance Microcontrollers", IEEE Trans. on EMC, vol 56, no 5, Oct. 2014.

[9] T. Steinecke, T. Gokcen, J. Kruppa, P. Ng and N. Vialle, "Layout-Based Chip Emission Models Using RedHawk", EMC Compo 2009, Toulouse, France.

[10] E. Sicard, L. Bouhouche, "Using ICEM model Expert for TC1796 Emission", IC-EMC application note, www.ic-emc.org.

[11] Liehui Ren, Tun Li, Sandeep Chandra, Xiaohe Chen, Hemant Bishnoi, Student Member, Shishuang Sun, Peter Boyle, Iliya Zamek, Jun Fan, Daryl G. Beetner, Senior Member, James L. Drewniak, "Prediction of Power Supply Noise From Switching Activity in an FPGA", IEEE Trans. on EMC, vol 56, no 3, June 2014.

[12] IEC 61967-4 – edition 1.1: Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz - Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method, 2006-07.

[13] C. Sui, L. Ren, X. Gao, J. Pan, J. L. Drewniak, D. G. Beetner, "Predicting Statistical Characteristics of Jitter due to Simultaneous Switching Noise", IEEE Trans. on EMC, vol. 58, no. 1, Feb 2016.

[14] Xilinx power tools tutorial - Spartan-6 and Virtex-6 FPGAs, UG733, March 15 2010, www.xilinx.com.

[15] IEEE Standard P1597, Standard for Validation of Computational Electromagnetics Computer Modeling and Simulation – Part 1, 2 2008.

[16] A.P. Duffy, A.J.M. Martin, A Orlandi, G Antonini, T.M. Benson, M.S. Woolfson, "Feature Selective Validation (FSV) for validation of computational electromagnetics (CEM). Part I – The FSV method", IEEE Trans. on Electromagn. Compatibility, Vol 48, No 3, Aug 2006, pp 449 – 459.

[17] A Orlandi, A.P. Duffy, B Archambeault, G Antonini, D.E. Coleby, S Connor "Feature Selective Validation (FSV) for validation of computational electromagnetics (CEM). Part II – Assessment of FSV performance", IEEE Trans. on Electromagn. Compatibility, Vol. 48, No 3, Aug 2006, pp 460 - 467.

**Chaimae Ghfiri** obtained her engineer's degree in electrical engineering in 2014 from the Ecole Nationale Supérieure d'Electrotechnique, Electronique, Informatique, d'Hydraulique et des Télécommunications (ENSEEIHT) in Toulouse, France during an international exchange program with Ecole Hassania des Travaux Publics (EHTP) in Casablanca, Morocco. She is currently a PhD student at the Institut de Recherche Technologique (IRT Saint-Exupéry) and the Laboratoire d'Analyse et d'Architecture *des Systèmes* (LAAS-CNRS) and she works on the development of predictive EMC models taking into account the ageing.

**Alexandre Boyer** obtained a Masters degree in electrical engineering in 2004 and a PhD in Electronics from the Institut Nationale des Sciences Appliquées (INSA) in Toulouse, France, in 2007. He is

currently an Associate Professor in the Department of Electrical and Computer Engineering at INSA, Toulouse. He is leading his research at the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS-CNRS), as part of the 'Energy and Embedded Systems' research group. His current research interests include IC susceptibility and reliability modeling, and computer aided design (CAD) tool development for EMC (IC-EMC freeware).

**Sonia Ben Dhia** obtained her Masters degree in electrical engineering in 1995, and a Ph.D. in Electronic Design from the Institut National des Sciences Appliquées (INSA), Toulouse, France, in 1998. She currently holds the rank of associate professor at INSA-Toulouse, Department of Electrical and Computer Engineering. She conducts her research at the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS-CNRS), as part of the research group Energy and Embedded Systems, in the field. Her research interests include signal integrity in deep sub-micron CMOS ICs and electromagnetic compatibility and reliability of ICs. She has authored technical papers on signal integrity and EMC. She has also contributed to the publication of 3 books.

**Andre Durier** obtained his engineering degree in electronics from the Institut Superieur d'Electronique et du Numérique (ISEN), Lille, France in 1988. He was hardware engineer at Thales and GDI Simulation before to become project manager at Siemens VDO Automotive in 1998. In 2009, he became technical expert in Electromagnetic Compatibility at Continental Automotive France. He participated to numerous research projects on the EMC and on the immunity to radiations and published some papers on conducted immunity modelling. He is currently program manager at the Institut de Recherche Technologique Saint Exupery in charge of several research projects on components robustness. He is member of the Association Francaise de Normalisation (AFNOR) participating to International Electrotechnical Commission Sub Committee 47A (IEC SC47A) projects on EMC measurements (IEC 61967 & IEC 62132) and modelling (IEC 62433) at Integrated Circuit level.