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Delay estimation and measurement circuit for a high-speed CMOS clocked comparator

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***Abstract*—Comparators are a critical element of Analog-to-Digital converters (ADCs) intended to operate in a harsh environments such as the automotive. The influence of temperature on key comparator properties such as the delay must be well understood to maximize their speed. In this paper a Double-Tail latch analysis leads to an analytical expression for the delay to more accurately guide the design over a wide temperature range. The results given by this model agree well with spice post-layout simulation for a CMOS 0.18-μm SOI process, taking into consideration both process and temperature variations. To verify experimentally the correctness of the model we also propose a novel on-chip fully digital asynchronous architecture to measure the delay of the comparator, robust against extreme temperature variations.**

***Index Terms*—latch, double tail, comparator, delay, measurement circuit, Monte-Carlo Analysis, PVT, temperature**

I. Introduction

Comparators are a critical element of Analog-to-Digital converters (ADCs) intended to operate in a harsh environments such as the automotive. Reliable and robust operation must be ensured under stringent manufacturing (cost, yield, etc.) and operating conditions (voltage fluctuations, mechanical stress, etc.) over the lifetime of the part. Among these constraints, the operating temperature range (-50°C to +175°C) is arguably the most difficult one. Hence, the influence of temperature on key comparator architectures balancing speed, power, resolution must be well understood. In CMOS technology, the best compromise is usually obtained by the use of clocked comparators, which rely on cross-coupled positive feedback circuits that latch to the supply rails. They must be initialized (reset) to a given metastable starting state, from which they will depart and follow a trajectory to one of two stable states depending on the input signal polarity. In most clocked comparators, the total decision time of the comparator can be understood as the concatenation of typically one or more linear phases, followed by one exponential phase.

To design a comparator for a given ADC it is essential to know the time needed to reach a decision when a small input voltage difference is applied. In this paper we formulate an improved analytical model to estimate the double-tail comparator delay over an extended temperature range (-50°C to +175°C).

The experimental measurement of the delay over such a wide temperature also poses an interesting challenge. Earlier works have used simple as well as complex circuits for delay extraction. For example, in [1] one generates a DC voltage that is proportional to the average delay, thus avoiding the routing of high speed signals of chip. This simple solution is strongly influenced by the parasitic capacitance and its variation. More sophisticated approaches such as Time-to-Digital converters (TDCs) [2], achieve fine time delay resolution, but are hard to design against extremely large process-voltage-temperature (PVT) variations. In this paper we introduce a novel wholly digital asynchronous architecture for measurement of comparator delay that strikes a good balance between accuracy and area, and is robust with respect to extreme measurement conditions.

This paper is organized as follows; first we describe the behaviour of the double-tail (DT) comparator in Figure 1. This review is followed by the development of a new analytical model for estimation of the DT propagation delay valid for small differential input voltages, where the delay sets the limit for the achievable conversion rate. We also give the biasing conditions for extraction of the small signal parameters of our model. Afterwards, in Section III we discuss a novel on-chip digital circuit able to measure the comparator time delay accurately across PVT variations. The results of our model over process and temperature variations are discussed in Section IV. The model fit to a $\pm 6\sigma$ Gaussian Monte-Carlo simulation and is compared to a previous model [3]. This last section also presents the preliminary results of the proposed measurement circuit.

II. Comparator delay model

The DT comparator [4], shown in Figure 1, has become popular in the past few years, together with its variations [3], [5]. The key idea is to cascade a preamplification stage and a regenerating latch to decouple the design constraints of the two amplifiers. This configuration also improves the voltage headroom. Here we develop an original model for the propagation delay taking into account the current drawn by transistors M6-M7, to improve the accuracy with respect to previous works [3].

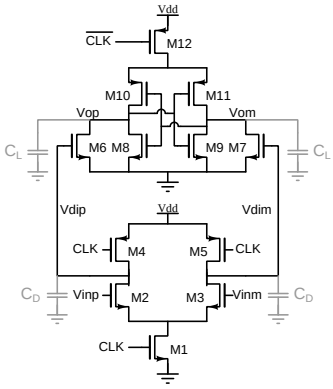


Fig. 1: Double-Tail comparator [4]

Briefly, during the reset phase, when CLK=0V, the tail transistor M1 is off and transistors M4-M5 are on. The drains of M2-M3 are pulled up to V_{DD}, discharging to the ground the output nodes (V_{op},V_{om}) of the cross-coupled latch, thanks to M6-M7. This is possible because M12 is off, driven by a complementary clock signal ($\overline{CLK}$). This reset phase is not considered as a part of our delay calculation since it has no impact on the decision operation. Once CLK toggles to V_{DD}, M4-M5 turn off, M1 turns on and the differential pair M2-M3 discharges the internal nodes $V_{dip,dim}$ to ground, at slightly different rates set by $I_{M2,M3}/C_D$. The capacitive load C_D is given by expression (1).

$$C_D = C_{gd2,gd3} + C_{gd4,gd5} + C_{gb6,gb7} + \frac{C_{gd6,gd7}C_L}{C_{gd6,gd7} + C_L} \quad (1)$$

The equation (2) describes the transient intermediate voltages $V_{dip,dim}$ through out the decision phase. The current $I_{M3,M2}$ has been assumed to remained constant until the beginning of regeneration phase.

$$V_{dip,dim}(t) = V_{DD} - \frac{I_{M3,M2}}{C_D}t \quad (2)$$

Our model of the comparator delay considers that the total delay is split between a linear preamplification t_{lin} and an exponential regeneration t_{reg}.

Once transistor M12 turned on, $V_{dip,dim}$ are translated by M6-M7 into current sinks at the output nodes. Hence, the output voltages $V_{op,om}$ ramp up at a rate of $(I_{M12}/2 - I_{M6,M7})/C_{load}$ where $C_{load} = C_L + C_{gs8,gs9} + C_{gs10,gs11} + \frac{(C_{gd9,gd8}+C_{gd10,11})C_L}{C_{gd9,gd8}+C_{gd10,11}+C_L}$. This expression assumes that the I_{M12} is equally shared between M10 and M11. The drain voltages of M8-M9 rise until one of them reaches V_{thn} above ground, when one can consider that regeneration takes over and the currents drawn by M6-M7 no longer matter.

The output voltages $V_{op,om}$ is therefore described as linear functions of the intermediate voltages $V_{dip,dim}$, which are themselves linear functions of the input voltages V_{inp} and V_{inm}. Therefore, the output voltages $V_{op,om}$ are a quadratic function of the input in the linear preamplification phase.

The time spent in this linear phase t_{lin} is thus given by the equation (3), and the differential output voltage $\Delta V_{out}(t_{lin})$ is approximately given by equation (4). One can observe that the small signal differential output voltage at the end of the linear preamplification, for $t = t_{lin}$, is dominated by the quadratic term if $g_{m6,m7}I_{M2,M3}t/C_D$ is greater than $I_{M12}/2 - g_{m6,m7}V_{DD}$.

$$t_{lin} = \frac{C_D/2}{g_{m6,m7}I_{M2,M3}}\left(\frac{g_{m6,m7}V_{DD} - I_{M10,M11}}{C_{load}} + \sqrt{\xi}\right) \quad (3)$$

$$\xi = (g_{m6,m7}V_{DD} - I_{M10,M11})^2 + 4V_{thn}\frac{g_{m6,m7}I_{M2,M3}(C_{load})}{C_D}$$

$$\Delta V_{out}(t_{lin}) = V_{op} - V_{om} \approx \frac{g_{m6}I_{M2} - g_{m7}I_{M3}}{(C_{load})C_D}t_{lin}^2 \quad (4)$$

For $t > t_{lin}$, the regeneration circuit drives the variation of the output voltage ΔV_{out}. The time to reach the fully restored logic level t_{reg} is given by equation (5). As mention earlier the total delay is the sum of t_{lin} and t_{reg}.

$$t_{reg} = \frac{C_L}{g_{m10,m11} + g_{m8,m9}} \ln\left(\frac{V_{logic}}{\Delta V_{out}(t_{lin})}\right) \quad (5)$$

Compared to the model given in [3] where the time delay is given by equation (6)-(8), one can observe that the linear time t_{lin} is substantially different.

$$t_{lin} = \frac{C_L V_{thn}}{I_{M2,M3}} \quad (6)$$

$$t_{reg} = \frac{C_L}{g_{m10,m11} + g_{m8,m9}} \ln\left(\frac{V_{logic}}{\Delta V_{out}(t_{lin})}\right) \quad (7)$$

$$\Delta V_{out}(t_{lin}) = 2V_{thn}\frac{g_{m6,m7}\Delta V_{dip,dim}}{I_{M12}} \quad (8)$$

A. Parameter Extraction

The DT comparator starts from a reset state, where intermediate voltages $V_{dip,dim}$ are pulled-up to V_{DD}. Thence, the parasitic capacitance estimation is extracted from post-layout simulation netlist by simulation for $CLK = V_{DD}$, $V_{DD} = V_{dip} = V_{dim} = 1.8V$. These operating conditions are assumed valid for the entire linear phase because the $V_{dip,dim}$ swing is small. Likewise the transconductance of M2-M3-M6-M7 are considered constant.

Given this considerations Table I lists the relevant parasitic capacitance of transistors.

TABLE I: extracted capacitance

Capacitance [fF]	M2-M3	M4-M5	M6-M7	M8-M9	M10-M11
cgb	4.07	7.59	1.61	1.17	1.69
cgs	73.4	0.24	27.7	0.56	0.20
cgd	68.6	0.23	25.9	0.58	0.21

TABLE II: extracted transconductance and current

$g_{m2,m3}$	328 μS	$g_{m8,m9}$	152.7 μS
$g_{m6,m7}$	4.3 μS	$g_{m10,m11}$	99.8 μS
I_{M1}	186 μA	I_{M12}	66.4 μA

In the case of M8-M9-M10-M11 the operating conditions for extraction of transconductance are different. Once regeneration starts, each output voltage continue to ramp up before the exponential increase is sufficient to push each one towards

a supply voltage. We can thus define the average conditions for those transistors for $V_{op} \approx V_{om} = V_{DD}/2$.

III. NEW DELAY MEASUREMENT CIRCUIT

Our new proposed circuit to reliably measure the comparator delay consists in a differential measure of a frequency generated by an auto-oscillator in which the comparator can be used. The frequency generated is the comparator clock and is then divided by a ratio N to be measured. The auto-oscillator generate a reference frequency without the comparator based only on digital cells used to generate the comparator clock. Then, the comparator's output voltages fully restored named CMPP and CMPM are used to generate a second frequency.

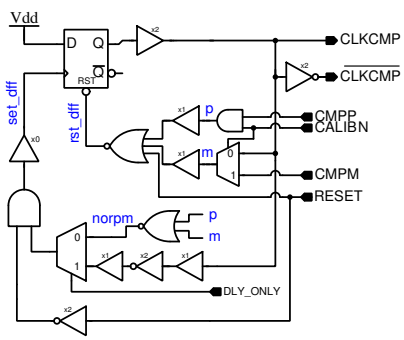


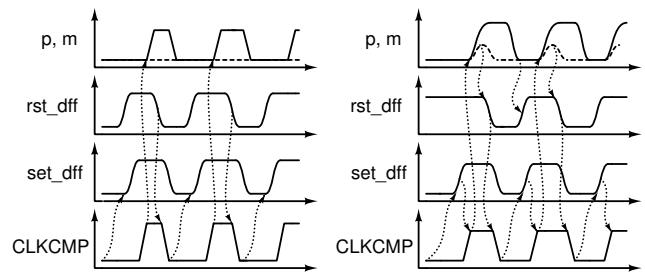
Fig. 2: proposed measurement circuit schematic

Figure 2 represents the schematic view of the circuit generating the frequency and connected to the comparator under test. Build around a central DFF, an inverter is used to generate the complementary clock of CLKCMP in order to ensure some delay between them to test the DT comparator. An initialization phase is required by a RESET set to '1'. The output of the DFF connected to CLKCMP through buffers is set to '0' and both comparators output, CMPP and CMPM, fall to '0'. Then a few picoseconds later, the clock signal of the DFF is also set to '0'. At the moment when the signal RESET is released to '0', the reset signal of the DFF is also released to '1' and CLKCMP keep its state. Few picoseconds later, the clock signal of the DFF rise to '1'. This edge triggers the DFF which set its outputs Q to '1', as depicted by the Figure 3 a and b. In consequence, the comparator makes a decision. The DFF is triggered either by the nor of p and m signal if CALIBN is '1' or by the inversion of CLKCMP if CALIBN is '0'. The DFF is reset, and the oscillations begin.

For DLY_ONLY set to '1', the clock of the DFF (set_dff) is the delayed inverted comparator clock CLKCMP. Therefore, the time of CLKCMP spend at zero is fixed. While, for a DLY_ONLY signal set to '0', the signal set_dff depends from the generated pulse of the nor gate. In that case, the time of CLKCMP spent at zero is defined by the speed of the comparator to reset.

The frequency difference between the two modes defined by CALIBN corresponds to the mismatch of the MUX inputs selecting either CMPM or CLKCMP, and the delay of the comparator to make a decision. While, the difference introduced by the two states of DLY_ONLY corresponds to the difference of the delay and the time to reset the comparator.

Thus, the proposed circuit is able to extract the delay of the comparator or the delay and the time to reset the comparator.



(a) CALIBN='0' (b) CALIBN='1'

Fig. 3: measurement circuit transient behaviour to only measure the delay

To ensure the correct operation, the delay between p/m to set_dff should be greater than the delay between p/m and rst_dff. And this over the process and temperature variation.

The calculation of the frequency in the normal operation mode (CALIBN='1' and DLY_ONLY=RESET='0') is given by the equation (9).

$$F_{CLKCMP} = \frac{1}{N}\left(T_{delay} + T_{set} + T_{rst} + T_{reset}\right)^{-1} \quad (9)$$

where T_{delay} is the delay of the comparator, T_{reset} the time the comparator takes to reset, and T_{set}/T_{rst} the time of the digital circuit to react.

In the calibration mode (CALIBN='0' and DLY_ONLY=RESET='0') the frequency is given by equation (10).

$$F_{CLKCMP*} = \frac{1}{N}\left(T_{set} + T_{rst}\right)^{-1} \quad (10)$$

The delay and the reset time is thus given by the equation (11).

$$T_{delay} + T_{reset} = \frac{1}{N}\left(\frac{1}{F_{CLKCMP}} - \frac{1}{F_{CLKCMP*}}\right) \quad (11)$$

When the DLY_ONLY signal is set to '1', the reset time of the comparator no longer matter, and T_{reset} of the equation (9) and (11) is 0.

IV. RESULTS

A. time delay model results

From the model describes in the section II, the analytical model have been validated with a 6-σ 100 points Monte-Carlo analysis at -50°C, +25°C, +125°C and +175°C.

The stimuli applied are a stair cased triangle signal compared to a dc voltage of 900 mV. As depicted by the Figure 4, the stair case triangle varies from -50 mV to +50 mV around the dc reference voltage with a 100 steps. The clock is fixed to 100 MHz with a rising and falling edge of 1 ns.

The delay is measured from the rising edge of the clock crossing 900 mV to the edge of $Q - \bar{Q}$ toggling by more than

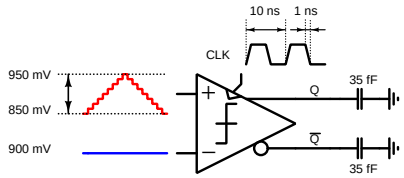
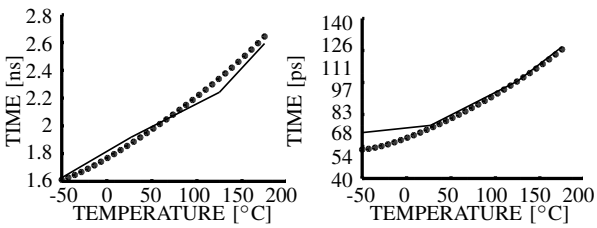


Fig. 4: simulation setup for the spice and the matlab model

75% of the voltage swing. The values kept are for each run the worst delay calculated.

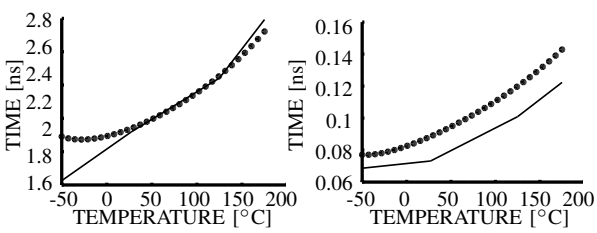
Figure 5 compares the estimation of the time delay to the simulated circuits in SPECTRE from from -50°C to +175°C and the standard deviation. The error on the estimation varies from -67ps to +94 ps for the proposed model. This represents a maximum error of 4.2 % due to a non accurate estimation of transconductance over the time and over the temperature.



(a) mean delay (b) standard deviation

Fig. 5: spice (-) and proposed analytical model (.) comparison of the mean time delay over temperature at 6-σ Monte-Carlo analysis

Figure 6 compares the estimation of the time delay to the simulated circuits in SPECTRE from from -50°C to +175°C and the standard deviation according the equation from [3]. The previous model of the double tail depicts an error on the estimation from -71 ps to +264 ps which represent an increased error of 80 % over the full temperature range compared to our model with and a reduced error from 27 $°C$ to 150 $°C$.



(a) mean delay (b) standard deviation

Fig. 6: spice (-) and analytical model from [3] (.) comparison of the mean time delay over temperature at 6-σ Monte-Carlo analysis

On the standard deviation the model from [3] exhibit an error from +8.4 ps to 20.5 ps while the proposed model commit an maximum error of -8.96 ps.

B. measurement circuit results

To verify the correct extraction of the comparator delay, and the time to reset, The proposed measurement circuit have been simulated post layout with a frequency divider of 64. The maximum frequency after the divider does not exceed 5.3 MHz.

With a verilog-a reference comparator with a time delay of 1.5 ns followed by inverters, the performances resulting from the circuit proposed are presented in the table III. Those results are compared to the simulation setup of reference presented Figure 4.

TABLE III: delay extraction from the proposed circuit for a comparator of reference

temperature	corner	T_{delay} from circuit	T_{delay} from Fig. 4	error
-50 $°C$	SS	1.627 ns	1.651 ns	24 ps
-50 $°C$	FF	1.636 ns	1.655 ns	19 ps
175 $°C$	SS	1.634 ns	1.66 ns	26 ps
175 $°C$	FF	1.645 ns	1.667 ns	22 ps

At the output of the comparator of reference extra inverters added are used to provide a capacitive load to the latch equal between the test setup. The error between the two simulation setup is less than 30 ps with a systematic error which can be explained by a different load on the inverters. The variation across corners is less than 5 ps for a maximum jitter of generated clock divided of 140 Hz, and a frequency measurement on 25 clock period of 2.9 MHz. Due to its asynchronous nature the circuit is hand-laid out in a 43.43 μm x 30.3 μm, a surface 3.3 times larger than the DT one.

V. Conclusion & Future Work

We have presented a new model for DT delay estimation, more accurate over an extended temperature range w.r.t. previous works, verified using $6-\sigma$ Monte-Carlo simulation runs under the SPECTRE simulator using a CMOS 0.18-μm SOI process. We also introduced a novel all-digital comparator delay measurement circuit for on-chip measurements based on a self-oscillating circuit with a differential frequency measurement methodology. The simulation results using a verilog-a reference comparator exhibit a low sensitivity on the process and temperature variation. A test chip was designed and sent for fabrication, experimental measurements will soon follow.

References

[1] B. Goll, M. S. Durante, and H. Zimmermann, "A measurement technique to obtain the delay time of a comparator in 120nm cmos," in *Proceedings of the International Conference Mixed Design of Integrated Circuits and System, 2006. MIXDES 2006.*, June 2006, pp. 563–568.

[2] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A cmos time-to-digital converter with better than 10 ps single-shot precision," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, June 2006.

[3] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, Feb 2014.

[4] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 314–605.

[5] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed adcs," in *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, Nov 2008, pp. 269–272.