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Noname manuscript No.
(will be inserted by the editor)

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Received: date / Accepted: date

Abstract Previous studies have shown that transconductance-to-drain-current ratio based design technique is useful for optimizing analog circuits. In this paper, we explore challenges associated with designing a low-power active inductor. We focus in particular on sizing issues that arise as the transistor speed is maximized and the current consumption is minimized. Finally, we apply the results to design an amplifier integrated with an active inductor in 0.18 μm CMOS process and show that by systematically working through sizing issues, a 10 μA amplifier with a tunable range of 691 MHz and 1.05 GHz can be designed.

Keywords Active inductor · g_m/I_D desgin

1 Introduction

Nanoscale Metal Oxide Field Effect Transistor (MOSFET) circuit design is driven by power consumption constraints. The minimal power consumption is achieved when transistors are operated in the weak inversion region [1]. In the absence of a model suitable for back of envelope calculations, designers often explore design space using arduous circuit simulations. Over-reliance on a circuit simulator can be problematic, potentially luring inexperienced designers to dive into simulation without understanding the underlying design trade-offs.

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In 1996, Silveira *et al.* proposed a powerful transconductance-to-drain current (g_m/I_D) method to help designers size up transistors quickly [1]. The so called "g_m/I_D design approach" was originally developed to calculate parameters such as small signal gain and bandwidth [1] and later extended to noise analysis [2], noise optimization [3], sensitivity analysis [4], and distortion analysis [5].

In this paper, we explore challenges associated with designing a low-power active inductor for sub GHz applications. We focus in particular on sizing issues that arise as the transistor speed is maximized and the current consumption is minimized.

Section 2 reviews the fundamentals of the g_m/I_D principle and the analysis of active inductor. Section 3 discusses the trade-offs involved in the design of a 10 μA active inductor at 1 GHz. Section 4 demonstrates a 10 μA current-reuse amplifier with an active inductor in 0.18 μm CMOS and shows that by systematically working through sizing issues a low current active inductor can be designed.

2 Analysis

2.1 Analysis of a Current-Reuse Active Inductor

Figure 1a shows an active inductor first proposed for GaAs and bipolar technologies [6] and later for CMOS technology [8]. The active inductor is composed of two transistors (M_1 and M_2) and is biased by two current sources (I_1 and I_2). The operation of the active inductor can be understood as follows. A test voltage (v_t) is applied to the source of M_2. A small signal current (i_2) with a magnitude equal to $g_{m2}v_t$ is generated as a result. The gate capacitance of M_1 integrates i_2 and

converts it into a rising voltage (v_{gs1}) at the gate of M_1. The transconductance of M_1 (g_{m1}) converts v_{gs1} into a current flowing into the drain terminal of M_1. As frequency increases, the impedance of C_{gs1} is reduced and less current is generated by M_1. Therefore, the impedance looking into the drain of M_1 increases with frequency and thus can be used as an active inductor.

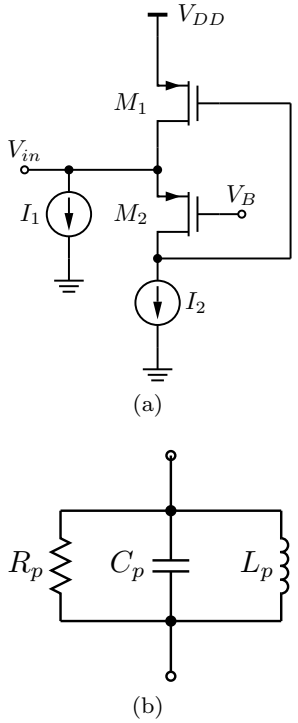


Fig. 1 (a) Schematic of a current-reuse active inductor (b) Equivalent circuit model for the active inductor

The equivalent circuit model (e.g. Fig. 1b) for the active inductor can be generated by replacing transistors in Fig. 1a with appropriate small signal model for M_1 and M_2. Figure. 2 shows the small signal model used to determine effective parallel inductance (L_p), the effective parallel resistance (R_p) and the effective capacitance (C_p) of the active inductor.

$$L_p = \frac{C_{gs1}}{g_{m1}g_{m2}(1 + g_{mbs2}/g_{m2})}, \tag{1}$$

$$R_{p,res} = \frac{1}{g_{m2}(1 + g_{mbs2}/g_{m2})} ||r_{o2}||r_{o1}, \tag{2}$$

$$C_p = C_{ss2} + C_{js2}. \tag{3}$$

g_{m1} and g_{m2} are the transconductance of M_1 an M_2. g_{ds1} and g_{ds2} are the drain-to-source transconductance of M_1 and M_2. g_{mbs2} is the source-body transconductance of M_2. C_{ss2} represents the total source capacitance of M_2 and includes contribution from C_{sg}, C_{sd}, and C_{sb}. C_{js2} represents the junction capacitance of the source of M_2.

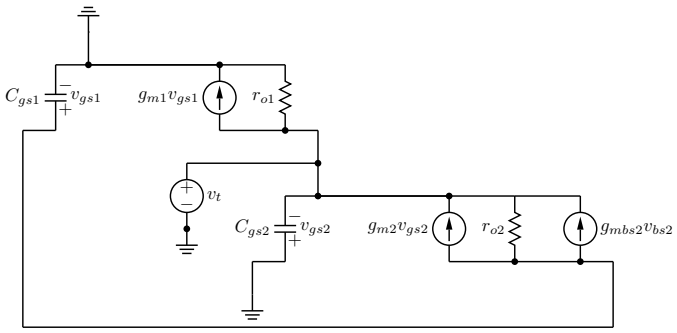


Fig. 2 Small signal model for the active inductor in Fig. 1a. The body terminal of M_2 is tied to V_{DD} and is treated as a small signal ground in this model

The quality factor of the active inductor can be calculated from R_p and $L_p$as follows

$$Q = \frac{R_p}{\omega L_p} \leq \frac{g_{m1}}{\omega C_{gs1}} = \frac{f_{T1}}{f}, \tag{4}$$

if $r_{o2}||r_{o1} >> 1/g_{m2}$. f_{T1} is the transit frequency of M_1. Equation 4 indicates that Q is proportional to f_{T1} and inversely proportional to f.

The self-resonant frequency (f_{res}) of the active inductor is related to the frequency at which an inductor resonates with its own capacitance. f_{res} is related to L_p and C_p of the inductor and can be associated with f_{T1} and f_{T2}, the transit frequency of M_1 and M_2, as follows:

$$f_{res} = \frac{1}{2\pi\sqrt{L_p C_p}} \approx \sqrt{f_{T1} f_{T2}} \tag{5}$$

2.2 g_m/I_D Principle

The g_m/I_D principle is applicable to parameters that are independent of a transistor's width. The basis of the g_m/I_D principle can be explained using Fig. 3. A transistor with a transconductance (g_m), a drain-to-source conductance (g_{ds}), and a current (I_D) is obtained using a gate-to-source voltage (V_{GS}) source and a drain-to-source voltage (V_{DS}) source. A second transistor with the same W/L ratio is placed in parallel. The transistors in parallel can be treated as one merged transistor with an aspect ratio of $2W/L$ and a transconductance over drain-current ratio of g_m/I_D. The drain-to-source conductance is doubled for the merged transistor. However, since g_m is also doubled for the merged transistor, the intrinsic gain is g_m/g_{ds}. Both the stand alone transistor and the merged transistor have the same g_m/g_{ds}, as long as they are biased at the same g_m/I_D. Once a transistor of a given W is characterized over a range

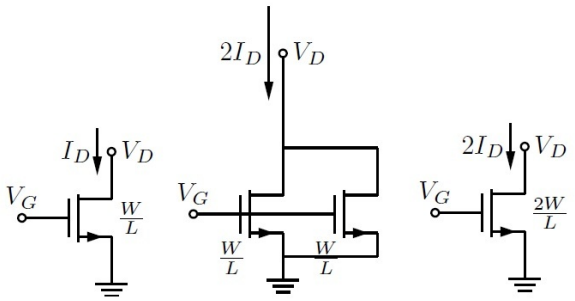


Fig. 3 Transistors biased at the same g_m/I_D

of g_m/I_D, the g_m/I_D based parameters can be generalized to a transistor of an arbitrary W, *assuming that* L *remains constant.*

The g_m/I_D dependent nature of g_m/g_{ds} can be generalized to any two parameters whose ratio does not depend on a transistor's width. For example a transistor's transit frequency (f_T), which is defined as g_m/C_{gs}, is a g_m/I_D parameter, since both g_m and C_{gs} are proportional to W. f_T is width independent and g_m/I_D dependent as a result.

2.3 g_m/I_D Dependent Inductor Parameters

Equation (1), (2), and (3) reveal that the effective active inductor parameters depend on small signal parameters, as well as width-independent parameters such as g_m/C_{gs}, g_m/g_{mbs} and g_m/g_{ds}. Once I_1 and I_2 are fixed, changing the g_m/I_D of a transistor changes the g_m, the width-independent parameters, as well as the effective inductor model parameters. Therefore, g_m/I_D can be used as a design variable in the design of an active inductor.

It can be shown that if $g_m/g_{mbs} >> 1$ and $g_m/g_{ds} >> 1$, (1), (2), and (3) can be reduced to

$$L_p = \frac{C_{gs1}}{g_{m1}g_{m2}} = \frac{1}{\omega_{T1}\frac{g_{m2}}{I_{D2}}I_{D2}}, \tag{6}$$

$$R_{p,res} = \frac{1}{g_{m2}} = \frac{1}{\frac{g_{m2}}{I_{D2}}I_{D2}}, \tag{7}$$

$$C_p = C_{gs2} = \frac{1}{\omega_{T2}}\frac{g_{m2}}{I_{D2}}I_{D2}. \tag{8}$$

Equation (6) shows that L_p is inversely proportional to g_{m1}/C_{gs1}, i.e. the f_T of M_1. As g_{m1}/I_{D1} increases, f_{T1} is decreased and L_p is increased as shown in Fig. 4.

Similarly, once I_{D1} and I_{D2} are fixed, increasing g_{m2}/I_{D2} leads to an increase in g_{m2}, and hence the effective parallel resistance at resonant frequency is reduced (Fig. 5a). As g_{m2}/I_{D2} increases, f_{T2} is decreased and C_P is increased (Fig. 5b).

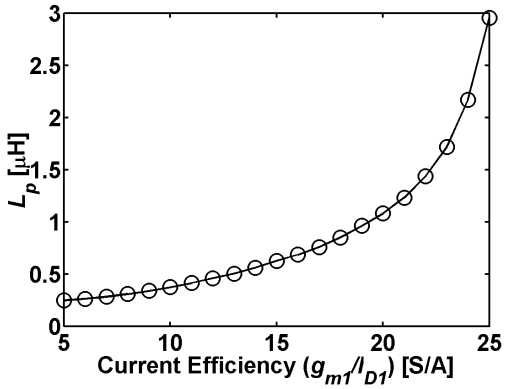
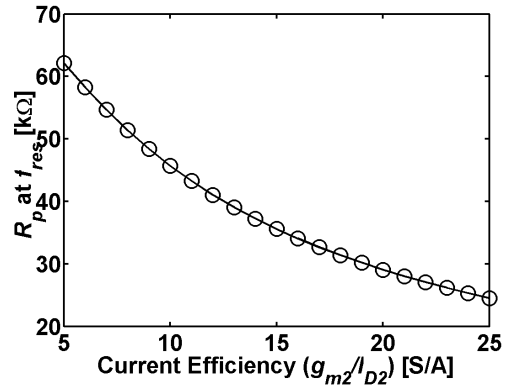
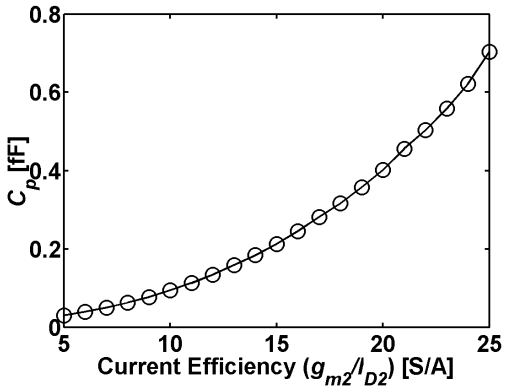


Fig. 4 g_m/I_D dependent inductance. L=180 nm. V_{SD}=275 mV. V_{SB}=0 V. g_{m2}/I_{D2} is 22 S/A



(a)



(b)

Fig. 5 g_m/I_D dependent inductor parameters. L=180 nm. V_{SD}=275 mV. V_{SB}=275 mV. g_{m1}/I_{D1}=12 S/A. (a) $R_{p,res}$ versus g_{m2}/I_{D2} (b) C_p versus g_{m2}/I_{D2}

3 Design Considerations

Section 2 shows that the effective active inductor parameters depend on the g_m/I_D dependent parameters. In low-power high-speed applications, design objectives such maximizing f_T of a transistor and minimizing cur-

rent consumption lead to transistor widths that approach minimum width allowed in a process, and hence the range of permissible g_m/I_D values is further limited. This section discusses sizing issues that are encountered in an active inductor design.

3.1 J_D and f_T

Current density J_D and transit frequency f_T are two g_m/I_D parameters that determine minimum design width and g_m/I_D dependent inductor parameters such as Q and f_{res}.

Using $g_m/I_D = 2/(V_{GS} - V_{TH})$, an approximate expression for J_D can be obtained [7]:

$$J_D = \frac{2\mu_n C_{ox}}{L(g_m/I_D)^2}. \quad (9)$$

J_D is inversely proportional to L and $(g_m/I_D)^2$. μ_n represents mobility and is g_m/I_D dependent. PSP model is used in Sect. 3.2 to confirm the g_m/I_D dependence of J_D.

A transistor's transit frequency (f_T) is defined as $g_m/(2\pi c_{gs})$. f_T is a g_m/I_D parameter since both g_m and c_{gs} are proportional to W. f_T is a function of both L^2 and g_m/I_D [7].

$$f_T = \frac{3\mu_n}{2\pi L^2 g_m/I_D} \quad (10)$$

f_T is inversely proportional to both L and g_m/I_D. Equation 10 is approximate. PSP model is used in Sect. 3.2 to confirm the g_m/I_D dependence of f_T.

Equation (4) and (5) suggest that f_T should in general be maximized in order to increase Q and f_{res}. Both L and g_m/I_D can be reduced to increase f_T. Since J_D is also inversely proportional to L and g_m/I_D, assuming that the current is constant, transistor W is reduced as L and g_m/I_D are reduced.

3.2 Design Considerations of M_1

Figure 6a confirms that as indicated by (10), f_{T1} is reduced as L_1 is increased. Figure 6b shows that current density (J_{D1}) is increased as L_1 is reduced. Assuming that I_{D1} is constant, the width of M_1 is reduced as L_1 is reduced (Fig.6b). Thus, if L is reduced to maximize Q and f_{res}, W_1 is reduced. The minimum W_1 is determined by the current specification, as well as the minimum allowable width in a process.

The choice of g_{m1}/I_{D1} is tied to the choice of V_{SD1} and V_{SD2} since $V_{SD1} + V_{SD2} = V_{SG1}$. Assume that $V_{SD1} = V_{SD2} = V_{SG1}/2$, V_{SD1} and V_{SD2} are known once V_{SG1} is known. g_{m1}/I_{D1} is not chosen arbitrarily since it affects f_{T1} and hence the quality factor.

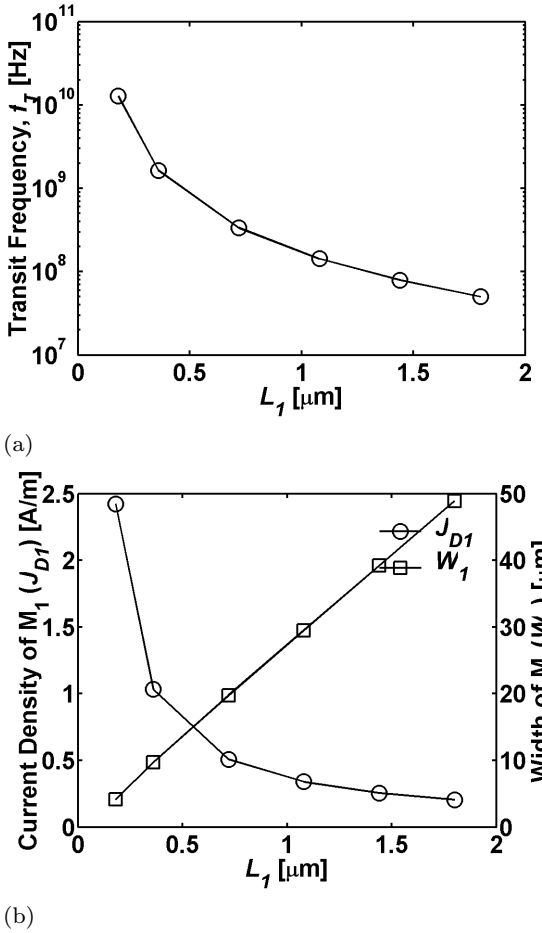


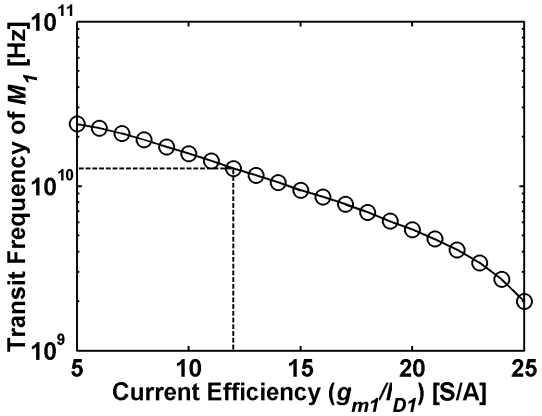
Fig. 6 (a) Transit frequency (f_{T1}) as a function of L_1 (b) Current density (J_{D1}) and Width (W_1) of M_1 as a function of L_1. In both (a) and (b), g_{m1}/I_{D1}=12 S/A. $|V_{DS1}|$=0.275 V and $V_{SB1} = 0$ V

Equation 10 shows that f_T is inversely proportional to g_m/I_D. Figure 7a re-confirms this observation. Moreover, it shows that in order to achieve an f_T in excess of 10 GHz, g_m/I_D for M_1 should be less than 15 S/A. Figure 7b shows that using $g_{m1}/I_{D1} = 12$ S/A, a V_{GS1} of 0.55 V is obtained.

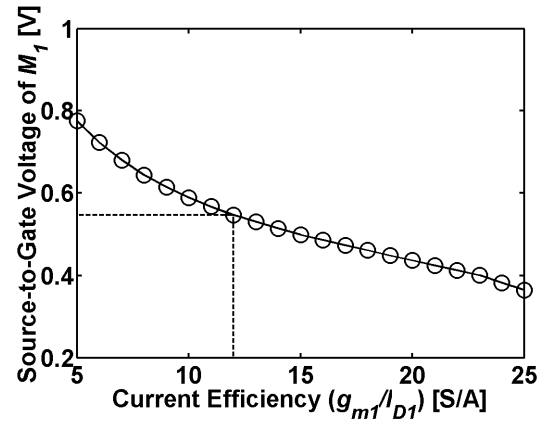
3.3 Design Considerations of M_2

In order to maximize Q and f_{res} of the active inductor, f_{T1} and f_{T2} should be simultaneously maximized. Hence L_2 is chosen to equal to L_{min}.

The determination of g_{m2}/I_{D2} is constrained by the minimum width of M_2. Figure 8a shows that g_{m2}/I_{D2} should be reduced in order to increase f_{T2}. As g_{m2}/I_{D2} is reduced, the current density is increased (Fig. 8b). Assume that I_{D2} is 1 μA, W is reduced as g_{m2}/I_{D2} is reduced. Figure 8c shows that at low g_{m2}/I_{D2} values (e.g. $g_{m2}/I_{D2} = 5$), the required width to maintain 1



(a)



(b)

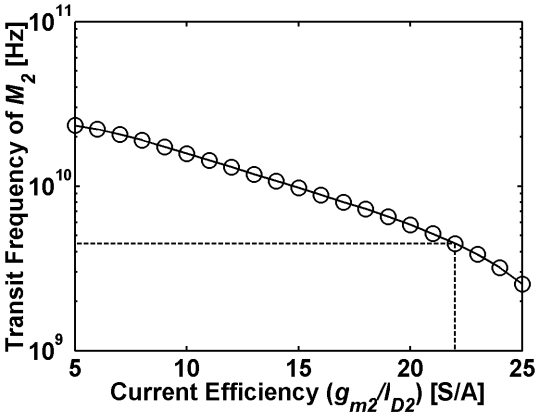
Fig. 7 (a) Transit frequency of M_1 as a function of g_{m1}/I_{D1} (b) V_{SG1} as a function of g_{m1}/I_{D1}. In both (a) and (b), the length is M_1 is 180 nm. V_{SD1}=0.275 V and $V_{SB1} = 0$ V

μA is below what is allowed by the process. As a result, g_{m2}/I_{D2} should be chosen to be much higher than the minimum allowable width. g_{m2}/I_{D2} is set to 22 S/A so that W_2 is $\approx 8W_{min}$, where $W_{min} = 0.4\mu$m is the minimum width supported by the 0.18 μm CMOS design kit.

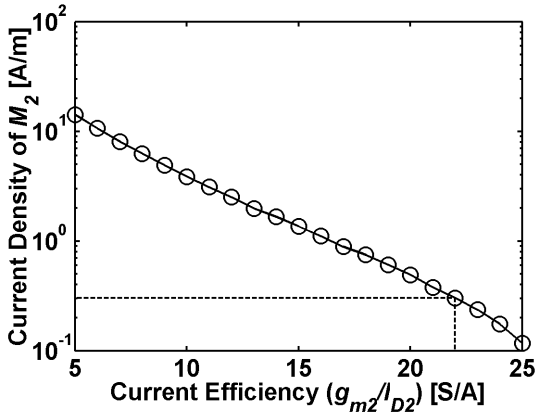
3.4 Simulated Impedance of an Active Inductor

The active inductor shown in Fig. 1a is constructed in a 0.18 μm CMOS. The g_m/I_D for M_1 and M_2 are 12 S/A and 22 S/A respectively for M_1 and M_2. The W/L ratio for M_1 and M_2 are 4.0/0.18 μm/μm and 3.2/0.18 μm/μm respectively. I_1 is set to 10 μA and I_2 is set to 1 μA. V_B, which is 1.1 V, is calculated from g_{m2}/I_{D2} and V_{SD1}.

Z_{in} represents the input impedance of the active inductor and hence the impedance seen by circuits connected to the active inductor. At resonant frequency, $|Z_{in}|$ is approximately $R_{p,res}$ or $1/(\frac{g_{m2}}{I_{D2}} I_{D2})$. As discussed in Sect. 3.3, the choice of g_{m2}/I_{D2} is constrained by W_2. It is difficult to raise $R_{p,res}$ by reducing I_{D2} since g_{m2}/I_{D2} would have to be increased to reduce current density. Increasing g_{m2}/I_{D2}, however, leads to a reduction in $R_{p,res}$.



(a)



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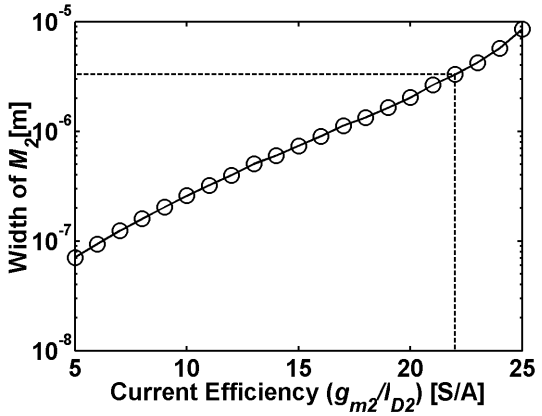

(c)

Fig. 8 Selection of g_m/I_D for M_2. L=180 nm. V_{SD}=275 mV. V_{SB}=275 mV. I_{D2}=1 μA. (a) f_{T2} versus g_{m2}/I_{D2}. (b) J_2 versus g_{m2}/I_{D2}. (c) W_2 versus g_{m2}/I_{D2}

Figure 9 shows a plot of $|Z_{in}|$ as a function of frequency. The resonant frequency is 1.6 GHz. The impedance at the resonant frequency is 13.7 kΩ. The quality factor is 0.6 and is comparable to quality factor reported in [9]. It is possible to increase the quality factor by adding a negative resistance in parallel with $R_{p,res}$ [8] at the expense of a slightly higher current consumption and lower resonant frequency.

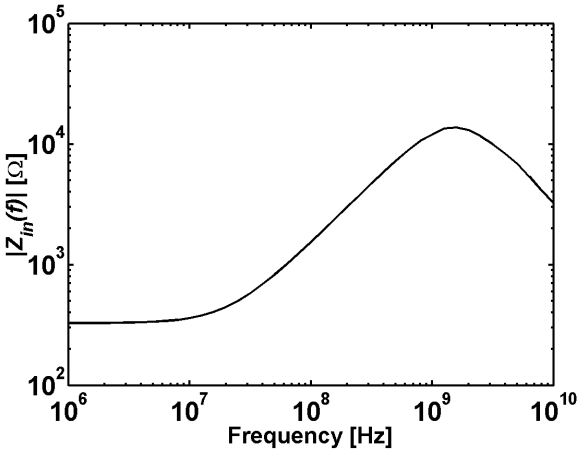

Fig. 9 $Z_{in}(f)$ of the active inductor shown in Fig. 1a

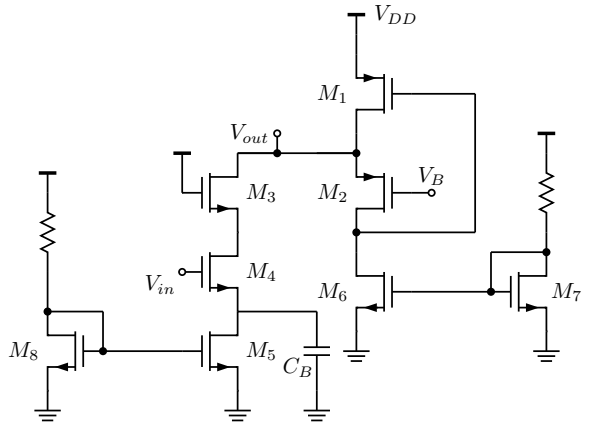

Fig. 10 A current-reuse amplifier with an active inductor. I_{D1}=10 μA and I_{D2} = 1 μA

4 Application

4.1 A Current-Reuse Amplifier

Active inductors are space efficient and are especially useful in applications where a large number of inductors are used [9]. Figure 9 shows a cascode amplifier (M_3 and M_4) loaded with an active inductor (M_1 and M_2). The inclusion of C_B shorts the source of M_4 to ground at the resonant frequency. The DC current of M_4 and $M2$ are controlled by current mirrors. The bias currents for M_1, M_2 and M_4 are 10 μA, 1 μA and 9 μA respectively.

The gain of the amplifier is approximately $g_{m4}|Z_{in}|$, or $(g_{m4}/I_{D4})I_{D4}$. g_{m4}/I_{D4} is chosen to be 18 S/A as a compromise bewteen speed and gain. I_{D4} represents the difference between I_{D1} and I_{D2}. One way to relax the constraint on W_2 (see in Sect. 3.3), is to keep I_{D1} constant while increasing I_{D2} and reducing I_{D4} simultaneously. The drawback of this approach, however is that if g_{m4}/I_{D4} were to remain constant, the gain of the amplifier would be reduced. Using $|Z_{in}|$=13.7 kΩ and g_{m4}=163 μS, our analysis shows that the expected gain is 6.9 dB. The Spectre simulation shows that the gain is 6.65 dB at 1.05 GHz.

The bias current of M_2 can be adjusted in order to change the resonant frequency. Figure 11 shows that by changing I_2 from 0.5 μA to 1.0 μA, the resonant frequency changes from 691 MHz to 1.05 GHz. The gain changes from 9.03 dB at I_2 = 0.5μA to 6.65 dB at 1.05 GHz. The Q varies slightly from 0.72 to 0.88. The frequency range and gain variation are comparable to results reported in [9]. Whereas the amplifier was biased at 14 μA in [9], the amplifier in Fig. 10 is biased at 10 μ, but yet it achieves comparable results using 28 percent less current.

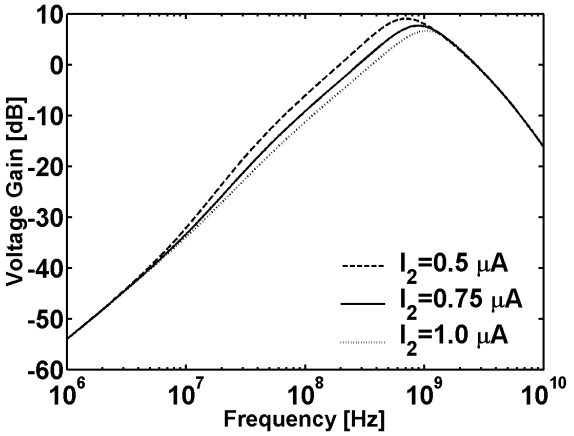

Fig. 11 Voltage gain of the amplifier shown in Fig. 10. I_2 is adjusted from 0.5 μA to 1.0 μA in order to change the resonant frequency from 691 MHz to 1.05 GHz

It is possible to increase the gain and the selectivity of the amplifier by cascading the current-reuse amplifier as shown in Fig. 12. Each current amplifier consumes 10 μA of current. Figure 12b shows that the voltage gain increases from 2.18 V/V to 10.29 V/V and 47.87 V/V when V_{o3} and V_{o5} are taken as the outputs respectively. The quality factor improves from 0.88 when V_{o1} is taken as the output to 1.69 and 2.02 when V_{o3} and V_{o5} are

taken as outputs. The drawback of this approach is that the total current is increased from 10 μA to 30 μA and 50 μA respectively.

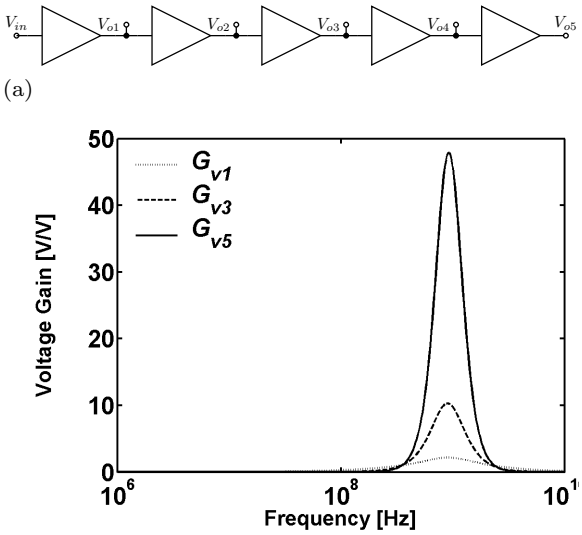

Fig. 12 Cascaded amplifier using the current-reuse amplifier in Fig. 10. Voltage gain G_{vi} is defined as V_{oi}/V_{in}, where $i = 1, 3$ and 5

5 Conclusion

We explore challenges associated with designing a low-power and high speed active inductor. We focus in particular on sizing issues that arise as the transistor speed is maximized and the current consumption is minimized. We apply the trade-off analysis to design a current-reuse amplifier with an active inductor in 0.18 μm CMOS and show that by systematically working through the sizing issues, a 10 μA amplifier integrated with an active inductor at 1 GHz can be designed with 28 percent less current than previously reported.

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