Design Considerations of a CMOS Envelope Detector for Low Power Wireless Receiver Applications

Jack Ou, Pietro Maris Ferreira

Design Considerations of a CMOS Envelope Detector for Low Power Wireless Receiver Applications

Jack Ou
Department of Electrical and Computer Engineering
California State University Northridge
Northridge, California 91330-8346
Email: jack.ou@csun.edu

Pietro M. Ferreira
GeePs (UMR CNRS 8507)
CentraleSuplec, Université Paris-Saclay
Gif-sur-Yvette, France
Email: maris@ieee.org

***Abstract*—Previous studies have shown that a transistor's transconductance-to-drain-current ratio is useful for optimizing analog circuits. In this paper, we derive an expression that captures the second order distortion generated at the output of an envelope detector. We use the derived expression, along with the nonlinear Taylor series coefficients to design a 3 μA envelope detector in 0.13 μm CMOS process.**

I. Introduction

Nanoscale Metal Oxide Field Effect Transistor (MOSFET) circuit design is driven by power consumption constraints. In 1996, Silveira *et al*. proposed a powerful transconductance-to-drain current (g_m/I_D) method to help designers size up transistors quickly [1]. The so called "g_m/I_D design approach" was originally developed to calculate parameters such as small signal gain and bandwidth [1] and later extended to distortion analysis [2].

A procedure to model a transistor's nonlinearity using g_m/I_D dependent Taylor series coefficients was described in [2]. Analytical expressions that link a transistor's distortion to its own g_m/I_D were discussed in [3] and further explored in [4].

In this paper, instead of seeking to minimize distortion, we *use* distortion to optimize the gain of an envelope detector. Section II reviews the fundamentals of g_m/I_D dependent Taylor series coefficients. Section III derives an expression that captures the second order distortion current generated at the output of an envelope detector. Section IV explores the design space of an envelope detector and discusses the design trade-offs of a 3 μA envelope detector. Section V summarizes the results and explores the limitations of the described technique.

II. Theory

A. g_m/I_D Dependent Taylor Series Coefficients

There are two types of nonlinear behaviors in circuits: hard nonlinearity and soft nonlinearity [5]. Hard nonlinearity is present when the input voltage becomes too large and clipping occurs at the output. The distortion caused by hard nonlinearity is very large. Few applications can tolerate hard nonlinearity. This paper focuses instead on circuits that exhibit primarily characteristics of soft nonlinearity.

Devices that exhibit soft (weakly) nonlinear behavior can be described by means of a power series. For a weakly nonlinear MOS transistor, the drain-to-source current (i_{ds}) is a function of the gate-to-source voltage (v_{gs}) and the drain-to-source voltage (v_{ds}) and can be written as a two-dimensional Taylor series approximation [6]:

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) = g_{m1}v_{gs} + g_{ds1}v_{ds} + g_{m2}v_{gs}^2 + g_{ds2}v_{ds}^2 \\ + x_{11}v_{gs}v_{ds} + g_{m3}v_{gs}^3 + g_{ds3}v_{ds}^3 \\ + x_{12}v_{gs}v_{ds}^2 + x_{21}v_{gs}^2v_{ds} \end{aligned} \quad (1)$$

where the Taylor coefficients (g_{mk}, g_{dsk}, and x_{pq}) are derived from the derivatives of I_{DS}.

g_{mk} is proportional to the derivatives of I_{DS} with respect to $V_{GS}$and is defined as,

$$g_{mk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{GS}^k}. \quad (2)$$

For instance, g_{m1} (i.e. the transconductance) is the first derivative of I_{DS} with respect to V_{GS} (g_{m1}) and g_{m2} is twice the derivative of g_{m1} with respect to V_{GS}.

g_{dsk} represents the derivatives of I_{DS} with respect to V_{DS} and is defined as,

$$g_{dsk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{DS}^k}. \quad (3)$$

g_{ds1}, for example, is the drain-to-source transconductance.

It is interesting to note that i_{ds} depends not only on the powers of v_{gs} and v_{ds}, but also on cross-terms such as x_{pq} which are defined as follows:

$$x_{pq} = \frac{1}{p!q!}\frac{\partial^{p+q} I_{DS}}{\partial V_{GS}^p \partial V_{DS}^q} \quad (4)$$

The cross-term x_{11}, for example, represents the dependence of the transconductance on the drain-source bias voltage and can become significant at high g_m/I_D. x_{12} and x_{21} are higher order derivatives of x_{11}.

It was shown in [2] that g_{mk}, g_{dsk}, and x_{pq} are proportional to transistor width (W). Consequently, a ratio formed by any

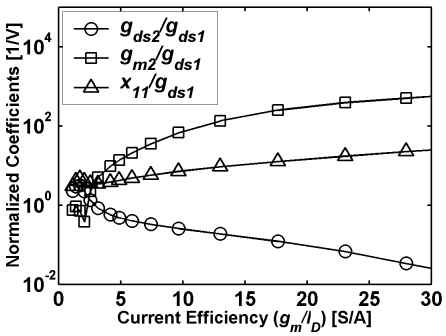

Fig. 1. g_m/I_D dependent ratios formed by two Taylor series coefficients. $I_D = 0.5\mu$A. $L = 600$ nm. $V_{DS} = 0.6$ V. $V_{SB} = 0$ V.

two Taylor series coefficients (e.g. g_{m2}/g_{ds1}) is W independent and depends only on the g_m/I_D of a transistor. Figure 1 shows a collection of g_m/I_D dependent ratios of Taylor series coefficients from a 0.13 μm CMOS process. g_{m2}, g_{ds2} and x_{11} are normalized to g_{ds1} in order to facilitate comparison of second order Taylor series coefficients. Figure 1 shows that for $g_m/I_D > 10$ S/A, $g_{m2}/g_{ds1} > x_{11}/g_{ds1} > g_{ds2}/g_{ds1}$, i.e. g_{m2} is a significant contributor of second order nonlinearity.

III. Analysis

A. Qualitative Understanding of an Envelope Detector

Envelope detectors are frequently used in wireless receivers. Similar to elementary amplifiers, envelope detectors can be categorized as common-drain [8], common-gate [9], and common-source [7] envelope detectors. With the exception of the common-source envelope detector, the source terminal is used either as an input or as an output of the envelope detector. The source terminal carries a non-zero bias voltage. A three-dimensional Taylor series coefficient must be used [10] to capture a transistor's nonlinear dependence on source-to-body voltage (v_{sb}). It can be challenging mathematically to analyze an envelope detector using a three-dimensional Taylor series.

In this paper, we focus instead on a common-source envelope detector with zero V_{SB} shown in Figure 2. We use g_m/I_D dependent two-dimensional Taylor series coefficient to model transistors' nonlinearity. The operation of the envelope detector can be understood as follows. A single tone at f_{in} is coupled to v_{in}. The second-order nonlinear parameters of M_1 produces an *upconverted* tone at $2f_{in}$ and a *downconverted* tone at DC at v_{op}. The DC current of M_3 produces a DC voltage at v_{on}. The output is taken differentially in order to remove the DC component from v_{op}. The upconverted tone and the tone at f_{in} are removed from the desirable signal, i.e. the downconverted tone at DC, with the capacitor across the outputs.

B. Circuit Analysis

As will be shown in Sec. V-A, M_1 is primarily responsible for the nonlinear operation of the envelope detector. Therefore, Fig. 3a can be used to approximate the behavior of the envelope detector. Fig. 3a can be further simplified to Fig. 3b by recognizing that the resistance looking into the source M_2 is R_X, where R_X is

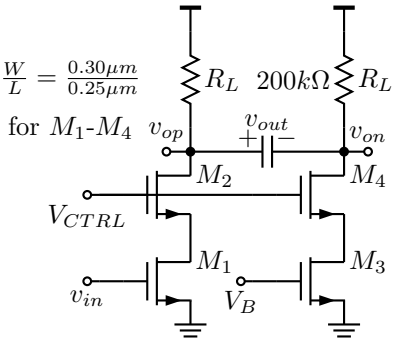

Fig. 2. Schematic of an envelope detector.

$$R_X = \frac{r_{o,2} + R_L}{1 + (g_{m,2} + g_{mb,2})r_{o,2}}. \quad (5)$$

where $g_{m,2}$, $g_{mb,2}$, $r_{o,2}$ are the transconductance, body transconductance and the output resistance of M_2.

Using (1) and expressing v_{ds} in a Taylor series approximation of v_{gs} [2], $i_{ds,2nl}$, the second order distortion of i_{ds} can be approximated as

$$i_{ds,2nl} = -(g_{m2,1} + g_{ds2,1}c_1^2 + x_{11,1}c_1)v_{in}^2, \quad (6)$$

where $g_{m2,1}$, $g_{ds2,1}$ and $x_{11,1}$ are g_{m2}, g_{ds2} and x_{11} of M_1. c_1 is equal to $-g_{m,1}(R_X||r_{o,1})$ and is the self-gain of M_1.

$i_{ds,2nl}$ is generated by M_1 and is converted into a voltage at v_{op} by R_L. It can be shown that if $v_{in} = v_m\cos(\omega_{in}t)$, the second order tones generated at v_{op} are equal to

$$v_{op,2nl} = -R_L(i_{ds,2nl,g_{m2,1}} + i_{ds,2nl,g_{ds2,1}} + i_{ds,2nl,x_{11,1}}), \quad (7)$$

where

$$i_{ds,2nl,g_{m2,1}} = g_{m2,1}\frac{v_m^2}{2} \quad (8)$$

$$i_{ds,2nl,g_{ds2,1}} = g_{ds2,1}c_1^2\frac{v_m^2}{2} \quad (9)$$

$$i_{ds,2nl,x_{11,1}} = x_{11,1}c_1\frac{v_m^2}{2} \quad (10)$$

$i_{ds,2nl,g_{m2,1}}$, $i_{ds,2nl,g_{ds2,1}}$, and $i_{ds,2nl,x_{11,1}}$ are second order distortion of i_{ds} due to $g_{m2,1}$, $g_{ds2,1}$ and $x_{11,1}$.

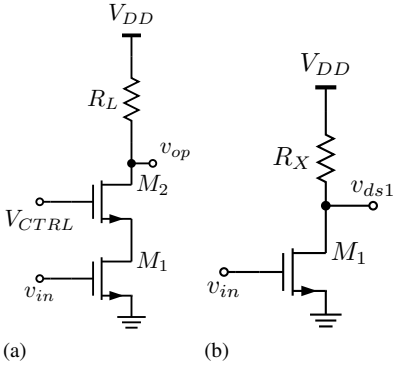

Fig. 3. (a) Equivalent circuit for the envelope detector in Fig. 2. (b) Equivalent circuit for analyzing distortion of M_1.

IV. DESIGN

The analysis in Sec.III shows that the envelope detector accomplishes spectrum translation through the second order nonlinearity of M_1, which is governed by the selection of L_1, $g_{m1,1}/I_{D,1}$ and $I_{D,1}$. In this section, we describe considerations that influence the selection of L_1, $g_{m1,1}/I_{D,1}$ and $I_{D,1}$.

A. Choice of L_1 and $I_{D,1}$

We start exploring the design space of L_1 by assuming that $I_{D,1}$ is 5 μA. Figure 4a-4b suggest that both speed (f_T) and current density are increased as L_1 is reduced. Thus, assuming that $I_{D,1}$ is constant, W_1 is reduced as L_1 is reduced (Fig. 4c).

For 0.13 μm CMOS, the minimum width allowed by the design kit is 280 nm. Figure 4b shows that the current density at $L = 250$ nm is 5 μA/μm. Using a current density of 5 μA/μm, W_1 (the width of M_1) as a function of I_{D1} is plotted in Fig. 4d. Figure 4d suggests that $I_{D,1}$ should exceed or equal to 1.5μA if W_1 were to exceed the minimum width permitted by the 0.13 μm design kit.

B. Choice of g_m/I_D

Section III shows that $i_{ds,2nl}$ is determined by $g_{m2,1}$, $g_{ds2,1}$, and $x_{11,1}$. Therefore, the design space for g_m/I_D of M_1 (i.e. $g_{m1,1}/I_{D1}$) should be explored. Figure 5 shows the dependence of $i_{ds,2nl}$ (the second order distortion of i_{ds}) as a function of $g_{m1,1}/I_{D1}$. Since I_{D1} is constant, c_1, the self-gain of M_1, is increased as the g_m/I_D of M_1 increases (Fig. 5a). Figure 5b, Fig. 5c and Fig. 5d are significant because they show that $g_{m2,1}$ is the primary contributor to $i_{ds,2nl}$ among the second-order nonlinear parameters. Since the contribution of $i_{ds,2nl}$ due to $g_{m2,1}$ increases with $g_{m1,1}/I_1$ (Fig. 5d), the gain (Eq. 11) of the envelope detector can be increased by increasing the g_m/I_D of M_1 at the expense of reducing the transit frequency of M_1, and hence the frequency range of the envelope detector.

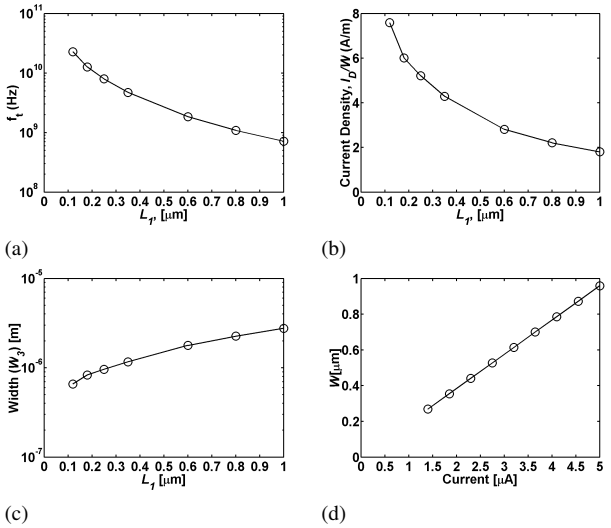

Fig. 4. Current density, W_1, f_{T1} plotted as a function of L_1. I_{D1} is 5 μA and $g_m/I_D = 20$ S/A for (a)-(c). W_1 is plotted as a function of I_{D1} in (d) assuming that g_m/I_D for M_1 is 20 S/A, L_1=250 nm, V_{DS}=0.6 V and V_{SB}=0.0 V.

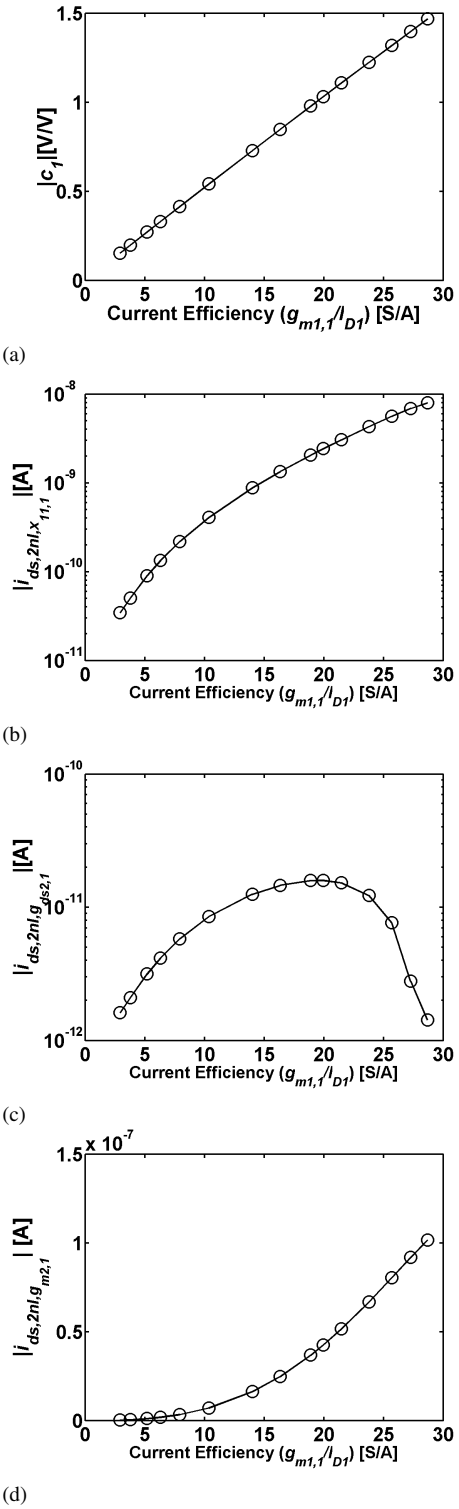

Fig. 5. (a) c_1 versus g_m/I_D of M_1. (b) $x_{11,1}$ contribution to $i_{ds,2nl}$. (c) $g_{ds2,1}$ contribution to $i_{ds,2nl}$. (d) $g_{m2,1}$ contribution to $i_{ds,2nl}$. $i_{ds,2nl}$ represents the second order distortion of i_{ds}. L_1 is 250 nm and $I_{D,1}$ is 1.5 μA.

V. SIMULATION RESULTS

A. Nonlinearity of M_2

It is assumed in Sec. III that M_1 is primarily responsible for the nonlinear operation of the envelope detector. To verify

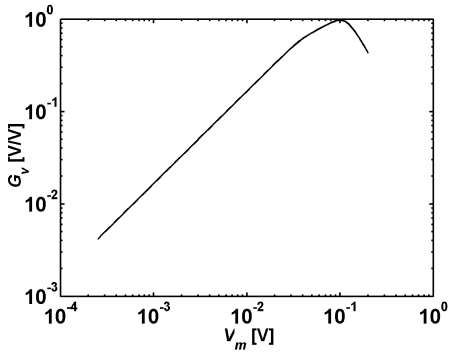

Fig. 6. Conversion gain as a function of v_m.

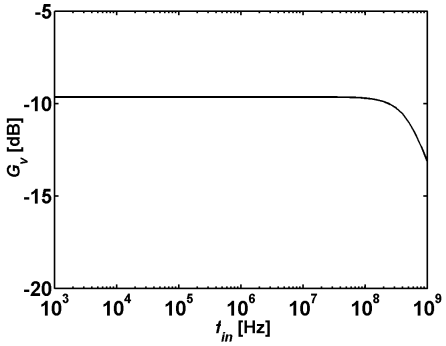

Fig. 7. Frequency dependence of G_v.

this assumption, a sinusoid with a magnitude of 20 mV and a frequency of 1 kHz is applied to v_{in}. A distortion summary is generated at v_{out} using SpectreRF. The total second order distortion at v_{out} is 6.598 mV with a contribution of 6.483 mV from M_1, a contribution of 0.115 mV from M_2. M_3 and $M4$ do not contribute any second order distortion. M_1 is primarily responsible for the second order nonlinearity at v_{out}.

B. g_m/I_D Analysis

The second order nonlinearity contribution of M_1 is calculated by applying a sinusoidal tone with a 20 mV magnitude at v_{in}. $v_{op,2nl}$ is computed using (7) and compared with that obtained using the Period Steady State (PSS) analysis. The second order distortion computed using the g_m/I_D method is 8.06 mV and the second order distortion computed using PSS is 6.48 mV.

C. Dependence on Input Amplitude

Equation (7) shows that $v_{op,2nl}$ is proportional to v_m^2. The conversion gain (G_v) for an envelope detector can be defined by dividing $v_{op,2nl}$ by v_m.

$$G_v = \frac{v_{op,2nl}}{v_m} = -\frac{R_L}{2}(g_{m2,1} + g_{ds2,1}c_1^2 + x_{11}c_1)v_m \quad (11)$$

Equation (11) shows that G_v is proportional to v_m. Figure 6 shows the PSS simulation of G_v as a function of v_m. G_v is proportional to v_m for $v_m \leq 100$mV. Since the drain current (i_{ds}) is approximated by a two-dimensional Taylor series in (1), the approximation becomes less accurate as v_{gs} increases in magnitude [2]. As v_m exceeds 100 mV, G_v is reduced as the Taylor series approximation becomes less accurate.

D. Frequency Dependence

The two-dimensional Taylor series approximation ignores frequency dependence introduced by reactive elements. While this approach may be sufficient for low frequency circuits, the approximation becomes less accurate as frequency increases. At higher frequencies, the frequency dependence of reactive components can be calculated. In order to gauge the frequency dependence of the envelope detector, the input frequency of the sinusoid is swept from 1 kHz to 1 GHz. Figure 7 shows that G_v remains flat up to 100 MHz.

VI. Conclusion

In this paper, we derive an expression that captures second order distortion generated at the output of an envelope detector. We explore the design space to optimize the conversion gain. We show that by systematically working through various design parameters, a 3 μA envelope detector can be designed in 0.13 μm CMOS process.

References

[1] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA," *IEEE J. Solid-State Circuits*, vol.31, no. 9, pp. 1314-1319, Sept. 1996.

[2] J. Ou and F. Farahmand, "Transconductance/drain current based distortion analysis for analog CMOS integrated circuits," New Circuits and Systems Conference (NEWCAS), 2012 IEEE 10th International, Montreal, QC, 2012, pp. 61-64.

[3] P. G. A. Jespers and B. Murmann, "Calculation of MOSFET distortion using the transconductance-to-current ratio (g_m/I_D)," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 529-532.

[4] I.M. Filanovsky and L.B. Oliveira, "Using 'Reconciliation' Model for Calculation of Harmonics in a MOS Transistor Stage Operating in Moderate Inversion," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, 2016.

[5] W. Sansen, "Analog Design Essentials", Springer, 2008, ch. 18, pp. 521-522.

[6] S. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling", *IEEE J. Solid-State Circuits*, Vol. 43, No.6, June 2008.

[7] XiongChuan Huang, P. Harpe, G. Dolmans, H. de Groot and J. R. Long, "A 780 to 950 MHz, 64 to 146 μW Power-Scalable Synchronized-Switching OOK Receiver for Wireless Event-Driven Applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, pp. 1135-1147, May 2014.

[8] S. Moazzeni, M. Sawan and G. E. R. Cowan, "An Ultra-Low-Power Energy-Efficient Dual-Mode Wake-Up Receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 517-526, Feb. 2015.

[9] M. Zgaren and M. Sawan, "A Low-Power Dual-Injection-Locked RF Receiver With FSK-to-OOK Conversion for Biomedical Implants," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2748-2758, Nov. 2015.

[10] J. Borremans, L. D. Locht, P. Wambacq and Y. Rolain, "Nonlinearity Analysis of Analog/RF Circuits Using Combined Multisine and Volterra Analysis," 2007 Design, Automation and Test in Europe Conference and Exhibition, Nice, 2007, pp. 1-6.