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# A Temperature-Aware Analysis of Latched Comparators for Smart Vehicle Applications

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## ABSTRACT

The challenges of the Internet of Things (IoT) in an urban environment are driven by smart vehicles which need to be able to efficiently sense and communicate with other nearby vehicles. System-on-chip (SoC) applications in the automotive market have strict circuit performances and reliability requirements for a temperature range of up to 175 $^{o}$C. This work proposes an analysis of latched-comparators performance considering process variability and temperature variation. State-of-the-art StrongArm and Double-Tail comparators are designed using an XH018 technology. Post-layout simulation results are drawn in order to validate the proposed temperature-aware analysis. Besides the known advantages of the Double-Tail comparator, this work demonstrates that such a comparator has a serious drawback under harsh environments. At 175 $^{o}$C, the Double-Tail presents a 3.1 ns worst case delay and 1.4 mV offset, while StrongArm shows 2.7 ns and 2.7 mV respectively. Moreover, the Double-Tail's input-referred noise achieves worst-case levels of 0.89 mV, the StrongArm's noise is below 0.4 mV. Therefore, the Double-Tail proved to be less reliable than the StrongArm and also foretells critical failure conditions in harsh environments.

## 1 INTRODUCTION

The advent of the Internet of Things (IoT) has brought the need for novel studies in order to conform to its extensive requirements, driven specifically by the Smart Vehicle industry. Smart vehicles must be able to efficiently sense and communicate with other nearby vehicles, including car, buses and trucks. For obvious reasons, the design and specification of microelectronic circuits, which are used in these applications, are regulated by a large number of strict security and safety standards. Reliability and robustness in the device operation must be ensured for harsh environments [5], including the required operating temperature range from -40 $^{o}$C to 175 $^{o}$C. This temperature range is arguably the most difficult environment challenge for electronics in the automotive industry [4]. Hence, in order to meet the IoT challenge, smart vehicles must integrate high performance electronics over a wide temperature range.

In the domain of vehicle smart sensing, the analog to digital interface is also a challenge. Analog-to-digital converters (ADCs) should remain reliable even under performance variation [2]. One of the most common architecture is the Successive Approximation Register ADC (SAR), which is designed with state of the art comparator circuits. The most common comparator designs are the StrongArm (SA) [11] and the Double-Tail (DT) latched comparator [12]. Many studies compare both SA and DT topologies, compiling a series of well-defined design parameters and considerations, even proposing changes to better increase the comparators' performances. However, they lack the analysis of performance variability considering temperature variation.

The objective of this work is then to propose a temperature-aware analysis of performance variability in state-of-the-art latched SA and DT comparators, which are designed using XH018 process technology from the XFAB Silicon Foundries. XH018 technology is ideal for system-on-chip (SoC) applications in the automotive market such as control devices inside combustion engine compartments or electric engine housings with temperature range up to 175 $^{o}$C, as well as embedded low-voltage applications in the communications, consumer and industrial market [13]. This work overviews the temperature effects on MOS devices and extends it to cover the comparators design parameters in order to address performance variations (i.e. offset, delay and noise).

Sec. 2 presents a detailed analysis of the temperature variations on both comparators. Subsec. 2.1 presents a brief introduction of temperature effects on MOS devices. Subsec. 2.2 and 2.3 include a study of the temperature effects on comparators' delay. Subsec. 2.4 evaluates offset tendencies in both topologies. Sec. 3 presents post-layout Monte Carlo simulations considering temperature variation

for both comparators' performance. Finally, conclusions concerning the theory and post-layout simulated results are drawn.

## 2 TEMPERATURE DEPENDENT ANALYSIS

### 2.1 Temperature Effects

The effects of temperature on system dynamics and behavior have been widely studied. Since 1995, C. Park *et al.* have described the trade-off between mobility ($\mu$) and threshold voltage ($V_{th}$) under temperature variation [9]. This trade-off causes a varying temperature dependency on the transistor current. In the 180 nm XH018 XFAB technology, as in other usual CMOS technologies, for transistors operating with a $V_{GS}$ voltage significantly greater than the threshold voltage, their current will always decrease with temperature [4].

According to Mathiessen's equation and the BSIM device model, the transistor's mobility ($\mu$) and threshold voltage ($V_{th}$) vary with temperature with the following expressions:

$$\mu\left(T\right) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-\beta_\mu} \text{[4]}, \tag{1}$$

$$V_{th}\left(T\right) = V_{th0} + \alpha_{V_{th}}\left(T - T_0\right) \text{ [8]}, \tag{2}$$

where $\alpha_{V_{th}}$ in $mV/K$ and $\beta_\mu$ are technology-dependent temperature coefficients.

In order to find temperature coefficients, electrical simulations were carried out with approximately the same conditions as the transistors in the differential pairs of comparators. In other words $V_{GS} = \frac{V_{DD}}{2} = 900\ mV$ and $V_{DS} = V_{DD} = 1.8\ V$ while maintaining the same sizing. Extracted temperature coefficients in the XH018 180 nm technology using n-type transistor are: $\alpha_{V_{th}} \approx -0.7\ mV/K$, $\beta_\mu \approx 1.5$. These results are required when deriving the system dependencies in the comparators.

### 2.2 StrongArm Delay

The SA comparator, shown in Figure 1(a), is the improved version as designed by [11]. The proposed temperature-aware analysis is based on a previous study presented by Babayan-Mashhadi and Lotfi on the delay analysis of SA and DT comparators [1]. The operation of the SA comparator can be separated into three main phases: a pre-charge, a decision delay and a regeneration phase. The pre-charge phase occurs for CLK = 0 and the two latter for CLK = 1. In the pre-charge phase, switches S1-S4 are turned on charging nodes $X_1$, $X_2$, $V_{OUTp}$, and $V_{OUTm}$ to $V_{DD}$. It will be assumed that by the time CLK rises to 1 these nodes are completely charged. This is a very plausible assumption considering a 100 MHz operating frequency for the comparator.

During the decision delay phase, $M_7$ turns on permitting transistors $M_1$ and $M_2$ to conduct. Each branch current, i.e. $I_{DM1}$ and $I_{DM2}$, begins to discharge nodes $X_1$ and $X_2$. Assuming $V_{INp} > V_{INm}$, the node $X_1$ will discharge faster until it reaches the voltage level of $V_{DD} - V_{TH}$, considering a node capacitance of $C_{LX}$ this would cause a first delay time $t_{o1}$ described by,

$$t_{o1} = \frac{C_{LX} V_{THN}}{I_{DM1,2}}, \tag{3}$$

where since the voltage difference is too small in this case,

$$I_{DM1,2} = I_{bias} + g_m \Delta V \approx I_{bias}, \tag{4}$$

where $I_{DM1,2}$ is the total current that passes through either the transistor $M_1$ or $M_2$, $g_m$ is the transistor's transconductance; and $I_{bias}$ is the bias current of the transistors of the differential pair.

When employing the quadratic model for the MOS transistor,

$$I_{bias} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{CM} - V_{TH}\right)^2. \tag{5}$$

where $V_{CM}$ is the common mode bias voltage at the inputs of the comparator.

As soon as $X_1$ reaches the voltage level of $V_{DD} - V_{THN}$, the transistor $M_3$ begins to conduct and successively discharges the node $V_{OUTm}$. This next step adds an extra delay time $t_{o2}$ as

$$t_{o2} = \frac{C_{Lo}\left|V_{THP}\right|}{I_{DM1,2}}. \tag{6}$$

The total time ($t_o$) to the latch enters in regeneration phase is then calculated by the $t_{o1} + t_{o2}$. Considering that $|V_{THP}| \approx V_{THN} = V_{TH}$ and $C_{Lo} \approx C_{LX} = C_L$,

$$t_o = t_{o1} + t_{o2} = \frac{2 \cdot C_L V_{TH}}{I_{DM1,2}}. \tag{7}$$

The $t_o$ temperature dependency is obtained by analyzing the two temperature-dependent parameters $V_{TH}$ and $\mu$. The $V_{TH}$ and $\mu$ dependencies described in Eq (2) and (1) are used to derive the $t_o$ temperature dependency as

$$\frac{\partial t_o}{\partial T} = 2 \cdot \frac{C_L}{I_{bias}}\left(\alpha_{V_{TH}} - \alpha_{I_{bias}}\frac{V_{TH}}{I_{bias}}\right), \tag{8}$$

where $\alpha_{I_{bias}}$ and $\alpha_{V_{TH}}$ are the temperature coefficients. The value of $\alpha_{I_{bias}}$ can be found using,

$$\alpha_{I_{bias}} = \frac{\partial I_{bias}}{\partial T} = \frac{1}{2} g_m \left(-\beta_\mu \frac{V_{CM} - V_{TH}}{T} - 2 \cdot \alpha_{V_{TH}}\right), \tag{9}$$

in order to prove that $t_o$ delay increases as temperature increases, it is sufficient to prove that

$$\alpha_{V_{TH}} - \alpha_{I_{bias}}\frac{V_{TH}}{I_{bias}} > 0. \tag{10}$$

Considering the average $V_{TH} \approx 400\ mV$ in the XH018 technology and a $g_m$ in the order of magnitude of hundreds of $\mu S$ and $I_{bias}$ in the order of magnitude of tens of $\mu A$, one may conclude that the condition in Eq. (10) is met.

### 2.3 Double-Tail Delay

The DT-comparator topology analyzed in this study was first proposed by Schinkel *et al.* in [12]. DT comparators were introduced because of their improved performance, specially in kick-back noise. The DT comparator's behavior can be separated into three phases: pre-charge, decision, and regeneration. Figure 1(b) presents a schematic illustration of the DT topology.

In the pre-charge phase, CLK = 0 switches $M_3$ and $M_4$ to charge the nodes $f_p$ and $f_n$ to $V_{DD}$ respectively. It is assumed that these nodes are completely charged by the time of CLK = 1. These nodes charged to $V_{DD}$ force the transistors $M_{R1}$ and $M_{R2}$ to conduct. Thus, the two output nodes are forced to ground.

In this case, the decision ($t_o$) delay can be identified as the time it takes either the $f_p$ or the $f_n$ node voltage to discharge from $V_{DD}$ to $V_{TH}$. As soon as $M_{tail1}$ begins to conduct, $M_1$ and $M_2$ begin to discharge $f_p$ and $f_n$ respectively. Considering $V_{INp} > V_{INm}$, $f_p$ node

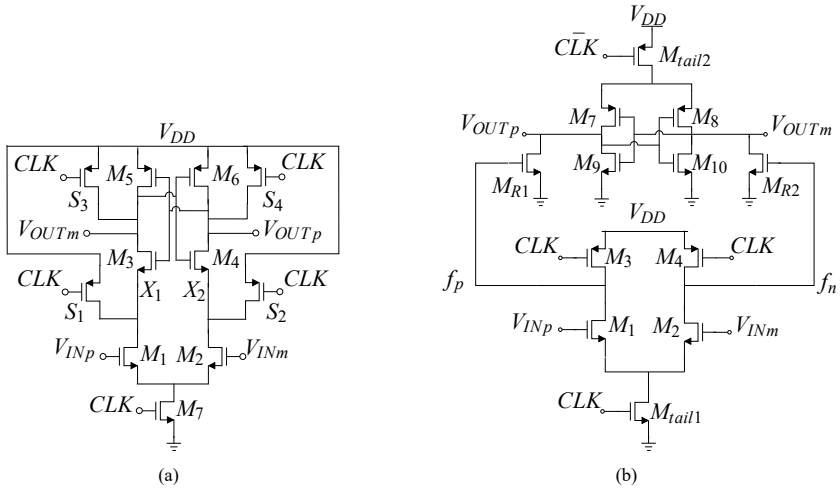


**Figure 1: Comparator Schematic of (a) StrongArm; (b) Double-tail.**

discharges faster than $f_n$. As soon as $f_p$ reaches the voltage value of $V_{TH}$, $M_{R1}$ no longer forces the ground voltage on $V_{OUTp}$; and the comparator latches in its regenerative phase. In order to calculate the decision delay time $t_o$ in this topology, it is considered the variation in the voltage $f_p$ and its final voltage $V_{TH}$ as

$$V_{DD} - \frac{I_D}{C_L} t_o = V_{TH}, \tag{11}$$

where $I_D \approx I_{bias}$ is the current provided by $M_1$; and $C_L$ is the output node capacitance. $I_{bias}$ being the bias current of the transistors in the differential pair.

Considering the temperature variation of the current $I_{bias}$ and $V_{TH}$, the temperature effects on the delay are due to a decrease of $V_{TH}$ and of $I_{bias}$, that implies a decrease on the discharge rate of the $f_p$ node voltage. This combined effect increases even more the delay in both cases. To clearly demonstrate the delay $t_o$, the following relation is found

$$t_o = \frac{C_L \left(V_{DD} - V_{TH}\right)}{I_{bias}}. \tag{12}$$

In order to derive a temperature-sensitive behavior, the total $t_o$ delay is derived with respect to the temperature as

$$\frac{\partial t_o}{\partial T} = \frac{C_L}{I_{bias}} \left( -\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{V_{DD} - V_{TH}}{I_{bias}} \right), \tag{13}$$

where the rise in the $t_o$ delay in relation to temperature increase is proven by showing that

$$-\alpha_{V_{TH}} - \alpha_{I_{bias}} \frac{V_{DD} - V_{TH}}{I_{bias}} > 0. \tag{14}$$

Considering the same values as previously, the condition in Eq. (10) is met and the delay will always increase with temperature. In the instant that $V_{DS}$ drops low enough, the transistor changes its operating region to the ohmic region. From this point, the current will continue to reduce independent of the temperature effects. In other words, it can be assumed that delay time always increases when the temperature increases. Eq (13) also shows that theoretically the $t_o$ delay in the DT comparator is much more sensitive to temperature variations than in SA comparators.

In both the SA and the DT comparators, one can identify the effects on $t_o$ as the main agent of the system delay degradation. However, it is possible to show how the delay of the regeneration phase ($t_{latch}$) is also affected by the temperature variations. In fact both SA and DT comparators have similar $t_{latch}$ degradation. The time it takes for the differential signal to regenerate to a stable value is inversely dependent on the the gain of the back to back inverters as shown by the equation developed in [14],

$$t_{latch} = \frac{C_L}{G_m} \ln\left( \frac{V_{DD}/2}{\Delta V_o} \right), \tag{15}$$

where $C_L$ represents the capacitance of the output node, $G_m$ the gain of the inverters and $\Delta V_o$ the voltage difference between the output nodes. It can then be deduced that by increasing the temperature, and thus reducing the gain of the transistors, $t_{latch}$ is increased.

## 2.4 Comparator Offset

Input-referred offset in latched comparators can be separated into two main parts, the offset coming from the mismatch in the differential pair and in the latch [6] in the following way

$$V_{OS,i-total} = \sqrt{V_{OS-diffpair}^2 + \frac{1}{G^2} V_{OS-latch}^2}, \tag{16}$$

where $V_{OS-diffpair}$ and $V_{OS-latch}$ are the offsets in each stage and $G$ the gain before the latch. In the case of the SA comparator this gain comes from the differential pair, but for the DT comparator it is the differential-pair gain multiplied by the gain from $M_{R1}$ or $M_{R2}$transistors. If one considers that the gain $G$ is significant enough to neglect the effects of the latch offset, a simple differential pair mismatch analysis can be done. The standard deviation of the offset in a differential pair is given by

$$\sigma^2 V_{OS-diffpair} = \frac{\sigma^2 \Delta I_D}{g_m^2} [3], \tag{17}$$

where $\sigma^2\Delta I_D$ is given by,

$$\sigma^2\Delta I_D = \frac{2}{WL}\left[g_m^2 A_{VT0}^2 + \left(\frac{I_D}{K}\right)^2 A_K^2\right], \quad (18)$$

where $K = \mu C_{ox}\left(\frac{W}{L}\right)$; $A_{VT0}$ is a technology-defined variability constant for the $V_{TH}$ and $A_K$ for the $K$. One can find the offset of the differential pair as

$$\sigma^2 V_{OS-diffpair} = \frac{2}{WL}\left[A_{VT0}^2 + \left(\frac{I_D}{Kg_m}\right)^2 A_K^2\right], \quad (19)$$

Assuming the comparators' layout is compact enough, the temperature variation equally affects all transistors. In fact, all transistors maintain the same temperature gradient; and temperature effects behave as a common-mode variation. One may assume that $A_{VT0}$ and $A_K$ remain constant with temperature and are process dependent [14]. Although the coefficients multiplying $A_K^2$ are temperature variant, $A_{VT0}^2$ will always dominate. As a result, the offset voltage in both topologies is mostly unaffected by temperature variation in the differential pair. Since the differential pair provides the biggest impact on the offset voltage, it is reasonable to conclude that the offset will present a negligible dependence on temperature.

## 3 POST-LAYOUT RESULTS

Both SA and DT comparators were designed using the XH018 180 nm technology which is measured and modeled for the $-40\ ^o$C to $175\ ^o$C temperature range [13]. Table 1 presents transistor sizing for SA (see Fig 1(a)) and DT comparators (see Fig 1(b)). Then, the layout of both comparator topologies is implemented using state of the art techniques. To efficiently compare both topologies, the layout is carried out minimizing mismatch, achieving a similar area, and placing I/O in same positions. Figure 2(a) shows the SA comparator layout, having an area of 49 x 10 $\mu$m$^2$. Figure 2(b) shows the DT comparator layout, having an area of 52 x 10 $\mu$m$^2$.

**Table 1: Transistor Sizing of SA and DT Comparators (W x L).**

| SA [11] | | DT [12] | |
|---|---|---|---|
| $M_{1-2}$ | 14.4 $\mu$m x 720 nm | $M_{1-2}$ | 14.4 $\mu$m x 720 nm |
| $M_{3-6}$ | 7.2 $\mu$m x 720 nm | $M_{3-4}$ | 1.1 $\mu$m x 180 nm |
| $M_7$ | 1.1 $\mu$m x 180 nm | $M_{R1,2}$ | 3.6 $\mu$m x 720 nm |
| $S_{1-4}$ | 1.1 $\mu$m x 180 nm | $M_{7-10}$ | 7.2 $\mu$m x 720 nm |
| | | $M_{tail1,2}$ | 1.1 $\mu$m x 180 nm |

To prove the temperature dependency of $t_o$ described in Subsec. 2.2 and 2.3, a first experiment is drawn based on a post-layout transient simulation. The simulation parameters are: 100 *MHz* clock, a 1*ps* strobe period, a common mode voltage of 900 *mV* and a differential voltage of 10 mV between input nodes. At the clock's rising edge, the simulation time is started as 0 ns in the X-axis; and it runs until 1 ns (sufficient time to observe $t_o$ for a 10 *mV* differential input). For the SA comparator, $X_1$ and $V_{OUTm}$ nodes are inspected (Y-axis). For the DT comparator, $f_p$ and $V_{OUTp}$ nodes are inspected (Y-axis). It is expected that $X_1$ and $f_p$ discharge until $t_o$ according to Eq. (7) for SA comparator and Eq. (12) for DT comparator. Figure 3 shows SA and DT post-layout simulation results for temperatures

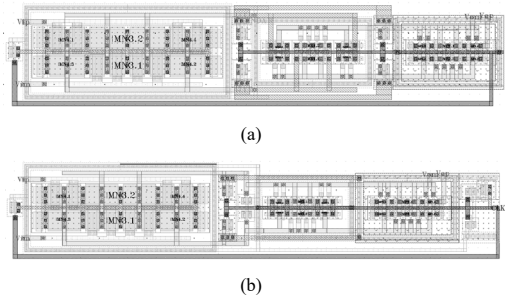


**Figure 2: Latched comparators' layout of (a) SA having an area of 49 x 10 $\mu$m$^2$ and (b) DT having 52 x 10 $\mu$m$^2$.**

of $-40\ ^o$C (dashed blue line), 27 $^o$C (continuous black line), and 175 $^o$C (dashed-dotted red line).

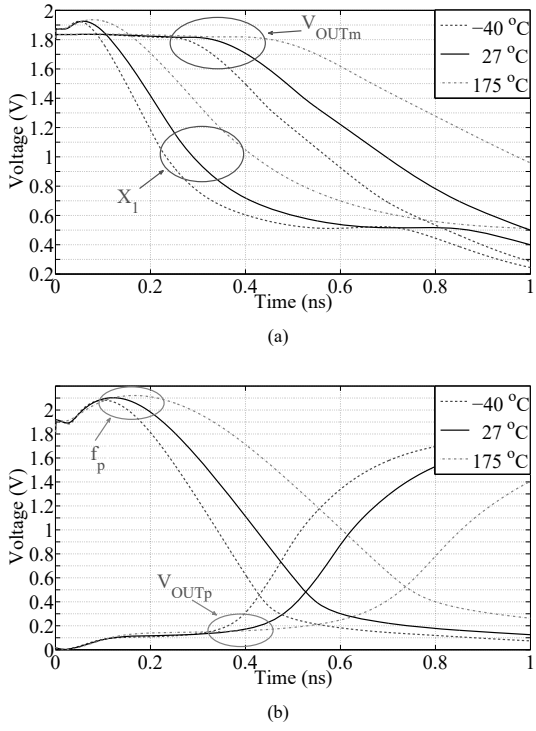


**Figure 3: Post-layout transient simulation of (a) $X_1$ and $V_{OUTm}$ for SA; and (b) $f_p$ and $V_{OUTp}$ for DT comparators in a temperature variation of $-40\ ^o$C (dashed blue line), 27 $^o$C (continuous black line), and 175 $^o$C (dashed-dotted red line).**

Figure 3(a) highlights SA operation when decision is being taken. One can notice that the $V_{OUTm}$ begins to latch around the same instant of time as the node $X_1$ achieves the voltage level $V_{DD} - 2{\cdot}V_{TH}$. This voltage level represents that by the time $V_{OUTm}$ decreases to $V_{DD} - V_{TH}$, the node $X_1$ discharges two times the value of $V_{TH}$. This point indicates the beginning of the latching phase; and it marks $t_o$

for SA comparator. Among temperature variation curves, it is remarkable the $t_o$ increase due a decreasing in the discharge rate and in the transistor $V_{TH}$. This validates the analysis presented in Subsec. 2.2 derived in Eq (8).

Figure 3(b) highlights DT operation while $f_p$ is discharging and $V_{OUTp}$ is rising. The delay $t_o$ can be identified as the time the $f_p$ node voltage reaches around one $V_{TH}$. Also, DT comparator latching is delayed as temperature increases due to the decrease of the discharge rate and the threshold voltage. This validates the analysis presented in Subsec. 2.3 derived in Eq (13).

Since latched comparators are linear time-varying circuits, the following experiments are run using a post-layout periodic-steady-state simulation. The test-bench used for the presented results was inspired by [7] and [10]. Delay, offset, and power consumption are evaluated in a 151-point Monte Carlo simulation for a 11-point temperature variation in a range from $-40\ ^o$C to $175\ ^o$C. The test-bench proposed in [7] is able to put latched comparator as close as possible of its metastable operation. In this case it achieves maximum delay for an input differential voltage equal to the comparator offset voltage. Power consumption is obtained by the RMS power consumed for one cycle in a periodic-steady-state regime.

Figure 4 presents the statistical results of the post-layout comparator delay in both architectures. The data is represented as a plot of the average delay values with an error bar representing three times the standard deviation for each temperature point. The results are presented as solid line for the SA delay and dotted line for the DT delay. While temperature increases, a linear increase of the mean delay is noticeable. This behavior was predicted in the previous transient simulations and is in agreement with the theoretical analysis presented in Eq. (8) and (13) (see Sec. 2 for details). From a linear fit, a delay temperature-coefficient of 6.3 *ps*/*K* for the SA comparator and 6.29 *ps*/*K* for the DT comparator is found. In fact, both SA and DT comparators delays vary with the same temperature coefficient. However, the DT comparator is always slower due to its larger $t_o$ for all temperatures. The temperature effect in delay standard deviation is diminished in the DT comparator, this may be due to the much faster regeneration phase as compared to the SA comparator. Additionally, a worse case delay greater than 2.5 *ns* (a quarter of clock period) is found. These results might suggest a comparator failure in high-temperature operations.

The average offset of both comparators is around zero as expected, that is why Figure 5 shows only the standard deviation of the comparators' input-referred offset ($3\sigma V_{OS,i-total}$). The solid line is the SA $3\sigma V_{OS,i-total}$; and the dotted one is the DT $3\sigma V_{OS,i-total}$. The $3\sigma V_{OS,i-total}$ data over temperature does not change significantly. This behavior validates the theory as predicted in Eq (19) in Sec. 2. One may concludes that the SA $3\sigma V_{OS,i-total}$ is less sensitive to temperature variation. Even if the SA presents a higher $3\sigma V_{OS,i-total}$ than the DT, due to the additional gain provided by the $M_{R1,2}$ transistors, DT $3\sigma V_{OS,i-total}$ variation is three times bigger than SA $3\sigma V_{OS,i-total}$ variation over the temperature range. In order to have a complete understanding of the input-referred offset, post-fabrication testing must be done. The input-offset's variability constants in Eq. 19 present a strong process dependency.

In high-temperature conditions, thermal noise becomes a major issue for a correct decision as it is statistically added to the comparator offset. The output-referred noise is estimated from a

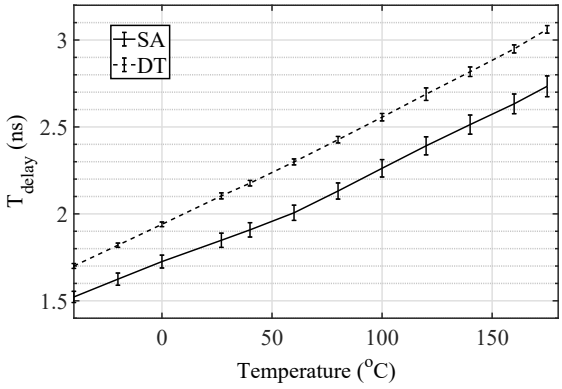


**Figure 4: A 151-points Monte Carlo post-layout simulation for a 11-points temperature variation in a range from $-40\ ^o$C to $175\ ^o$C for SA and DT comparator mean delay with a $3\sigma$ error bar.**

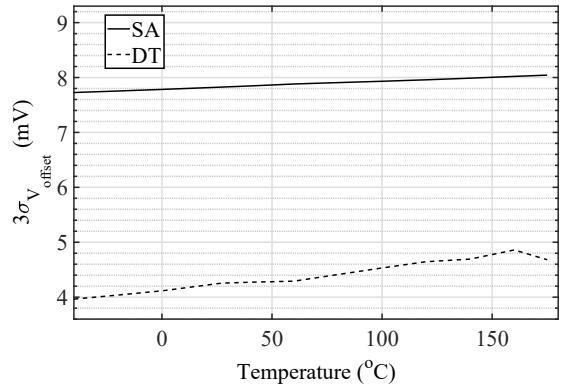


**Figure 5: A 151-points Monte Carlo post-layout simulation for a 11-point temperature variation in a range from $-40\ ^o$C to $175\ ^o$C for SA and DT comparator $3\sigma V_{OS,i-total}$.**

periodic noise analysis. Input-referred noise is estimated from the output-referred noise and the comparator gain. This gain is obtained from a periodic AC analysis evaluated at the instant the comparator achieves its decision threshold (i.e. $V_{DD}/2$) at the output nodes. Details of the test-bench setup are presented in [7] and [10].

Figure 6 presents the mean and the worst case (WC) of SA and DT input-referred noise obtained from a 151-points Monte Carlo post-layout simulation for a 11-point temperature variation.The WC is the defined by $\mu_{n,i} + 3\sigma_{n,i}$. The solid line is the SA mean and WC; and the dotted one is the DT mean and WC. Input-referred noise WC results are marked with squares in Figure 6. Since thermal noise is linearly dependent on temperature, SA and DT input-referred noise increase linearly; but the standard deviation increases slightly faster than the mean. The DT presents more noise than the SA; and DT noise increases at a much faster rate. Considering noise as an additive source of decision errors as offset voltage, the lower offset voltage of the DT comparator is payed off by a higher noise.

This trade-off is due to the extra DT transistors increasing gain, reducing offset voltage, but generating more noise. Indeed, thermal noise under temperature instability may vary input voltage incurring in a bit-flip and a Single Event Upset (SEU) [5]. At the best of our knowledge, this drawback is first revealed in this work.

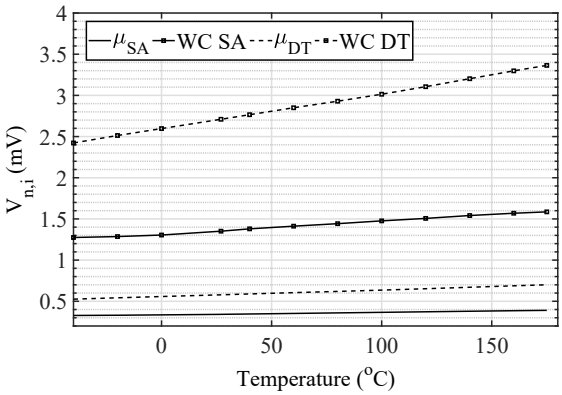


**Figure 6: A 151-points Monte Carlo post-layout simulation for a 11-points temperature variation in a range from $-40\ ^{o}$C to $175\ ^{o}$C for SA (solid line) and DT (dotted line) comparator input-referred noise mean and worst case (WC) (square marks).**

To summarizes the SA and DT performance comparison, Table 2 draws performance trade-offs under temperature variation. A linear fit of the presented post-layout simulations for a 11-point temperature variation is done in order to determine a temperature coefficient for each SA and DT comparator characteristic. One may conclude that the DT comparator achieves a smaller offset in the expense of power consumption and noise. DT offset and noise has a bigger temperature coefficient than SA. Both SA and DT comparator's delays are equally sensitive to temperature variation. At high temperatures, however, the variation of the comparators' characteristics may incur in a circuit failure. However, the DT comparator is found to be less reliable than the SA comparator at these temperatures.

**Table 2: Performance Comparison of Comparators in 180nm Technology and 1.8V Supply Voltage**

| Performance | SA [11] | DT[12] |
|---|---|---|
| *Total Delay*/10 $^{o}C$ | 63 *ps* | 62.9 *ps* |
| $\sigma V_{OS,i-total}$/10 $^{o}C$ | 4.88 $\mu V$ | 13.9 $\mu V$ |
| $\sigma_{n,i}$ $\sigma$/10 $^{o}C$ | 4.1 $\mu V$ | 11.8 $\mu V$ |
| $\sigma_{n,i}$ $\mu$/10 $^{o}C$ | 3.0 $\mu V$ | 8.0 $\mu V$ |
| *Average Power Consumption* | 0.35 *mW* | 1.7 *mW* |

## 4 CONCLUSIONS

This work proposed a temperature-aware analysis of performance variability in state-of-the-art latched SA and DT comparators. At $175\ ^{o}$C, the DT presented a 3.1 ns worst case delay and 1.4 mV offset, while the SA showed 2.7 ns and 2.7 mV respectively. Moreover, the DT's input-referred noise achieves worst-case levels of 0.89 mV; while SA's noise is below 0.4 mV. Post-layout simulations validated the delay analysis, which demonstrated a high sensitive to temperature variation incurring in circuit failure at high temperatures. Offset voltage was found to be less sensitive to temperature, however it is overcome by input-referred noise. Combining comparators' offset and noise, input voltage uncertainty may incur in a bit-flip and thus a Single Event Upset (SEU). This work has found that the DT is less reliable than the SA. Additionally, the proposed analysis foretells failure conditions in harsh environments. At the best of our knowledge, SA and DT drawback over temperature is first revealed in the available literature by this work.

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