Very High Sustainable Forward Current Densities on 4H-SiC p-n Junctions Formed by VLS Localized Epitaxy of Heavily Al-Doped p++ Emitters

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Abstract. This study deals with the electrical characterization of PiN diodes fabricated on a 4°off-axis 4H-SiC n^+ substrate with a n^- epilayer (1×10^{16} cm^{-3} / 10 µm). Optimized p^{++} epitaxial areas were grown by Vapour-Liquid-Solid (VLS) transport to form p^+ emitters localized in etched wells with 1 µm depth. Incorporated Al level in the VLS p^{++} zones was checked by SIMS (Secondary Ion Mass Spectroscopy), and the doping level was found in the range of $1\text{-}3\times10^{20}$ $at.cm^{-3}$. Electrical characterizations were performed on these PiN diodes, with 800 nm deposit of aluminium as ohmic contact on p-type SiC. Electrical measurements show a bipolar behaviour, and very high sustainable forward current densities $\geq$ 3 $kA.cm^{-2}$, preserving a low leakage current density in reverse bias. These measurements were obtained on structures without any passivation and no edge termination.

Introduction

Continuous improvement of bulk and epilayers of 4H-SiC semiconductor materials, allows currently the marketing of power devices. However, technological difficulties still remain unresolved, like the implementation of a fully satisfactory process to locate p-type doping area into 4H-SiC. Indeed, ion implantation is the only viable technique in industry to perform localized p^+ doping, however with significant drawbacks [1]. The damages created during ion implantation require a high temperature annealing (~1700°C or higher [2]) to both partially activate the Al elements and restore the crystal quality. Moreover, in practice, with standard ion implanter energy (< 200 keV), the depth of the p-type implanted areas is limited to a few hundreds of nm, which can lead in turn to severe design restrictions. To solve this problem, VLS localized epitaxy has been previously proposed by some of the authors as an alternative to implement deeper localized Al doping at high concentrations [3, 4]. Further works have resulted in the improvement of localized VLS process, yielding optimized structural morphology [5], preserving a threshold voltage of ~ 3 V in forward bias, value predicted by the classical theory, on a 4H-SiC p-n junction, and eliminating the need of high temperature post-growth annealing (previously ~1700°C) [6]. To the best of our knowledge, this electrical behaviour has never been obtained before with such low temperature doping process (1100°C). This study was followed with a new one whose aim was to increase the deposit thickness up to 1 µm [7]. Implementing these new p-type VLS layers with an adequate technological process has allowed us to obtain 4H-SiC diodes withstanding spectacular high current densities in forward bias, and providing low leakage current densities in reverse bias. Hereafter are presented elements of the technological process and the J-V characteristics of these diodes which clearly present a bipolar behavior (light emission in forward bias).

Experimental section

The manufacturing process to prepare the sample, and details about the optimization of VLS localized epitaxy have been reported elsewhere [7]. After VLS growth sequence, the amount of Al incorporated into the grown layer (doping profile) was determined by Secondary Ion Mass Spectrometry (SIMS) for different diameters of the wells. The doping uniformity was checked.

Then, to fabricate the PiN diodes (see Fig.1), classical Ni-based ohmic contacts were deposited on the back side of the n-type substrate by e-beam evaporation, followed by a Rapid Thermal Annealing (RTA) at 900°C in argon atmosphere. Because of the high doping level of the VLS p^{++} epilayers, it was possible to get ohmic contacts on these p-type layers just by depositing an Al layer (by sputtering), i.e. without annealing this metallization. This Al layer was thick enough (800 nm) to get full coverage of the rather rough VLS epilayers surface (see Fig. 2), presenting a pronounced step-bunching which is a good evidence that the growth from the melt occurred in a homo-epitaxial way.

The as-fabricated PiN diodes were electrically characterized in order to validate the quality of the p-n junction, using a Keithley 2636 System Measure Unit with a "Signatone S1160" probe station. These measurements were done on vertical diode configuration, at room temperature. Note that neither passivation nor edge termination (such as guard rings, mesa or JTE) were used.

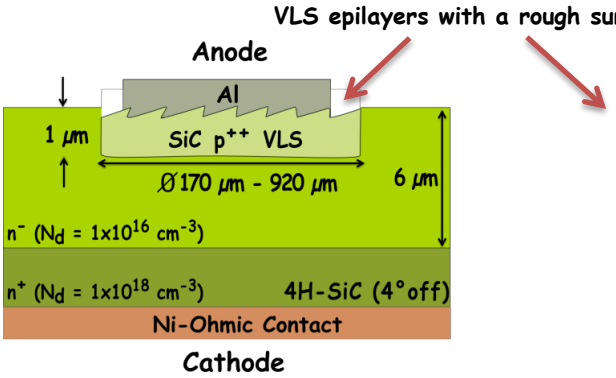

Figure 1: Schematic cross sectional view of the fabricated PiN diodes, with p^{++} emitter formed by VLS epitaxy

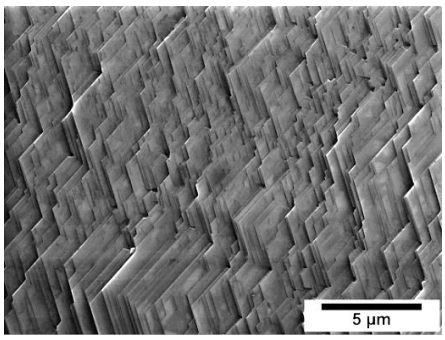

Figure 2 : SEM image (top view), surface morphology over a VLS thick layer

Results and discussions

As a first result, most of the aluminum concentration values measured by SIMS were in the range 1-3×10^{20} at.cm^{-3} (see Fig. 3) with a nearly constant value over the layer thickness, clearly visible for the largest diodes (Ø 920 µm) where the deposit thickness is ~ 900 nm. It should be emphasized that such a high and constant doping level is quite difficult to be reached by standard CVD or by ion implantation without degradation of the layer crystalline quality. The thickness values, measured by SIMS, in the range of 200-900 nm, are in agreement with those measured by Tencor stylus profilometer from the difference between the depth of the etched well, before and after VLS growth [7].

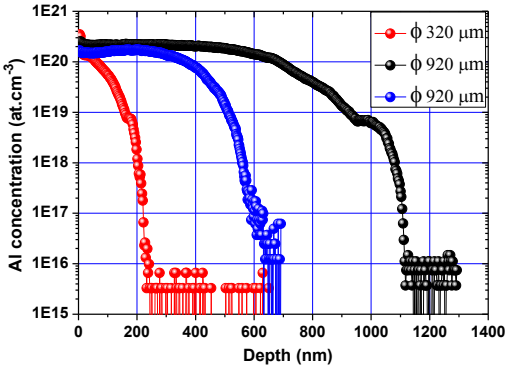

Figure 3: SIMS depth profiles of Al concentration in SiC layers grown by VLS

Typical current density vs. voltage (J-V) characteristics, measured on diode structures with VLS grown emitters are reported in Fig. 4. For a better readability, only a few J-V characteristics amongst the more representative have been plotted. The total current is limited to 1A in all cases due to instrumental limitations of the K2636 SMU unit.

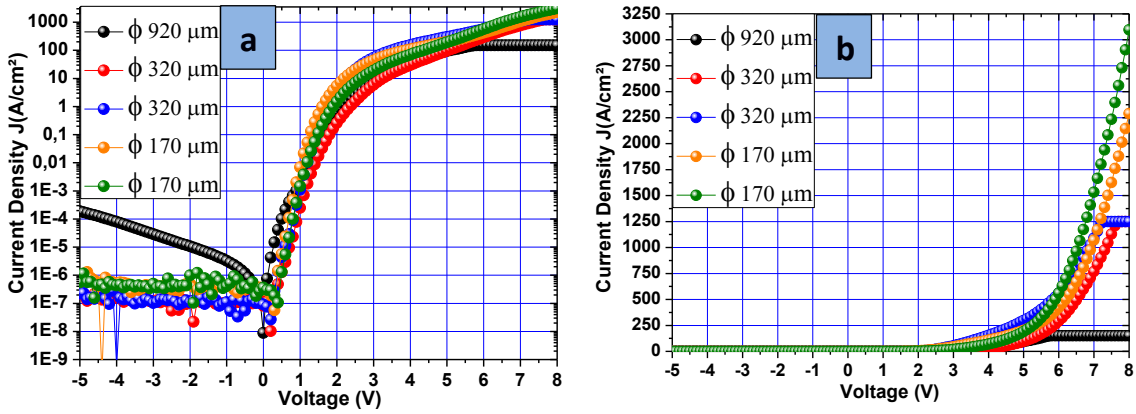

Figure 4: J-V behaviors as a function of the diameter of the well
(a) Reverse and forward bias in logarithmic scale and (b) forward bias in linear scale.

In forward bias, PiN diodes exhibit spectacular high and sustainable current densities: from 150 A.cm^{-2} for Ø 920 µm (limited by the measurement power compliance) to several kA.cm^{-2}, in the range 1250-3000 A.cm^{-2} for the smaller ones. Measured threshold voltages are around ~ 3 V, which is the typical threshold voltage for 4H-SiC p-n junction. Moreover, as an improvement over a previous report [7], the current density curves overlap quite well in forward bias, confirming that the metal deposit of the front side top contact (800 nm thickness) is now thick enough to fully cover the whole VLS layers. Such an optimized front side top contact avoids high electric field spots inducing premature breakdown. In reverse bias, leakage current density is rather low, measured in the range of 10^{-6}-10^{-7} A.cm^{-2} for diodes of smaller diameters, and surprisingly higher for Ø 920 µm, measured in the range of 10^{-5}-10^{-4} A.cm^{-2}, unlike previously reported value of leakage current density of ~ 10^{-8} A.cm^{-2} [7]. The high leakage current density for Ø 920 µm diodes is probably due to device processing issues. On the border of the anode contact, the metal is probably not completely etched and it slightly overlaps with the n-zone at the well edge, resulting in a parasitic Schottky contact in parallel with the p-n junction.

Then, repetitive current-voltage measurements in reverse regime were carried out. A series of tests at the same reverse voltage was performed on the same diode in order to study the evolution of the leakage current. Compliance has been fixed at 10 or 100 µA, depending on the test, in order to avoid the destruction of the diode. Fig. 5 reports results of measurements performed on Ø 170 µm diodes.

In order to compare our results with those previously presented in [6], breakdown voltage tests were performed under the same conditions, i.e. in air and at room temperature. In the present case, breakdown voltage V_{BR} is estimated at - 420 V. Due to the low compliance at 10 µA, the diode is not destroyed when breakdown begins at ~ 420 V. In the second test, with the same compliance, pre-breakdown leakage current is a little higher. No degradation is observed between 2nd and 3rd test. But for the third test, compliance has been set to 100 µA, and subsequently the diode has been a little more degraded.

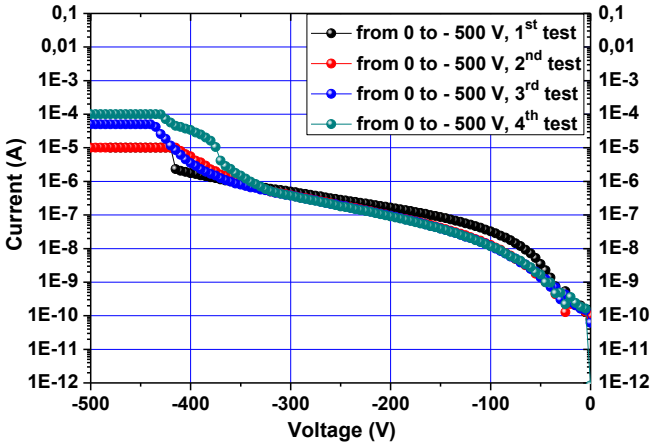

Figure 5: Breakdown voltage test of PiN diodes (Ø 170 µm) without passivation or edge termination

Indeed, on the 4th pre-breakdown test, the current increases drastically at ~370 V. For such a doping level and thickness, 420 V represents η = 38 % of the theoretical V_{BR} calculated in ideal 1D planar model. η is the "blocking efficiency" of the junction. In a previous study [6], the experimental breakdown voltage was as low as 50 V, which represented only 2 % of the theoretical value. As a result, the net increase of the blocking efficiency confirms the beneficial effects of the crystalline quality optimization of the VLS epilayers.

Conclusion

SIMS analysis were performed on p^{++} VLS epilayers, and a doping level in the range of $1\text{-}3\times10^{20}$ at.cm^{-3} has been measured, confirming deposit thickness in the range of 200-900 nm. Then, PiN structures were implemented including these optimized p^{++} VLS layers, together with an optimized technological process, which has provided 4H-SiC diodes presenting a bipolar behaviour, and very high sustainable forward current densities ≥ 3 kA.cm^{-2} while preserving a low leakage current density in reverse bias. These results were obtained without passivation and edge termination. Reverse I-V measurements were carried out and a net increase in blocking efficiency, up to 38 %, was found, as compared to 2 % in our previous study before optimization of VLS growth process. These improvements in blocking efficiency confirm the beneficial effects of the VLS crystalline quality optimization [7]. Even better performances can be expected in the future from diodes with adequate passivation and edge termination.

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