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A 14-b Two-step Inverter-based $\Sigma\Delta$ ADC for CMOS Image Sensor

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***Abstract*—This paper presents a 14-bit Incremental Sigma Delta (I$\Sigma\Delta$) analog-to-digital converter (ADC) suitable for a column wise integration in a CMOS image sensor. A two-step conversion is performed to improve the conversion speed. As the same $\Sigma\Delta$ modulator is used for both steps, the overall complexity is reduced. Furthermore, the use of inverter-based amplifiers instead of operational transconductance amplifier (OTA) facilitates the integration within the column pitch and decreases power consumption. The proposed ADC is designed in 0.18 μm CMOS technology. The simulation shows that for a 1.8 V voltage supply, a 20 MHz clock frequency and an oversampling ratio (OSR) of 70, the power consumption is 460 μW, achieving an SNR of 83.7 dB.**

***Index Terms*—ADC, incremental, sigma-delta ($\Sigma\Delta$), two-step, CMOS Image Sensor, column-parallel ADC, second-order $\Sigma\Delta$, inverter-based amplifier**

I. Introduction

High quality CMOS imaging sensor (CIS) arrays are reaching performance levels close to scientific CCD arrays. Frame rate and pixel pitch have increased, while read-out noise level has quickly fallen. These developments are raising considerably the requirements on the analog-to-digital (ADC) converter necessarily present in the image processing chain. Several improvements have been tried and developments in this field have arguably converged to column-parallel ADC converter arrays, because this configuration has been shown to yield the best tradeoff among pitch, conversion rate, conversion resolution and power consumption.

Fitting the ADC in the ever narrower pixel pitch has driven the converter architectures from straightforward cyclic towards successive approximation register (SAR) and single-slope (SS) converters. SS converters are widely used because of their simplicity and low power consumption. However, they are slow, and it's difficult to obtain more than 10-bits of resolution. To raise the resolution above this, the trend is to move towards hybrid converters, where two kinds of converters work in tandem.

Conceptually, the conversion is done in two steps: first the most significant bits (MSBs) are extracted generating an analog residue. In the second step, this residue is converted by the second stage and the least significant bits (LSBs) are obtained. In the Nyquist converters, the analog residue in intermediate steps is proportional to the original analog input. In oversampling converters, such as Sigma-Delta ($\Sigma\Delta$) ADCs, the residue at every step is proportional to the integral of an error signal. In imaging sensor applications, one uses incremental $\Sigma\Delta$ (I$\Sigma\Delta$) ADCs, where the integrators are reset before each conversion. I$\Sigma\Delta$ converters are able to achieve very high resolution while using simple circuits that can be easily scaled down.

For example, Seo *et al*. [1] have developed a 17 bits I$\Sigma\Delta$+cyclic ADC, and Shin *et al*. [2] introduced a 14.3-bits I$\Sigma\Delta$+SAR ADC, both focusing imaging systems. However, these architectures still required moderately complex circuitry due to the use of Nyquist converters in one of the steps. The work reported in Oike et al. [3] and Chen et al. [4] have pushed the concept further by using I$\Sigma\Delta$ ADCs for both steps. The overall OSR is then decreased compared to a standard I$\Sigma\Delta$ ADC and the implementation of the hybrid ADC takes less area and power. A further improvement of I$\Sigma\Delta$ ADCs was the use of inverters to implement the integrator of the $\Sigma\Delta$ loop, as reported by Chae *et al*. [5], as well as Wang *et al*. [6] and Tang *et al*. [7]. However, to obtain a high DC gain over an appreciable output voltage range is a challenging task. Still, the key advantage of inverter-based I$\Sigma\Delta$ ADC is the reduction in area and power consumption.

In this paper, a 14-bit two-step inverter-based I$\Sigma\Delta$ using second-order cascaded integrators feed-forward (CIFF) is introduced. The main contribution of our proposal is the use of a second-order modulator for both steps, in addition to the use of gain-boosted inverter-based integrators. This paper is organized as follows; In section II, the high-level I$\Sigma\Delta$ architecture is presented. In section III, the circuit implementation of the ADC is shown. In section IV, results from simulations are shown and compared to similar work. Section V concludes this article.

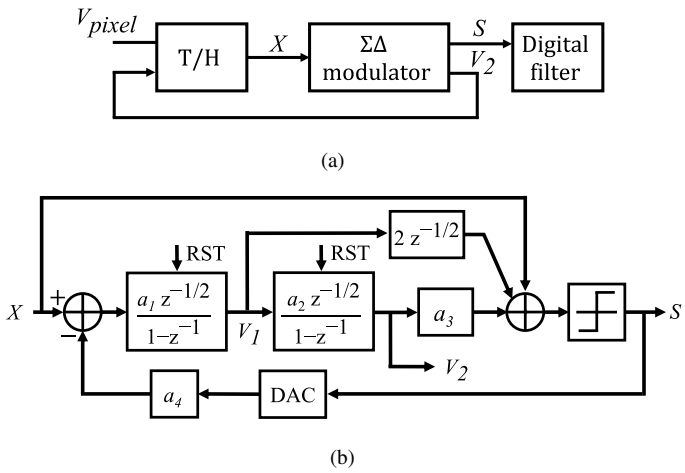

Figure 1. (a) High-level view of two-steps architecture, schematic of the sample and hold and (b) the IΣΔ second order modulator

II. Proposed two-step ADC architecture

The high-level view of the proposed ADC architecture is shown in fig.1(a). The architecture is composed of a track and hold (T/H), a ΣΔ modulator and a digital filter. The chosen modulator is a second-order CIFF architecture [8] shown in fig.1(b). Our two-step IΣΔ ADC first performs a coarse conversion of the pixel value stored in the T/H, giving an analog residue V_2 loaded into the T/H. Then a fine conversion is performed on this residue, using the same modulator. The residue of the coarse conversion can be expressed as follows,

$$V_2[M1] = a_1 a_2 \sum_{K=1}^{M_1-1} \sum_{i=1}^{K-1} (X[i] - a_4 S_1[i]) \qquad (1)$$

with a_1 and a_2 coefficients in the modulator, M_1 the number of samples for the first step and S_1 the bitstream of the coarse conversion. The fine conversion is then realized on this residue. The final reconstructed signal is then a linear combination of both bitstream and it can be written as,

$$\hat{X} = K_1 \sum_{K=1}^{M_1-1} \sum_{i=1}^{K-1} S_1[i] + K_1 K_2 \sum_{K=1}^{M_2-1} \sum_{i=1}^{K-1} S_2[i] \qquad (2)$$

with,

$$K_i = \frac{2}{a_1 a_2 (M_i - 1)(M_i - 2)}, i = 1, 2 \qquad (3)$$

where M_2 is the number of samples for the second step, S_2 the bitstream of the fine conversion and K_i the coefficient associated with the coarse and fine conversion. To maximize the resolution, M_1 and M_2 must be equal [9] with M_1 = M_2 = 35.

In a two-step ADC the range difference between the output of the first step of the conversion ($V_2[M_1]$) and the effective input of the second step can highly deteriorate the overall resolution. To optimize this range difference , it is well known that IΣΔ must be analyzed in the temporal domain instead of the frequency domain. One can see from (1) that the residue depends on the modulator coefficient a_1, a_2 and a_4. They must be adjusted to maximize the residue range within the input range. This optimization must also guarantee a non-saturation of the amplifier. For this design, the amplifier input range is limited to 85% of the reference scale and integrators levels do not go above 90% of the reference. The parameters a_1, a_2, a_3, a_4 are set by simulation and their values are respectively 0.5, 0.5, 0.75 and 0.5. With this set of parameters, the simulation of the maximum integrator value and the residue value are respectively shown in fig.2. In both results, values do not exceed the saturation or output limit for any input. The residue range is about 75% of the input range of the modulator. Since the saturation of the amplifier is avoided and the residue range fits the input range of this modulator, this architecture is suitable for a two-step ADC.

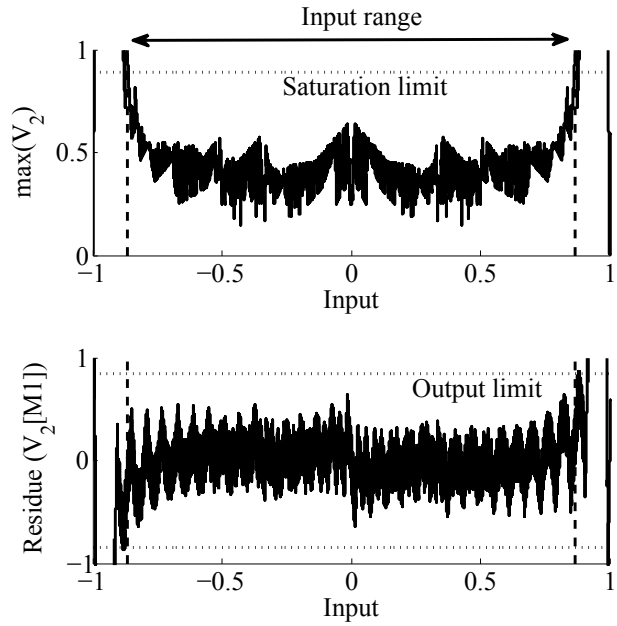

Figure 2. maximum of second integrator level (top) and residue values (bottom) with both axis scaled to ΣΔ reference level

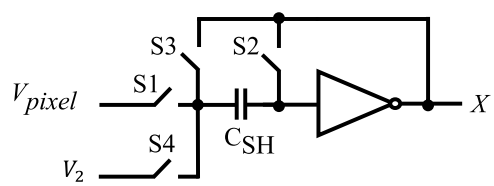

Figure 3. Schematic of the T/H with an auto-zeroing switched-capacitor

III. Circuit implementation

The T/H circuit and the switched capacitor circuit of the modulator are shown in fig.3 and fig.4. In both circuits, amplifiers have been designed with inverters to reduce area and power consumption. Since inverter amplifiers have very large offset variation due to the process we use an auto-zeroing scheme proposed in [5] for the ΣΔ modulator circuit. A similar method is applied to the T/H. Before the beginning

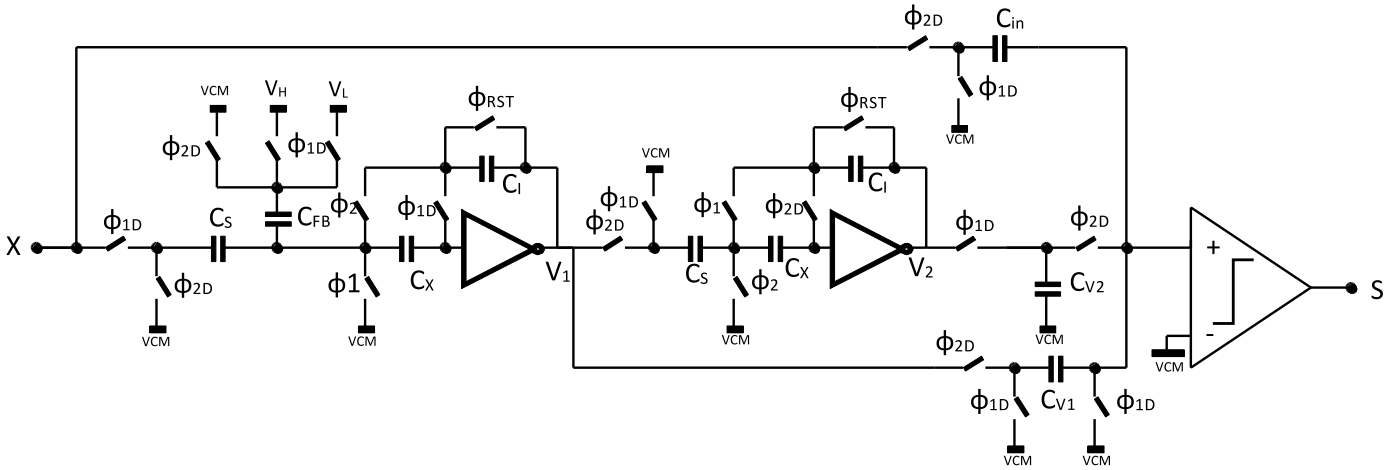

Figure 4. Switched capacitor circuit of the 2nd order modulator

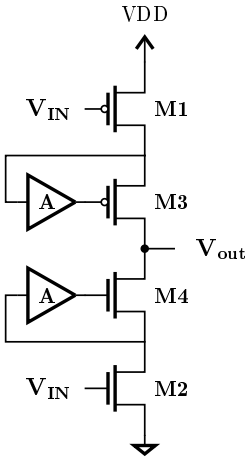

Figure 5. Gain boosted amplifier

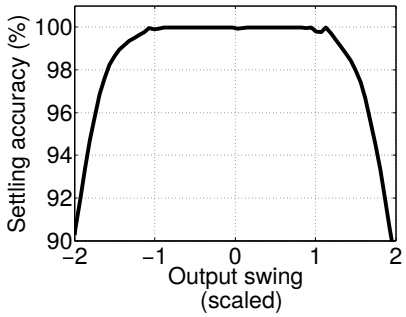

Figure 6. Settling accuracy of an integration step

of the coarse conversion, the pixel value is loaded into the capacitance C_{SH} (switches S1 and S2 closed, S3 and S4 opened). Then the value of the pixel is disconnected from the amplifier (S1 and S2 being open). Then S3 is closed canceling the offset of the amplifier and storing the pixel value at the end of the operation. To load the residue $V_2[M_1]$ into the T/H at the end of the coarse conversion, the switch sequence is the same except that S4 is closed instead of S1 to select the right input. As the switched capacitor circuit is used for both steps, the CIFF architecture used requires additional reset operations to correctly perform the second step. These operations are also justified by the delayed values send to the comparator. The comparator used is a low kickback noise architecture [10].

To perform a 14-bit resolution conversion, a minimum DC gain of 76 dB is needed [9]. The DC gain of an inverter is expressed as follows

$$A_v = (g_{m(N)} + g_{m(P)})(r_{o(N)}//r_{o(P)}) \quad (4)$$

where $g_{m(N)}$ and $g_{m(P)}$ represent the transconductance of NMOS and PMOS respectively, $r_{o(N)}$ and $r_{o(P)}$ their output resistance. From eq.(4) one can see that the gain can be increased with $r_{o(N,P)}$. Simple and cascoded inverters cannot reach a sufficiently high gain in this technology. Our solution is to add gain-boosting to the inverter [13]. The schematic of a gain-boosted inverter is shown in fig.5. Thanks to the gain boosting amplifier circuit, the effective transconductance of the cascode transistor is increased, hence considerably increasing the output resistance of the inverter-based amplifier. The output linearity swing is the output range of the amplifier where a minimum DC gain of 76 dB is ensured [9]. A trade-off has to be found between the maximum DC gain and output linearity. To ensure good output linearity swing, low-threshold transistor are used in the gain-boosting module. With this amplifier, linear output range reaches 50% of the supply range. The settling accuracy of a transition from the voltage common mode to the extreme value is shown in fig.6. The X-axis, the output swing, is scaled to the $\Sigma\Delta$ reference. From this figure, one can observe that an accuracy of 99.9% is guaranteed for an output swing of 95% of the I$\Sigma\Delta$ reference.

The supply voltage of the circuit is 1.8 V. The static current for a gain-boosting module is about 4 μW and 140 μW for an amplifier.

Table I
PERFORMANCE COMPARISION

	[1]	[11]	[12]	[3]	This work
Technology (μm)	0.18	0.35	0.18	0.15	0.18
ADC architecture	$\Sigma\Delta$+Cyclic	$\Sigma\Delta$+SAR	$\Sigma\Delta$+Cyclic	2 step $\Sigma\Delta$	2 step $\Sigma\Delta$
Sampling rate (kS/s)	30	150	50	-	200
Resolution	17	14.3	10.2	12	14
Power (μW)	345	300	13	363	460
DNL (LSB)	-0.88/1.38	-0.79/0.97	-	-0.7/1.8	-
INL (LSB)	-26.3/35	-1.7/2.79	-	-22/20	-
SNDR (dB)	85	-	63	-	83
FoM (fJ/step)	790	100	220	-	185

IV. RESULTS

The proposed two-step inverted based ADC is simulated in 0.18 μm technology. The ADC OSR is 70 and its bandwidth is up to 200 kS/s. Output spectrum is presented in fig.7 with an input signal frequency of 200 kHz and a 256 points FFT. This work achieves a SNR of 83 dB. The figure-of-merit (FoM) is written as follows,

$$FoM = \frac{P}{2^{ENOB}.Fs} \tag{5}$$

with P the power dissipation of the ADC, *ENOB* the effective number of bits calculated from the SNR, and F_s the sampling frequency of the ADC. This ADC achieves a FoM of 185 fJ/step. A comparison with similar works is shown in Table I. This work consumes lower power and is very competitive compared to previous results.

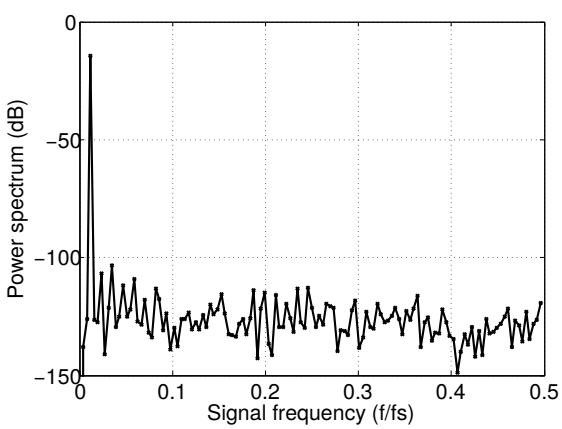

Figure 7. Simulated output spectrum of I$\Sigma\Delta$ ADC with a 256 points FFT

V. CONCLUSION

A two-step inverter-based I$\Sigma\Delta$ ADC is presented in this paper. The $\Sigma\Delta$ modulator is first analyzed. Then the circuit implementation of the T/H and the $\Sigma\Delta$ modulator is analyzed. The used gain boosting amplifier is explained. Finally simulations results show that using a supply voltage of 1.8 V, a clock frequency of 20 MHz, a total OSR of 70, this work achieves a SNR of 83.5 dB for a power consumption of 460 μW. The FoM of the ADC is 185 fJ/step. Future work consists of layout of the ADC and its implementation on chip.

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